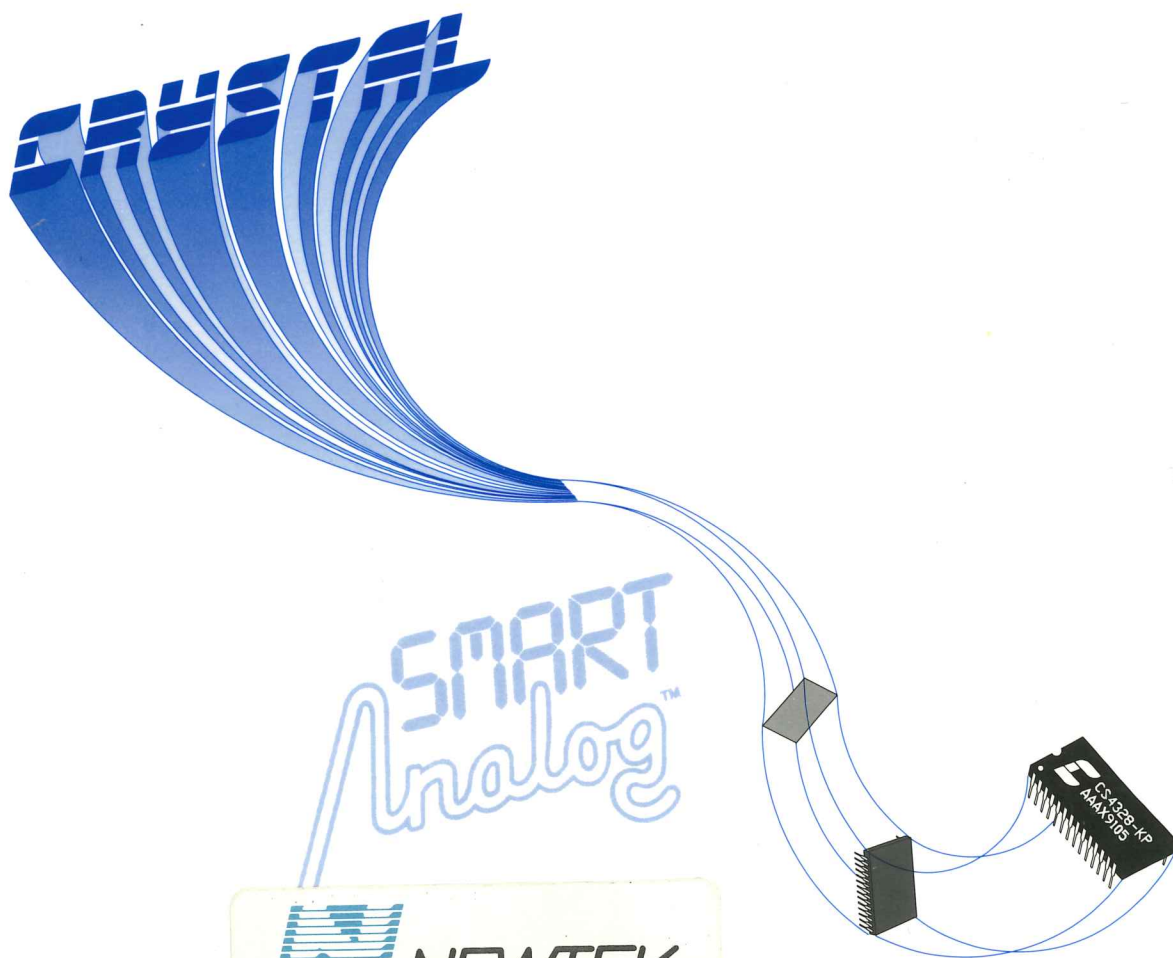


# ANALOG/DIGITAL CONVERSION IC's



**NEWTEK**

*La haute technologie en semiconducteur*

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**VOL 1 DATA BOOK**



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# Crystal Semiconductor Corporation

## Volume 1 Data Book A/D Conversion IC's

April 1992

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Products in this book may be covered by one or more of the following patents. Additional patents are pending.

U.S.A.:

4,709,225; 4,849,662; 4,804,863; 4,748,418; 4,746,899; 4,805,198; 4,851,841; 4,943,807; 4,939,516; 5,055,846; 4,918,454; 4,941,156; 4,988,954; 5,068,660; 5,079,550; 5,039,989; 5,012,244; 5,088,107; 5,087,914; 5,061,925.

Germany:

P3,642,070; P3,736,735; P3,737,279; P3,733,682.

Great Britain:

2,184,621; 2,198,306; 2,198,305; 2,195,848.

France:

2,591,753; 2,604,839.

Japan:

SHO. 61-299798.

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Digital Volume Control

Multimedia Codecs

Digital-to-Analog Converters

Analog-to-Digital Converters

AES/EBU &amp; S/PDIF Interfaces

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General Purpose &amp; Military

Seismic

DC Measurement

Transducer Interface

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Digital Volume Control

Multimedia Codecs

Digital-to-Analog Converters

Analog-to-Digital Converters

AES/EBU &amp; S/PDIF Interfaces

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### COMPANY INFORMATION

1

Crystal's proprietary SMART Analog™ design technique, incorporating analog and digital circuitry in monolithic CMOS devices, represents a powerful new technology in the semiconductor industry. This innovative approach to design eliminates many of the sources of inconsistent performance in traditional analog circuitry.

Maximum system performance is built-in from initial research on end-user requirements through product definition. Product quality and reliability is designed into the device architecture and is further assured through rigorous standards for fabrication, assembly and testing. Crystal's part numbering scheme is as follows:

#### CSLXXXX - TPNNH/R



DEVICE REVISION: DOES NOT APPEAR HERE ON PACKAGE MARK.  
REVISION IS COVERED IN DATE CODE STAMP.  
USED ONLY FOR ORDERING/TRACKING.

SPECIAL HANDLING, ALPHA ONLY A-COMMERCIAL HIGH-REL.  
B-MILITARY 883B REV. C PROCESSING

ELECTRICAL OR SPEED SPECIFICATION. (OPTIONAL) UP TO 2  
NUMERIC DIGITS. NO ALPHA CHARACTERS. SEE DATA SHEET

PACKAGE CODE -REQUIRED, ALPHA CHARACTER ONLY, NO NUMERICS

P = PLASTIC DIP S = 0.3" SOIC  
C = CERAMIC SIDBRAZE E = CERAMIC LCC  
D = CERDIP J = J-LEAD CERAMIC CHIP CARRIER  
L = PLASTIC LEADED CHIP CARRIER, J LEAD G = GULLWING CERAMIC CHIP CARRIER  
U = UNPACKAGED DIE

TEMPERATURE SPECIFICATION - REQUIRED, ALPHA CHARACTER ONLY

SIGNAL CONDITIONING/COMMUNICATION:

C = 0 °C to 70 °C  
I = -40 °C to 85 °C  
M = -55 °C to 125 °C

TEMPERATURE/ACCURACY - REQUIRED, ALPHA CHARACTER ONLY

DATA ACQUISITION:

TEMPERATURE

ACCURACY

	GOOD	BETTER	BEST
0 °C to 70 °C	J	K	L
-40 °C to 85 °C	A	B	C
-55 °C to 125 °C	S	T	U

UP TO FOUR ALPHANUMERIC DIGITS COMPRISE REMAINDER OF BASIC PART NUMBER

CRYSTAL PRODUCT LINE (PROPRIETARY PARTS; SECOND-SOURCE PARTS HAVE EXCEPTIONS):

3 = DATA ACQ. SUPPORT CIRCUITS  
4 = D/A CONVERTERS  
5 = A/D CONVERTERS  
6 = TELECOMMUNICATIONS  
7 = SIGNAL CONDITIONING  
8 = DATACOMMUNICATIONS

CRYSTAL SEMICONDUCTOR

"CS" = ALL CRYSTAL PRODUCTS; EXCEPT FOR

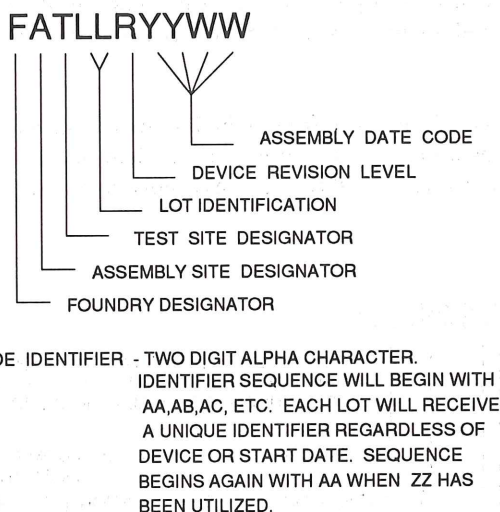
"CXT" = QUARTZ CRYSTALS

"CDB" = EVALUATION BOARD

"CX" = CUSTOM PRODUCTS

REV4

In addition to the part number, all Crystal parts have a second line of marking, which can be decoded as follows:



### **COMPANY BACKGROUND**

Crystal Semiconductor Corporation was founded in 1984 with the goal of supplying the industry with high-performance, mixed analog/digital CMOS circuits.

To meet its objectives, Crystal recruited a staff of renowned CMOS analog design engineers, a scarce resource in the industry, and teamed them with designers trained in system architecture development.

By coupling this design staff with highly qualified application and test engineers and seasoned management, Crystal has achieved several industry firsts. Systems designers now benefit from the performance and cost savings of Crystal breakthroughs such as self-calibrating ADCs, monolithic T1 interfaces and the industry's first implementations of "delta sigma" oversampling A-to-D converters.

Headquartered in Austin, Texas, Crystal sells its products worldwide through a network of manufacturer's representatives. Crystal's entire marketing and sales organization is committed to providing quality products and reliable, rapid service.

## **QUALITY AND RELIABILITY INFORMATION**

Crystal Semiconductor is committed at every level of the company to the highest possible standards of quality and reliability in its products. This commitment is evident in all phases of operations: initial product definition, design, fabrication, assembly, test, qualification and customer service. Product quality and reliability is an active concern of each Crystal employee.

### ***In Product Definition***

To ensure maximum system performance, Crystal works with users to identify and quantify the parameters, including quality and reliability issues, that best serve customer needs. Quality and reliability become part of the design goals, along with electrical performance and cost.

### ***In Design***

Conservative 3-micron CMOS design rules are the basis for all current Crystal products. In addition, extensive use is made of proven standard cells to drastically reduce the possibility of design errors.

Each pin in every SMART Analog product is designed to meet ESD levels of at least 2500V when tested per MIL STD 883C, Method 3015. Each pin is also designed to withstand more than 200mA of DC latch current.

Crystal SMART Analog design architectures provide quality and reliability comparable to leading digital devices and memories. This is far superior to traditional analog ICs and hybrids. On-chip digital error correction provides stable performance over time and temperature by taking advantage of digital controls that are insensitive to parametric analog problems such as leakages and shifts in threshold voltage. Using Crystal devices, designers have fewer

error sources to consider. The result is a less complicated, more reliable system.

### ***In Fabrication and Assembly***

Crystal ensures reliable delivery of quality parts by accessing established foundries in multiple locations (Japan and California today). Each fabrication facility is qualified by Crystal. Assembly is performed both domestically and off-shore under carefully documented and well-controlled conditions.

Wafer fabrication and assembly processes undergo in-line quality inspections. Wafers are inspected optically to guidelines based on MIL STD 883C, Method 2010. Each die is electrically tested using proprietary test circuits that verify key parameters. Following assembly, packages are subjected to a variety of mechanical inspections to verify integrity and insure high quality. (For example, x-ray inspection to 3.0 percent LTPD is one of the standard production tests.)

### ***In Test***

In a break from traditional analog components, Crystal's SMART Analog products include basic test capabilities designed into each chip. Crystal's in-process quality assurance program uses this designed-in testability to monitor and track the performance and quality of these complex circuits. Finished packaged components are tested 100 percent electrically, over temperature where critical parameters are involved. With these extensive quality programs, Crystal guarantees outgoing electrical quality levels on all data sheet specifications to a 0.065 percent AQL level over the full specified temperature range.

Throughout the assembly and test phases, traceability to the original wafer lot is carefully maintained.



### In Product Qualification

Before any Crystal product is released to production and shipped in volume, it must undergo a thorough qualification program. Crystal has separate qualification criteria to address both long-term reliability and infant mortality so that the sources of failure are identified and eliminated. Crystal uses military specifications as the guidelines for reliability tests, methods and procedures. (See Table 1.)

To ensure reliability of the design and processes, full qualification requires that three non-consecutive lots are used during the qualification program. Fabrication and assembly facilities are audited every six months and periodically monitored. Any major design or process changes restart the qualification procedure.

These steps guarantee that Crystal products maintain the high standards of reliability designed-in from the start.

**TABLE 1 - QUALIFICATION TESTS**

TEST	MIL STD 883C METHOD	CONDITION	INFANT MORTALITY TESTS		LONG-TERM RELIABILITY TESTS		
			DURATION	PASS/FAIL CRITERION	DURATION	PASS/FAIL CRITERION	CRYSTAL GOAL
OPERATING LIFE	1015 COND D	+125°C, Dynamic Bias ±5.5V Supplies	168 hrs	0.25%	1000 HRS	75 FITS†† (25°C/60%UCL 1.0 eV Act. Energy)	10 FITS† (25°C/ 60% UCL)
TEMPERATURE HUMIDITY STRESS (Plastic Parts)		+85°C/85% RH Static Bias	168 hrs	1.0 LTPD	1000 HRS	3.0 LTPD	1.0 LTPD
TEMPERATURE CYCLING Hermetic Packages	1010.5 COND C	-65°C to +150°C Then Gross Leak Test	100 CYCLES	1.0 LTPD	1000 CYCLES	3.0 LTPD	1.0 LTPD
TEMPERATURE CYCLING Molded Packages	1010.5 COND B or *	-55°C to +125°C or -40°C to +125°C	100 CYCLES	1.0 LTPD	500 CYCLES	3.0 LTPD	1.0 LTPD
THERMAL SHOCK	1011.4 COND B or **	-55°C to +125°C or -40°C to +125°C *** Then Gross Leak Test	100 CYCLES	1.0 LTPD	500 CYCLES	3.0 LTPD	1.0 LTPD
AUTOCLAVE (Plastic Parts)		+121°C/100% RH 2 Atmosphere, No Bias	48 HRS	1.0 LTPD	144 HRS	3.0 LTPD	1.0 LTPD
CENTRIFUGE	2001	30 Kg/Y1 Axis				5.0 LTPD	1.0 LTPD
ELECTROSTATIC DISCHARGE	3015			1500V-0 Fail	5 UNITS, ALL PINS	1500V-0 FAIL	4000V
LATCH UP		dc Current		100 mA-0 Fail	5 UNITS, ALL PINS	100mA-0 FAIL	200mA

\* JEDEC STD 22-B, A104 COND B

\*\* JEDEC STD 22-B, A106 COND C

\*\*\* For hermetic Packages Only

† Equivalent to 50 FITS, 70°C/60% UCL, 0.7 eV

†† Equivalent to 300 FITS, 70°C/60% UCL, 0.7 eV

Contact Crystal for individual product ESD information.

### *In Customer Service*

Compliance with purchasing requirements is ensured through the use of Crystal's computerized system "Compass"(Crystal On-line Marketing Production and Sales System). This processing system ensures that all orders are entered correctly, scheduled properly, produced according to schedule, and shipped with zero discrepancies.

All systems and procedures at Crystal Semiconductor are aimed at continuously improving the quality and reliability of our products and services to meet the needs of our customers.

Crystal's philosophy on quality is to anticipate problems and develop systems and controls to alleviate possible problems. It is a well stated fact by Juran and Deming, two of the nation's foremost experts on quality, that 85% of all quality problems are system related and 15% are worker related. Therefore, Crystal devotes its major quality efforts toward preventing system related quality problems.

Crystal has a very aggressive audit program in place. Monthly internal audits are performed to insure compliance to the extensive documentation of instructions and criteria for testing and inspection. Semiannual vendor audits are performed on the assembly and fabrication foundries. Vendor audits insure the adequacy and compliance of specifications, product flow,

training, process controls and cleanliness. All internal and external audits have provisions for ratings and a system for corrective action requirements. These frequent audits by assembly, fabrication and quality engineers maximize system quality compliance.

As an added measure of continued high quality from assembly and fabrication foundries, thorough incoming inspections are performed. Wafer level optical inspection is based upon guidelines of MIL STD 883C, METHOD 2010. Test die are electrically tested to verify compliance to key process parameters based upon design rules specifications. These electrical parameters include threshold voltages, breakdown voltages, material resistance, and contact resistance. Assembly packaging inspection includes external visual, marking permanency, solderability, x-ray, hermeticity, die shear, wirepull and internal visual.

Preventive measures are very much in force in the final test area. Equipment calibration and preventive maintenance procedures are strictly adhered to. Handling procedures for Electrostatic Discharge are in place throughout the test areas. Non-conforming material is segregated until corrective action is agreed upon. There are controlled procedures for releasing new test programs and new test equipment to the production environment. In summary, Crystal Semiconductor is committed to meet the quality requirements of its customers.

## ● Notes ●

**GENERAL INFORMATION 1****DIGITAL AUDIO: DIGITAL AUDIO PRODUCTS 2**

Digital Volume Control  
Multimedia Codecs  
Digital-to-Analog Converters  
Analog-to-Digital Converters  
AES/EBU & S/PDIF Interfaces

**DATA ACQUISITION: ANALOG-TO-DIGITAL CONVERTERS 3**

General Purpose & Military  
Seismic  
DC Measurement  
Transducer Interface

**SUPPORT FUNCTIONS: SUPPORT FUNCTION PRODUCTS 4**

Power Monitor  
Track & Hold Amplifiers  
Voltage References

**COMMUNICATIONS: COMMUNICATIONS PRODUCTS 5**

T1/CEPT Line Interfaces & Framers  
Jitter Attenuators  
T3 Receiver  
Local Area Network I.C.s  
DTMF Receivers

**MISCELLANEOUS: APPLICATION NOTES & PAPERS 6****APPENDICES 7**

Radiation Information  
Reliability Calculation Methods  
Package Mechanical Drawings

**SALES OFFICES 8**



## INTRODUCTION

Digital audio products include a wide variety of A/D and D/A converters, along with S/PDIF & AES/EBU interfaces and a digitally controlled volume/level adjusting device.

### CS5326/7/8/9 and CS5336/8/9 Delta-Sigma Audio A/D Converters

This new class of device features 64X oversampling, using a Delta-Sigma architecture with resolutions of 16 or 18-bits. Output word rates can be from 1 kHz to 50 kHz. These stereo parts have 2 sample and holds, dual Delta-Sigma modulators, two anti-aliasing and decimation filters, and a voltage reference, all in a 28-pin package. Performance measurements include 95 dB dynamic range in stereo mode, up to 100 dB in mono mode, along with 0.0015% THD.

### CS5389 Analog to Digital Converter

The CS5389 is Crystal's newest audio A/D converter aimed at the professional audio market. Dual differential inputs, with special modulator design, yield a dynamic range of 107 dB. Excellent noise rejection and low idle tones yield a superbly performing A/D Converter.

### CS5349 Single Supply, Stereo A/D Converter for Digital Audio.

The CS5349 is a complete, 16-bit analog-to-digital converter for stereo digital audio systems that require a single +5V supply. Similar to the CS5339, the CS5349 features 64X oversampling Delta Sigma conversion with on-chip sample and hold, filtering and voltage reference in a 28-pin package.

**Audio A/D Converter Comparison Table**

Device	CS5326	CS5327	CS5328	CS5329	CS5336	CS5338	CS5339	CS5349	CS5389
Number of Bits	16	16	18	18	16	16	16	16	18
Dynamic Range (dB)	95	95	100*	100*	95	95	95	90	107
SOIC Package	-	-	-	-	✓	✓	✓	✓	✓
Filter Passband (kHz)	0-22	0-20	0-22	0-20	0-20	0-22	0-22	0-22	0-22
Filter Transition Band (kHz)	22-26	20-24	22-26	20-24	20-26	22-28	22-28	22-28	22-28
Stop Band Attenuation (dB)	-86	-86	-86	-86	-80	-80	-80	-80	-80
Overrange Tag Bits	-	-	-	-	✓	✓	✓	✓	✓
Left/Right Tag Bits	-	-	-	-	✓	✓	✓	✓	✓
Master Clocking Mode	-	-	-	-	✓	✓	✓	✓	✓
SCLK active edge	↑	↑	↑	↑	↑	↑	↓	↓	↓
Master Clock Frequency (XFs)	128	128	128	128	256/384	256/384	256/384	256/384	256/384
Power Supply Voltages (V)	±5	±5	±5	±5	±5	±5	±5	+5	±5
Operation < 30 kHz without TEST Mode	-	-	-	-	✓	✓	✓	✓	✓
Power Consumption mW	450	450	450	450	400	400	400	325	550

\* In Mono Mode

All frequencies are with an output word rate of 48 kHz

### **CS4328 Digital to Analog Converter**

The CS4328 is the industry's first complete stereo digital-to-analog output system. This 18-bit stereo D/A converter uses Crystal's well established oversampling converter techniques.

The CS4328 includes the major system elements of 8X interpolation filter, 64X Delta-Sigma modulator, 1-bit D/A converter and a 124 dB signal-to-noise ratio analog anti-imaging filter, all in one packaged, tested, solution. The device features patented Delta-Sigma architectures to maintain excellent distortion performance, even at low signal levels. The output anti-imaging filters are the first to be based on a mixed linear/switched capacitor architecture. This approach is particularly insensitive to clock jitter and allows the benefit of scaling the bandwidth proportionally to the system master clock. The CS4328 is therefore adjustable for both audio and voice band applications. The flexible digital interface mates with CD player circuitry, DAT recorders and DSP's.

### **CS4303 Digital to Analog Converter**

The CS4303 is an all digital I.C. containing an 8X interpolation filter and overall 64X oversampling delta-sigma modulator. Addition of an external analog reconstruction filter yields 107 dB dynamic range with superb low level linearity.

### **AES/EBU & S/PDIF Transmitters & Receivers**

The CS8401A/2A digital audio transmitters, along with the CS8411/2 digital audio receivers, allow digital communication between audio equipment. Requiring minimum external circuitry, these IC's support both the professional AES/EBU and consumer S/PDIF formats.

The CS8401 and CS8411 have a CPU interface, and must be controlled via a CPU. The CS8402 and CS8412 have dedicated interface pins, and do not need a CPU for control. The CS8411 and CS8412 receivers have low-jitter, on-chip clock recovery.

The CS8425 is a combined transmitter & receiver intended for use in automotive applications.

### **CS4215/16 Multimedia Stereo Audio Codecs**

The CS4215 and CS4216 are complete audio coders/decoders. Each device contains 2 A/D converters, 2 D/A converters, adjustable input gain and adjustable output level. Both digital and analog filtering is included, so no external analog filters are required. The CS4215 also has a microphone input, headphone output, and a monitor speaker drive. Potential applications include audio i/o for personal computers and workstations.

### **CS3310 Digital Volume Control**

The CS3310 is a stereo volume control with a simple serial digital interface for adjusting the audio signal level. The signal path is all analog, with special low distortion circuitry. The CS3310 generates no audible "zipper" noise when the volume level is changed. The adjustable range is -98dB to +30dB in 0.5 dB steps.

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## Stereo Digital Volume Control

### Features

- Complete Digital Volume Control  
2 Independent Channels  
Serial Control  
.5 dB Step Size
- Wide Adjustable Range  
-98 dB Attenuation  
30 dB Gain
- Low Distortion & Noise  
0.001% THD  
110 dB Dynamic Range
- Noise Free Level Transitions
- Low Power Dissipation: 30 mW

### General Description

The CS3310 is a complete stereo digital volume control designed specifically for digital audio systems. It features an 8-bit serial interface that controls two independent, low distortion audio channels.

The CS3310 includes an array of well matched resistors and a low noise active output stage. A total adjustable range of 128 dB is achieved through 98 dB of attenuation and 30 dB of gain.

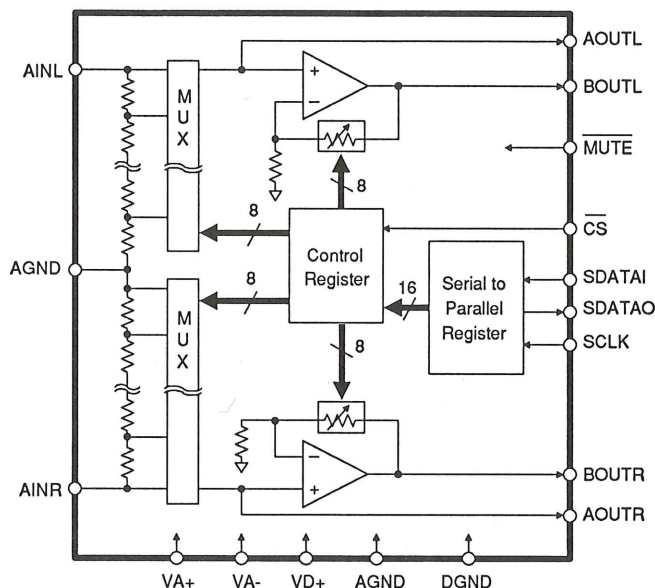
The device operates from  $\pm 5V$  supplies and accepts inputs up to  $\pm 3.75V$ . The CS3310 has a distortion of 0.005% and a dynamic range of 110 dB.

The CS3310 is housed in a 0.3" wide 16-pin DIP and also available in a 16-pin surface mount SOIC package.

### ORDERING INFORMATION:

Contact Crystal Semiconductor.

2



### Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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## •Notes•



## 16-Bit, 48 kHz, Multimedia Audio Codec

### Features

- Sample Rates Ranging From 4kHz to 48kHz
- 16-bit Linear, 8-bit  $\mu$ -law or A-law Coding
- >80 dB Signal-to-Noise Ratio
- Programmable Gain For Analog Inputs
- Programmable Attenuation for Analog Outputs
- On-chip Oscillators
- +5V Power Supply
- Microphone and Line Analog Inputs
- On-chip Anti-aliasing Filters
- On-chip Output Smoothing Filters
- Serial Digital Interface

### Description

The CS4215 is a single-chip, stereo, analog-to-digital and digital-to-analog converter using delta-sigma conversion techniques. Applications include CD-quality music, FM radio quality music, telephone-quality speech, and modems.

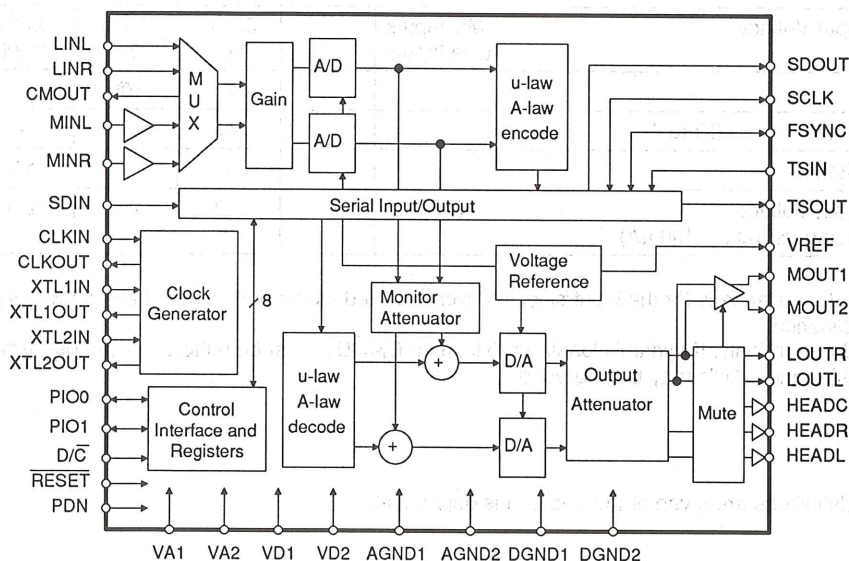
The +5V only power requirement makes the CS4215 ideal for use in workstations and personal computers.

Integration of microphone and line level inputs, input and output gain setting, along with headphone and monitor speaker drive, results in a very small footprint.

The CS4215 is supplied in a 44-pin plastic package with J-leads (PLCC).

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Ordering Information: CS4215-KL



### Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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**ANALOG CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ;  $V_{A1}, V_{A2}, V_{D1}, V_{D2} = +5\text{V}$ ;

Input Levels: Logic 0 = 0V, Logic 1 =  $V_{D1}, V_{D2}$ ; Full Scale Input Sine wave, 1 kHz; Conversion Rate = 48 kHz;  
 SCLK = 3.072 MHz; Measurement Bandwidth is 10 Hz to 20 kHz; Slave mode; Unless otherwise specified.)

Parameter *	Symbol	Min	Typ	Max	Units
<b>Analog Input Characteristics</b> - Minimum gain setting (0 dB); unless otherwise specified.					
ADC Resolution		16	-	-	Bits
ADC Differential Nonlinearity		-	-	$\pm 0.9$	LSB
Dynamic Range	Line Inputs	80	84	-	dB
	Mic Inputs	72	-	-	dB
Signal-to-(Noise + Distortion)	Line Inputs	$S/(N+D)$	-	-	dB
	Mic Inputs	72	-	-	dB
Interchannel Isolation	Line to Line Inputs	-	80	-	dB
	Line to Mic Inputs	-	60	-	dB
Interchannel Gain Mismatch	Line Inputs	-	-	0.1	dB
	Mic Inputs	-	-	0.1	dB
Frequency Response	(0 to 0.45 $F_s$ )	-0.5	-	+0.2	dB
Programmable Input Gain	Line Inputs	-0.2	-	22.7	dB
	Mic Inputs	19.8	-	42.7	dB
Gain Step		1.3	1.5	1.7	dB
Offset Error	Line Inputs	-	10	-	LSB
Full Scale Input Voltage:	Mic Inputs	0.266	0.28	0.294	$V_{pp}$
	Line Inputs	2.66	2.8	2.94	$V_{pp}$
Gain Drift		-	100	-	ppm/ $^\circ\text{C}$
Input Resistance (Note 1)		20	-	-	k $\Omega$
Input Capacitance		-	-	15	pF
CMOUT Output Voltage (Maximum output current = 400 $\mu\text{A}$ )	(Note 2)	1.9	2.1	2.3	V

Notes: 1. Input resistance is for the input selected. Non-selected inputs have a very high ( $>1\text{M}\Omega$ ) input resistance.

2. DC current only. If dynamic loading exists, then CMOUT must be buffered or the performance of ADC's and DAC's may be degraded.

\* Parameter definitions are given at the end of this data sheet.

Specifications are subject to change without notice.

**ANALOG CHARACTERISTICS** (Continued)

Parameter *	Symbol	Min	Typ	Max	Units
<b>Analog Output Characteristics</b> - Minimum Attenuation; Unless Otherwise Specified.					
DAC Resolution		16	-	-	Bits
DAC Differential Nonlinearity		-	-	±0.9	LSB
Dynamic Range (All Outputs)		80	84	-	dB
Signal-to-(Noise + Distortion) (OLB = 1)	Line Out (Note 3)	80	-	-	dB
	Headphone Out (Note 4)	60	-	-	dB
	Speaker Out (Note 4)	60	-	-	dB
Interchannel Isolation	Line Out (Note 3)	-	80	-	dB
	Headphone Out (Note 4)	-	40	-	dB
Interchannel Gain Mismatch	Line Out	-	-	0.2	dB
	Headphone	-	-	0.2	dB
Frequency Response (0 to 0.45 Fs)		-0.5	-	+0.2	dB
Programmable Attenuation (All Outputs)		0.2	-	-94.7	dB
Attenuation Step		1.3	1.5	1.7	dB
Offset Voltage Line Out		-	10	-	mV
Full Scale Output Voltage with OLB = 0	Line Output (Note 3)	2.66	2.8	2.94	V <sub>pp</sub>
	Headphone Output (Note 4)	3.8	4.0	4.2	V <sub>pp</sub>
	Speaker Output-Differential (Note 4)	7.6	8.0	8.4	V <sub>pp</sub>
Full Scale Output Voltage with OLB = 1	Line Output (Note 3)	1.9	2.0	2.1	V <sub>pp</sub>
	Headphone Output (Note 4)	1.9	2.0	2.1	V <sub>pp</sub>
	Speaker Output-Differential (Note 4)	3.8	4.0	4.2	V <sub>pp</sub>
Gain Drift		-	100	-	ppm/°C
Deviation from Linear Phase		-	-	1	Degree
Out of Band Energy (22 kHz to 100 kHz) Line Out		-	-60	-	dB
<b>Power Supply</b>					
Power Supply Current (Note 5)	Operating	-	110	140	mA
	Power Down	-	0.5	2	mA
Power Supply Rejection (1 kHz)		-	40	-	dB

Notes: 3. 10 kΩ, 100 pF load.

4. 48 Ω, 100 pF load. For the headphone outputs, S/(N+D) with 10kΩ, 100pF load is 80dB

5. Typical ratio between VA1, VA2 pins current and VD1, VD2 pins current is 50%. Values given are for unloaded outputs.

## A/D Decimation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.0	μs

## D/A Interpolation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.1/Fs	

## DIGITAL CHARACTERISTICS (TA = 25°C; VA1, VA2, VD1, VD2 = 5V)

Parameter	Symbol	Min	Max	Units
High-level Input Voltage	VIH	(VD1,VD2)-1.0	(VD1,VD2)+0.3	V
Low-level Input Voltage	VIL	-0.3	1.0	V
High-level Output Voltage at IO = -2.0 mA	VOH	(VD1,VD2)-0.2	-	V
Low-level Output Voltage at IO = 2.0 mA	VOL	-	0.1	V
Input Leakage Current (Digital Inputs)		-	10	μA
Output Leakage Current (High-Z Digital Outputs)		-	10	μA

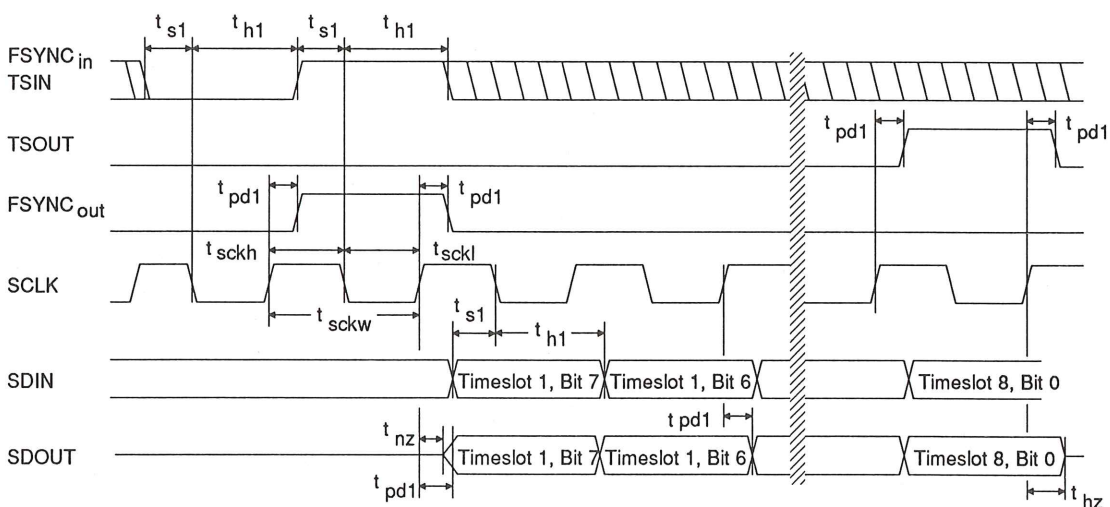


**SWITCHING CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ;  $V_{A1}, V_{A2}, V_{D1}, V_{D2} = +5\text{V}$ , outputs loaded with 30 pF; Input Levels: Logic 0 = 0V, Logic 1 =  $V_{D1}, V_{D2}$ )

Parameter	Symbol	Min	Typ	Max	Units
SCLK period Master Mode, XCLK = 1 (Note 6) Slave Mode, XCLK = 0	$t_{sckw}$ $t_{sckw}$	- 80	$1/(F_s \cdot \text{bpf})$ -	- -	s ns
SCLK high time Slave Mode, XCLK = 0	$t_{sckh}$	25	-	-	ns
SCLK low time Slave Mode, XCLK = 0	$t_{sckl}$	25	-	-	ns
Input Setup Time	$t_{s1}$	15	-	-	ns
Input Hold Time	$t_{h1}$	10	-	-	ns
Input Transition Time 10% to 90% points		-	-	10	ns
Output delay	$t_{pd1}$	-	-	20	ns
Output to Hi-Z state Timeslot 8, bit 0	$t_{hz}$	-	-	12	ns
Output to non-Hi-Z Timeslot 1, bit 7	$t_{nz}$	15	-	-	ns
Input Clock Frequency Crystals CLKIN		- 1.024	- -	27 13.5	MHz MHz
Input Clock (CLKIN) low time		30	-	-	ns
Input Clock (CLKIN) high time		30	-	-	ns
Sample rate	$F_s$	4	-	50	kHz
RESET low time (Note 7)		500	-	-	ns

Note: 6. In Master mode with BSEL1,0 set to 64 or 128 bits per frame (bpf), the SCLK duty cycle is 50%.  
When BSEL1,0 is set to 256 bpf, SCLK will have the same duty cycle as CLKOUT.  
See Internal Clock Generation section.

7. After powering up the CS4215, RESET should be held low for 50 ms to allow the voltage reference to settle.



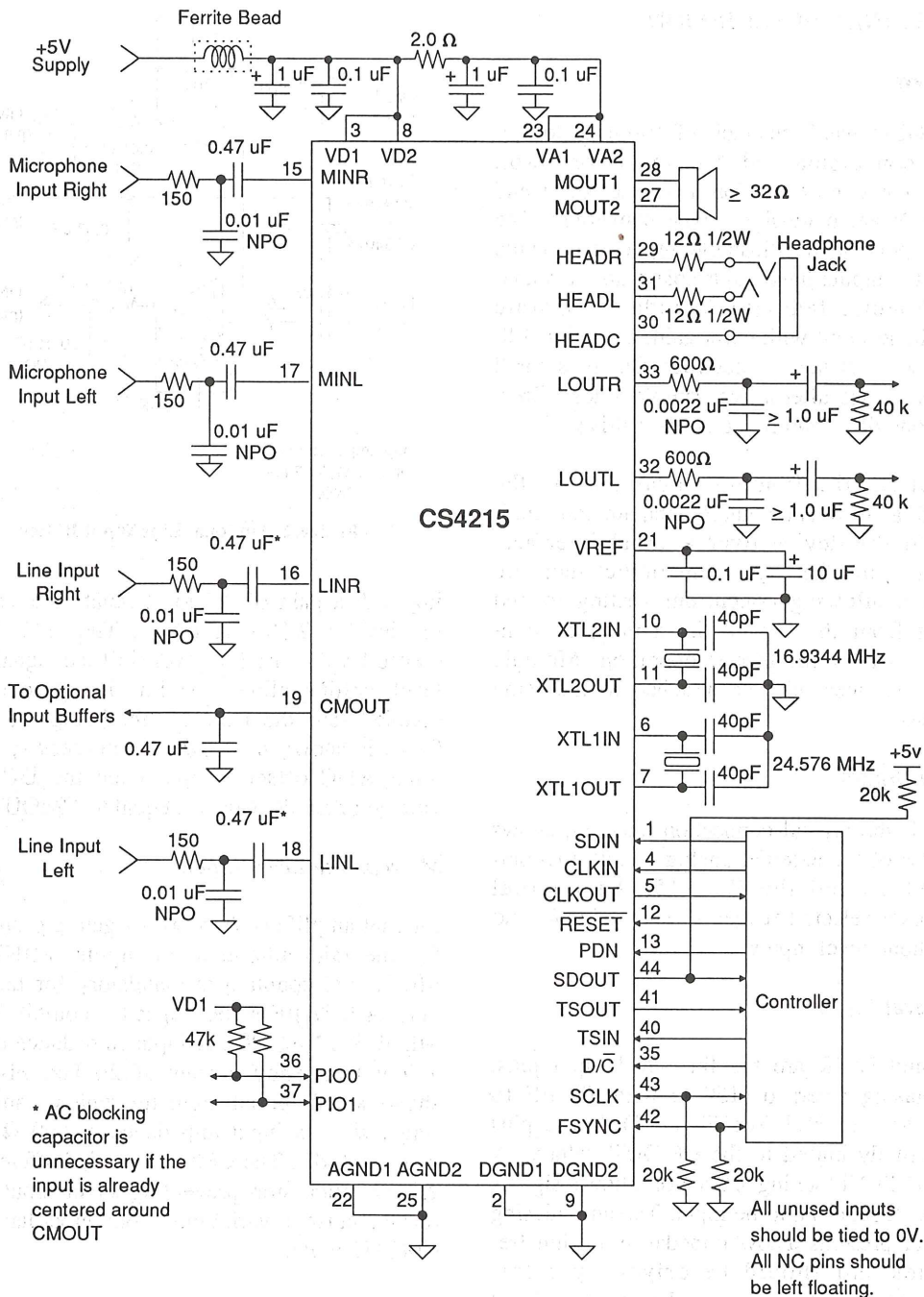
**ABSOLUTE MAXIMUM RATINGS** (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter	Symbol	Min	Max	Units	
Power Supplies:	Digital Analog	VD1,VD2 VA1,VA2	-0.3 -0.3	6.0 6.0	V V
Input Current	(Except Supply Pins)		-	±10.0	mA
Analog Input Voltage			-0.3	(VA1, VA2)+0.3	V
Digital Input Voltage			-0.3	(VD1, VD2)+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS** (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter	Symbol	Min	Typ	Max	Units	
Power Supplies:	Digital	VD1,VD2	4.75	5.0	5.25	V
	Analog	VA1,VA2	4.75	5.0	5.25	V
Operating Ambient Temperature	T <sub>A</sub>	0	25	70	°C	



## FUNCTIONAL DESCRIPTION

### Overview

The CS4215 has 2 channels of 16-bit analog-to-digital conversion and 2 channels of 16-bit digital-to-analog conversion. Both the ADCs and the DACs are delta-sigma type converters. The ADC inputs have adjustable input gain, while the DAC outputs have adjustable output attenuation. Special features include a separate microphone input with extra gain, an optional 8-bit  $\mu$ -law or A-law encoder/decoder, pins for 2 crystals to set alternative sample rates, direct headphone drive and mono speaker drive.

Control for the functions available on the CS4215, as well as the audio data, are communicated to the device over a serial interface. Separate pins for input and output data are provided, allowing concurrent writing to and reading from the device. Data must be continually written for proper operation. Multiple CS4215 devices may be attached to the same data lines.

### Analog Inputs

Figure 1, the typical connection diagram, shows examples of the external analog circuitry recommended around the CS4215. An internal multiplexer selects between line level inputs and microphone level inputs.

### Line Level Inputs

LINL and LINR are the line level input pins. Anti-aliasing filters of  $150\ \Omega$  with  $.01\ \mu\text{F}$  to ground are required (see Figure 1). These pins are internally biased to the CMOUT voltage. A  $0.47\ \mu\text{F}$  DC blocking capacitor allows signals centered around  $0\text{V}$  to be input. The anti-aliasing RC filter presents a low impedance at high frequencies and should be driven by a low impedance source. Figure 2 shows an optional dual op-amp buffer which combines level shift-

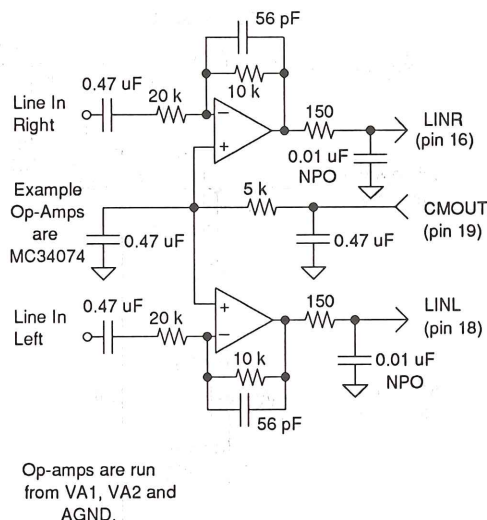


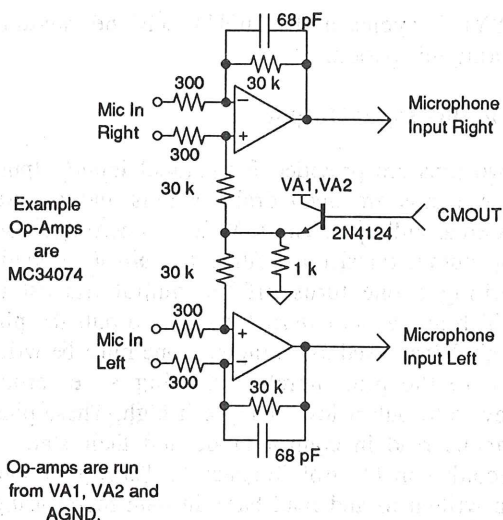
Figure 2. Optional Line Input Buffer

ing with a gain of 0.5 to attenuate the standard line level of  $2\text{ V}_{\text{rms}}$  to  $1\text{ V}_{\text{rms}}$ . The CMOUT reference level is used to level shift the signal. This level shifting allows the line inputs to be DC coupled into the CS4215, rendering the series  $0.47\ \mu\text{F}$ , shown in Figure 1, unnecessary. Minimum ADC offset results when the DC input voltage of LINR, LINL is equal to CMOUT.

### Microphone Level Inputs

Internal amplifiers with 20 dB gain are provided for the microphone level inputs, MINR and MINL. AC coupling is mandatory for these inputs. A  $0.47\ \mu\text{F}$  series capacitor combined with MINR & MINL  $20\text{ k}\Omega$  input impedance defines a low frequency corner of 20 Hz. Figure 3 shows a differential input microphone amplifier stage, with an input impedance of  $600\ \Omega$  and a gain of 40 dB. The CMOUT pin is buffered by a 2N4124 transistor, preventing small input signal related current variations from modulating the CMOUT voltage.





**Figure 3. Optional Microphone Input Buffer**

### Adjustable Input Gain

The signals from the microphone or the line inputs are routed to a programmable gain circuit which provides up to 22.5 dB of gain in 1.5 dB steps. Level changes only take effect on zero crossings to minimise audible artifacts, often referred to as "zipper noise". If there is no zero crossing, then the requested level change will occur after a timeout of 511 frames (10.6 ms at 48 kHz frame rate). There is a separate zero crossing detector for each channel.

### Analog Outputs

The analog output of the DACs is routed via an attenuator to a pair of line outputs, a pair of headphone outputs and a mono monitor speaker output.

### Output Level Attenuator

The DAC outputs are routed through an attenuator, which provides 0 dB to 94.5 dB of attenuation adjustable in steps of 1.5 dB. Level changes are implemented using both analog and digital attenuation techniques. Level changes

only take effect on zero crossings to minimize audible artifacts. If there is no zero crossing, then the requested level change will occur after a timeout of 511 frames (10.6 ms at 48 kHz frame rate). There is a separate zero crossing detector for each channel.

### Line Outputs

LOUTR and LOUTL output an analog signal, centered around CMOUT voltage. The minimum recommended load impedance is 8 k $\Omega$ . Figure 1 shows the recommended 1.0  $\mu$ F DC blocking capacitor with a 40 k $\Omega$  resistor to ground. When driving impedances greater than 10 k $\Omega$ , this provides a high pass corner of 20 Hz. These outputs may be muted.

### Headphone Outputs

HEADR and HEADL output an analog signal, centered around CMOUT voltage. The default headphone output level (OLB = 0) contains an optional 3 dB gain over the line outputs which allows reasonable listening levels, even with small amplitude digital sources. These outputs have increased current drive capability, with a minimum load impedance of 20  $\Omega$ . External 12  $\Omega$  series resistors reduce output level variations with different impedance headphones. The common return line from driving headphones should be connected to HEADC, which is biased up at CMOUT voltage. This removes the need for AC coupling, and also controls where the return currents flow. All three headphone output lines are short-circuit protected. These outputs may be muted.

### Speaker Output

MOUT1 and MOUT2 differentially drive a small loudspeaker, whose impedance should be greater than 32  $\Omega$ . The signal is a summed version of the right and left line output, tapped off prior to the mute function, but after the attenuator. The speaker output may be independently muted.

Some small speakers distort heavily when presented with low frequency energy. In this case, a high-pass filter would help eliminate the low frequency energy. This may be implemented with the CS4215 by AC coupling both speaker terminals with a resistor to ground on the speaker side of the DC blocking capacitors. The values selected would depend on the speaker chosen, but typical values would be 22  $\mu$ F for the capacitors, with the positive side connected to the codec, and 50 k $\Omega$  resistors. The resistors provide a bias point and have negligible effect when compared to the speaker impedance.

### ***Input Monitor Function***

To allow monitoring of the input audio signal, the output of the ADCs is routed through a monitor path attenuator, then digitally mixed into the input data for the DACs (see the front page block diagram). Changes in the input gain setting directly affect the monitor level. Changes in the output level setting will also directly affect the monitor output level. If full scale data from the ADCs is added to full scale digital data from the serial interface, then clipping will occur.

### ***Calibration***

Both output offset voltage and input offset error are minimized by an internal calibration cycle. At least one calibration cycle must be invoked after power up. A calibration cycle will occur immediately after leaving the reset state. A calibration cycle will also occur immediately after going from control mode to data mode (D/C going high). Some time must be allowed between powering up the CS4215, or exiting the power down state, and initiating a calibration cycle, to allow the voltage reference to settle. This is achieved by holding  $\overline{\text{RESET}}$  low for 50 ms after power up or exiting power down mode. The input offset error will be calibrated for whichever input channel is selected (microphone or line, using the IS bit) upon entering the data mode. Calibration takes 194

FSYNC cycles and SDOUT will be random during this period.

### ***Parallel Input/Output***

Two pins are provided for parallel input/output. These pins are open drain outputs and require external pull-up resistors. Writing a zero turns on the output transistor, pulling the pin to ground; writing a one turns off the output transistor, which allows an external resistor to pull the pin high. When used as an input, a one must be written to the pin, thereby allowing an external device to pull it low or leave it high. These pins can be read in control mode and their state is recorded in Control Register 5. These pins can be written to and read back in data mode using Data Register 7. Figure 4 shows the Parallel Input/Output timing.

### ***Clock Generation***

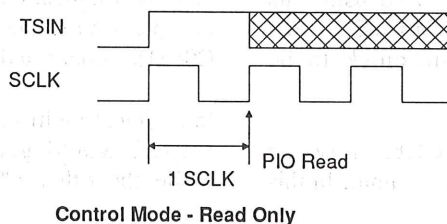
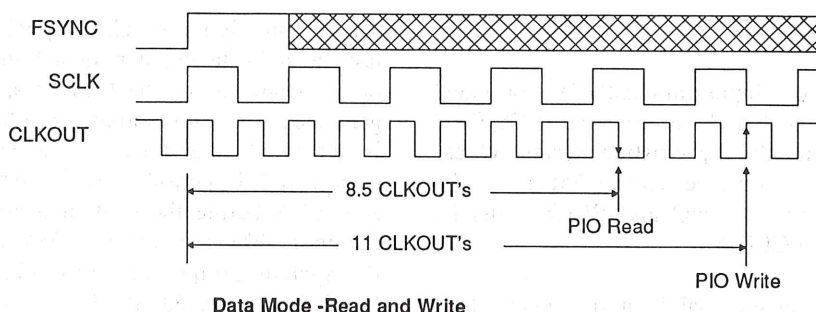
The master clock that operates the CS4215 may be generated using the on-chip crystal oscillators, or by using an external clock source. If the active clock source stops, then the CS4215 will enter a power down state to prevent overheating. In all modes SCLK & FSYNC must be synchronous to the selected master clock.

If the master clock source stops, the digital filters will power down after 5  $\mu$ s. If FSYNC stops, the digital filters will power down after approximately 1 FSYNC period. The CS4215 will not enter the total power down state.

### ***Internal Clock Generation***

Two external crystals may be attached to the XTL1IN, XTL1OUT, XTL2IN and XTL2OUT pins. Use of an external crystal requires additional 40 pF loading capacitors to digital ground (see Figure 1). XTAL1 oscillator is intended for use at 24.576 MHz and XTAL2 oscillator is intended for use at 16.9344 MHz. The gain of the internal inverter is slightly





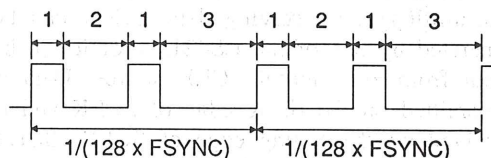
- Notes:
1. DATA MODE READ - The data is sent out via SDOUT on the next frame.
  2. CONTROL MODE READ - The data is sent out, via SDOUT, the same frame.
  3. DATA MODE READ, WRITE - are tied to the rising edge of FSYNC and CLKOUT. They are independent of SCLK.
  4. CONTROL MODE READ - The PIO pins are sampled by a rising edge of SCLK.

**Figure 4. PIO Pin Timing**

higher for XTAL1, ensuring proper operation at >24 MHz frequencies. The crystals should be parallel resonant, fundamental mode and designed for 20 pF loading (equivalent to a 40 pF capacitor on each leg). If XTAL1 or XTAL2 is not selected as the master clock, that particular crystal oscillator is powered down to minimize interference. An example crystal supplier is CAL Crystal, telephone number (714) 991-1580.

An internally generated clock which is 256 times the sample rate (FSYNC rate) is output (CLKOUT) for potential use with an external AES/EBU transmitter, or another CS4215. No glitch occurs on CLKOUT when selecting alternate clock sources. Also, CLKOUT will exhibit a minimum of 1 and a maximum of 2 rising edges after D/C goes low and will then stop in

the low state. This is true if one of the crystal oscillators is being used, or if either CLKIN or SCLK is the master clock source and is continuous. The duty cycle of CLKOUT is 50% if the master clock is one of the crystal oscillators and the DFR bits are 0, 1, 2, 6 or 7. If the DFR bits are 3 or 5, the duty cycle is 33% (high time). If the DFR bits are 4 then CLKOUT has the timing shown in Figure 5 if the master clock is SCLK or CLKIN, the duty cycle of CLKOUT will be the same as the master clock source.



**Figure 5. CLKOUT duty cycle using the on-chip crystal oscillator when DFR = 4 (typically FSYNC = 37.8 kHz)**

## External Clock

An external clock input pin (CLKIN) is provided for potential use with an external AES/EBU receiver, or an already existing system clock. The input clock must be exactly 256 times the sample rate, i.e. FSYNC and SCLK must be synchronous to CLKIN.

Alternatively, an external high frequency clock may be driven into XTL1IN or XTL2IN. The correct clock source must be selected using the MCK bits. Manipulating DFR bits will allow various divide ratios from the clock to be selected.

As a third alternative, SCLK may be programmed to be the master clock input. In this case, it must be 256 times Fs.

## Serial Interface

The serial interface of the CS4215 is used to transfer digital audio data and control data into and out of the device. Multiple CS4215 devices may share the same data lines. DSP's supported include the Motorola 56001 in network mode and a subset of the 'CHI' bus from AT&T/Intel.

## Serial Interface Signals

Figure 6 shows an example of two CS4215 devices connected to a common controller. The Serial Data Out (SDOUT) and Serial Data In (SDIN) lines are time division multiplexed between the CS4215's.

The serial interface clock, SCLK, is used for transmitting and receiving data. SCLK can be generated by one of the CS4215's, or it can be input from an external SCLK source. Data is transmitted on the rising edge of SCLK and is received on the falling edge of SCLK. SCLK frequency is always equal to the bit rate.

The Frame Synchronizing signal (FSYNC) is used to indicate the start of a frame. It may be output from one of the CS4215's, or it may be generated from an external controller. If FSYNC is generated externally, it must be high for at least 1 SCLK period, and it must fall at least 2 SCLK's before the start of a new frame (see Figure 7). The frequency of FSYNC is equal to the system sample rate (see Figure 7). Each CS4215 requires 64 SCLK's to transfer all the data. If FSYNC is an output from the CS4215, then the frequency can be set to 64, 128, or 256 bits per frame, thereby allowing for 1, 2 or 4 CS4215's connected to the same bus.

In a typical multi-part scenario, one CS4215 (the master) would generate FSYNC and SCLK, while the other CS4215's (the slaves) would

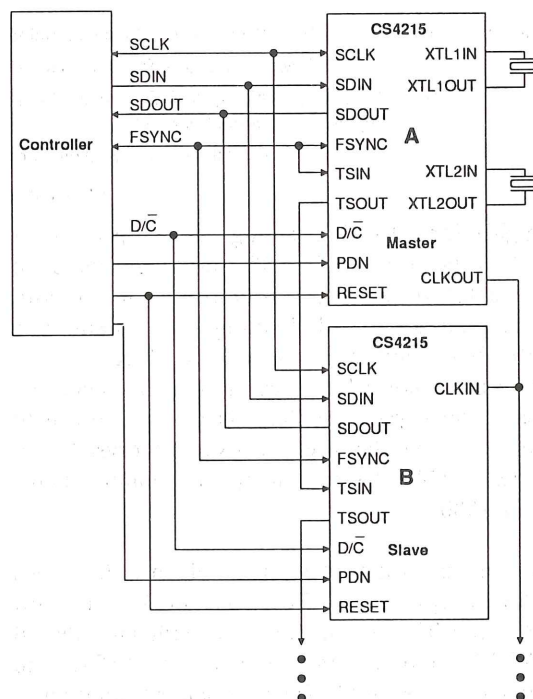


Figure 6. Multiple CS4215's



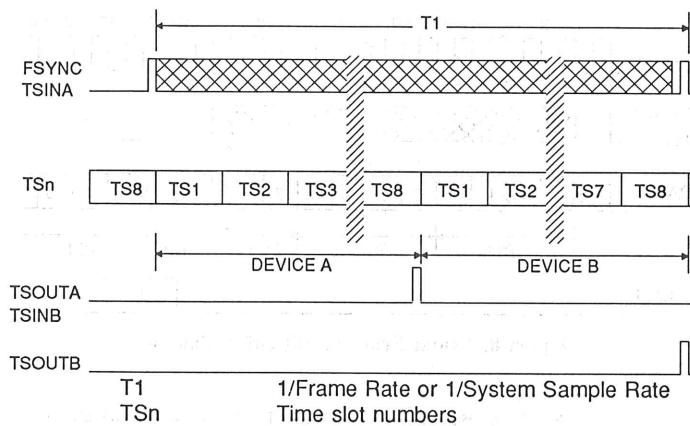


Figure 7 Serial Interface Timing for 2 CS4215's

receive FSYNC and SCLK. The CLKOUT of the master would be connected to the CLKIN of each slave device as shown in Figure 6. Then, the master device would be programmed for the desired sample frequency (assuming one of the crystals is selected as the clock source), the number of bits per frame, and for SCLK and FSYNC to be outputs. The slave devices would be programmed to use CLKIN as the clock source, the same number of bits per frame, and for SCLK and FSYNC to be inputs. Since CLKOUT is always 256 times the sample frequency and scales with the selected sample frequency on the master, the slave devices will automatically scale with changes in the master codec's sample frequency.

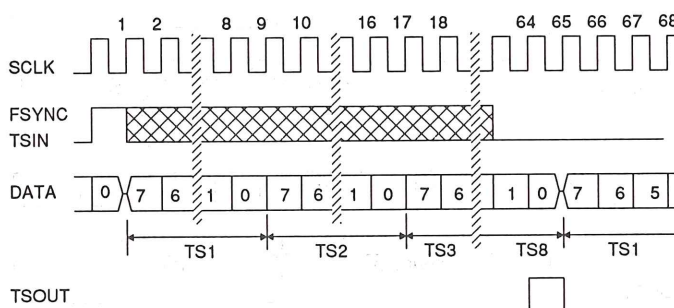
CS4215's are timed onto the bus using the Time Slot Out (TSOUT) and Time Slot In (TSIN) signals. TSOUT is an output signal that is one SCLK bit time long, and indicates that the CS4215 is about to release the bus. TSIN is an input signal that informs the CS4215 that the next time slot is available for it to use. The first device in the chain uses FSYNC as its TSIN signal. All subsequent devices use the TSOUT of the previous device as its TSIN input. TSIN must be high for at least 1 SCLK period and fall at least 2 SCLK's before start of a new frame.

### Serial Interface Operation

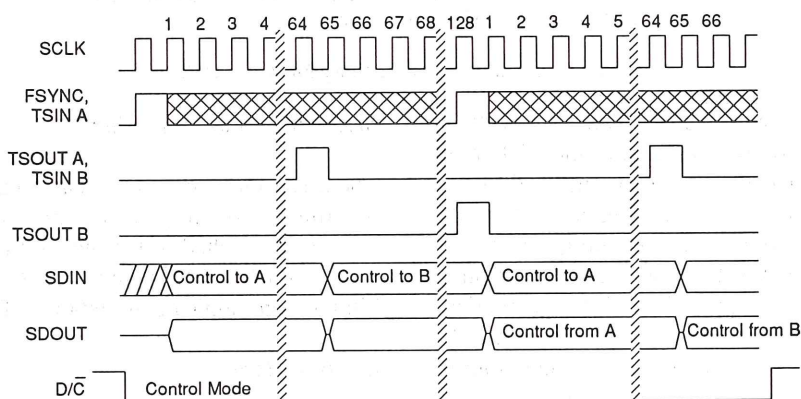
The serial interface format has a variable number of time slots, depending on the number of CS4215's attached to the bus. All time slots have 8 bits. Each CS4215 requires 8 time slots (64 bits) to communicate all data (see Figure 8).

### Control Mode

The Control Mode is used to set up the CS4215 for subsequent operation in Data Mode by loading the internal control registers. Control mode is asserted by bringing D/C low. If D/C is low during power up, then the CS4215 will enter control mode immediately. The SCLK and FSYNC pins are tri-stated, and the CS4215 will receive SCLK and FSYNC from an external source. If the CS4215 is in master mode (SCLK and FSYNC are outputs) and D/C is brought low, then SCLK & FSYNC will continue to be driven for a minimum of 4 and a maximum of 12 SCLK's, if the ITS bit = 0. If ITS is 1, SCLK and FSYNC will three-state immediately after D/C goes low. When the ITS bit is set to 0, extreme care must be used to guarantee that the master clock source exists when the CS4215 is programmed to generate SCLK and FSYNC. If the master clock selected does not exist and the CS4215 is programmed as the serial port master,



**Figure 8. Frame Sync and Bit Offset Timing**



**Figure 9. Control Mode Timing for 2 CS4215's**

control mode will be blocked since the codec cannot generate the extra SCLKs needed when entering control mode. Therefore, the CS4215 cannot be reprogrammed to correct the error without giving the codec a reset command, via the reset pin, which places the control registers in their default state. The values in the control registers for control of the serial ports are ignored in control mode. The data received on SDIN is stored into the control registers which have addresses matching their time slots. The data in the registers is transmitted on SDOUT with the time slot equal to the register number (see Figure 9).

The steps involved when going from data mode to control mode and back are as follows:

- 1) Lower the output level to maximum attenuation.
- 2) Mute the speaker output.
- 3) Assert D/C low.
- 4) If the CS4215 was in master mode and the ITS bit = 0, wait at least 12 SCLK periods to allow SCLK and FSYNC to three-state.
- 5) Set the external controller to drive SCLK and FSYNC into the CS4215.
- 6) Repeatedly send control information to the CS4215's, with the CLB bit low.
- 7) Read back and verify the control information from the CS4215's. Mask off reserved bits. Wait for the CLB bit to go low.
- 8) Set the CLB bit high and send at least two more frames. This will cause the CS4215's to ignore any further activity on the bus. Also, the SDOUT pin will be held in the high impedance state after transmitting 1 frame with CLB high.
- 9) If the CS4215 is programmed to be the master, then set the external controller to receive SCLK and FSYNC from CS4215.
- 10) Set up new audio data to be transmitted to the CS4215's.
- 11) The D/C line is then brought high, sending the CS4215 into data mode. The CS4215 will execute an offset calibration cycle.
- 12) Transmit/receive audio data.

### Control Formats

The CS4215 control registers have the functions and time slot assignments shown in Table 1. The register address is the time slot number when D/C is 0. Reserved bits should be written as 0 and could be read back as 0 or 1. When comparing data read back, reserved bits should be masked. The SDOUT pin goes into a high-impedance state prior to Time Slot 1 and after Time Slot 8.

Time slot	Description
1	Status
2	Data Format
3	Serial Port Control
4	Test
5	Parallel Port
6	RESERVED
7	Revision
8	RESERVED

Table 1. Control Registers

### Control Time Slot 1, Status Register

D7	D6	D5	D4	D3	D2	D1	D0
RESERVED				OLB	CLB	RESERVED	

- CLB** Control Latch Bit. This bit is controlled to ensure proper transition between control and data mode.
- OLB** Output Level Bit.
- 0 - Line full scale outputs are 2.8 V<sub>pp</sub> (1 V<sub>rms</sub>). Headphone full scale output is 4.0 V<sub>pp</sub>. Speaker full scale output is 8.0 V<sub>pp</sub>.
  - 1 - Line and Headphone full scale outputs are 2.0 V<sub>pp</sub>. Speaker full scale output is 4.0 V<sub>pp</sub>.
- RESERVED** These bits are reserved for future use.

### Control Time Slot 2, Data Format Register

D7	D6	D5	D4	D3	D2	D1	D0
RESERVED		DFR2	DFR1	DFR0	ST	DF1	DF0

- DF1, DF0** Data format selection.
- 0 - 16 bit linear
  - 1 - 8 bit  $\mu$ -law
  - 2 - 8 bit A-law
  - 3 - Reserved
- ST** Stereo bit.
- 0 - Mono mode
  - 1 - Stereo mode
- DFR2-DFR0** Data conversion frequency selection
- |                  |            |
|------------------|------------|
| XTAL1            | XTAL2      |
| Crystal Used     |            |
| 0 - 8 kHz        | 16.9344MHz |
| 1 - 16 kHz       | 5.5125 kHz |
| 2 - 27.42857 kHz | 11.025 kHz |
| 3 - 32 kHz       | 18.9 kHz   |
| 4 - NA           | 22.05 kHz  |
| 5 - NA           | 37.8 kHz   |
| 6 - 48 kHz       | 44.1 kHz   |
| 7 - 9.6 kHz      | 33.075 kHz |
|                  | 6.615 kHz  |

DFR bits do not apply to CLKIN, which is always at 256Fs.

### Control Time Slot 3, Serial Port Control Register

D7	D6	D5	D4	D3	D2	D1	D0
ITS	RSRV	MCK1	MCK0	BSEL1	BSEL0	XCLK	XEN

- XEN** Transmitter enable
- 0 - Enable the serial data output.
  - 1 - Disable (high-impedance state) serial data output.
- XCLK** Transmit clock
- 0 - Receive SCLK and FSYNC from external source.
  - 1 - Generate SCLK and FSYNC.
- BSEL1, BSEL0** Select bit rate
- 0 - 64 bits per frame.
  - 1 - 128 bits per frame.
  - 2 - 256 bits per frame.
  - 3 - Reserved
- MCK1, MCK0** Clock Source Select
- 0 - SCLK is master clock, 256 bits per frame. BSEL must be set to 2, and XCLK must be set to 0.
  - 1 - XTAL1, 24.576 MHz, is clock source.
  - 2 - XTAL2, 16.9344 MHz, is clock source.
  - 3 - CLKIN is clock source, and must be 256 Fs.
- RSRV** Reserved Bit
- ITS** Immediate Three-State Bit.
- 0 - FSYNC and SCLK three-state up to 12 clocks after D/C goes low.
  - 1 - FSYNC and SCLK three-state immediately after D/C goes low.



### Control Time Slot 4, Test Register

D7	D6	D5	D4	D3	D2	D1	D0
TEST						ENL	DAD

DAD	Loopback mode 0 - Digital-Digital loopback 1 - Digital-Analog-Digital loopback
ENL	Enable loopback testing 0 - disabled 1 - enabled
TEST	The TEST bits must be written as zero, otherwise special factory test modes may be invoked.

### Control Time Slot 5, Parallel Port Register

D7	D6	D5	D4	D3	D2	D1	D0
PIO1	PIO0	RESERVED					

The parallel port register is used to read and write the two open-drain input/output pins. The outputs are all set to 1 on RESET. PIO bits are read only in control mode. Note that, since PIO signals are open drain signals, an external device may drive them low even when they have been programmed as highs. Therefore, the value read back may differ from the value written. In the data mode, ( $D/\bar{C}=1$ ), this register can be read and written to through the serial port as part of the Input Settings Registers.

### Control Time Slot 7, Revision Level of the CS4215

D7	D6	D5	D4	D3	D2	D1	D0
RESERVED				RV3	RV2	RV1	RV0

RV0 - RV3 Revision level of the CS4215.  
1st Revision Samples = 0000  
2nd Revision Samples = 0001

This data sheet is for Revision Level 0001 silicon.

### Data Mode

The data mode is used during conversions to pass digital data between the CS4215 and external devices. The frame sync rate is equal to the value of the conversion frequency set by the DFR2-DFR0 bits of the Data Format register. Each frame has either 64, 128, or 256 bit times depending on the BSEL bits in the Serial Control register. Control of gain, attenuation, input selection and output muting are embedded in the data stream.

### Data Formats

All time slots contain 8 bits. The MSB, D7, of the data is transmitted/received first. The CS4215 data registers have the functions and time slot assignments shown in Table 2. The register address is the time slot number when  $D/\bar{C}$  is 1. The SDOUT pin goes into a high-impedance state prior to Time Slot 1 and after Time Slot 8 (see Figure 10).

Time slot	Description
1	Left Audio MS8 bits
2	Left Audio LS8 bits
3	Right Audio MS8 bits
4	Right Audio LS8 bits
5	Output Setting
6	Output Setting
7	Input Setting
8	Input Setting

Table 2. Data Registers

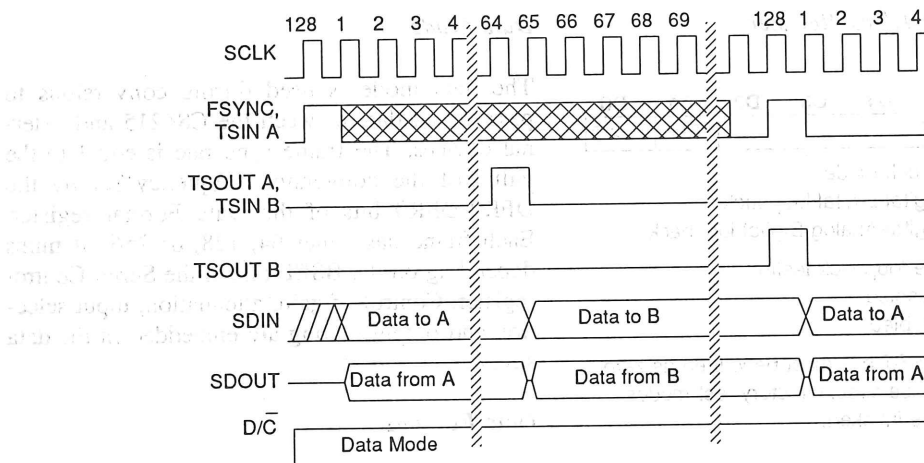


Figure 10. Data Mode Timing for 2 CS4215's

### Data Time Slot 1&2, Left Channel Audio Data

Time slot 1 and 2 contain audio data for the left channel. MSB first, 2's complement coding is used. In mono modes, only this left channel data is used, however both the right and left output DAC's are driven. In 8-bit modes, only time slot 1 is used for the data.

### Data Time Slot 3&4, Right Channel Audio Data

Time slot 3 and 4 contains audio data for the right channel. MSB first, 2's complement coding is used. In mono modes, the right ADC outputs zero and the right DAC uses the left digital data. In 8-bit modes, only time slot 3 is used for the data.

### Data Time Slot 5, Output Setting

D7	D6	D5	D4	D3	D2	D1	D0
HE	LE	LO5	LO4	LO3	LO2	LO1	LO0

LO5 - LO0 Output attenuation setting for the left channel. LO5 is the MSB. LO0 represents 1.5 dB. 0 = no attenuation.

HE Headphone output enable control.  
0 - Headphone output off.  
1 - Headphone output on.

LE Line output enable control  
0 - Analog line output off.  
1 - Analog line output on.

### Data Time Slot 6, Output Setting

D7	D6	D5	D4	D3	D2	D1	D0
0	SE	RO5	RO4	RO3	RO2	RO1	RO0

RO5 - RO0 Output attenuation setting for the right channel. RO5 is the MSB. RO0 represents 1.5 dB. 0 = no attenuation. Not used in mono modes.

SE Speaker Enable control bit.  
0 - speaker off  
1 - speaker on

### Data Time Slot 7, Input Setting

D7	D6	D5	D4	D3	D2	D1	D0
PIO1	PIO0	OVR	IS	LG3	LG2	LG1	LG0
LG3 - LG0		Input gain for left channel. LG3 is the MSB. LG0 represents 1.5 dB. Full gain is 22.5 dB. 0 = no gain.					
IS		Input Selection 0 - Line level input. 1 - Microphone level input.					
OVR		Overrange. When read as 1, this bit indicates that an input over-range condition has occurred. The bit remains set until cleared by writing 0 into the register. Writing a 1 enables the over-range detection. The bit will remain 0 until an over-range occurs. Serial port clear has priority over internal setting.					
PIO1-PIO0		Parallel input/output bits.					

### Reset

**RESET** going low causes all the internal control registers to be set to the states indicated in Table 3. **RESET** must be brought low and high at least once after power up. Reset returning high causes the CS4215 to execute an offset calibration cycle. Reset returning high should occur at least 50 ms after the power supply has stabilized.

LO5-LO0 = 63	MCK-MCK0 = 0
RO5-RO = 63	LE = 0
RG3-RG0 = 0	IS = 0
OVR = 0	DF1-DF0 = 1
DFR2-DFR0 = 0	XCLK = 0
BSEL1 - BSEL0 = 2	ADL = 0
ENL = 0	DCB = 1
HE = 0	OLB = 0
LG3-LG0 = 0	MA = 16
PIO1-PIO0 = 3	SE = 0
ST = 0	ITS = 0
XEN = 1	

Table 3. Control Register Status After Reset

### Data Time Slot 8, Input Setting

D7	D6	D5	D4	D3	D2	D1	D0
MA3	MA2	MA1	MA0	RG3	RG2	RG1	RG0
RG3 - RG0				Input gain for the right channel. RG3 is the MSB. RG0 represents 1.5 dB or less. Full gain is at least 22.5 dB. Not used in mono modes.			
MA3 - MA0				Monitor path attenuation. MA0 represents 6 dB. MA3 is the MSB. 0 = no attenuation. 15 = mute monitor path.			

### Power Down Mode

Bringing the PDN pin high puts the CS4215 into the power down mode. In this mode HEADC and CMOUT will not supply current. Power down will change all the control registers to the reset state shown in Table 3. In the power down mode, the TSOUT pin will follow the TSIN state with less than 10 ns delay.

After returning to normal operation from power down, an offset calibration cycle must be executed. Either bringing **RESET** low then high, or updating the control registers, will cause an offset calibration cycle. In either case, a delay of 50 ms must occur after PDN goes low before executing the offset calibration. This allows the internal voltage reference time to settle.

Figure 11 summarizes all the time slot bit allocations for the 4 data modes and for control mode.





### Loopback Test Modes

The ability to run diagnostic self-tests is crucial to today's complex computers. The CS4215 contains three loopback modes that may be used to test the codec. Two of the loopback test modes are designed to allow the host to perform a self-test on the CS4215. The third mode allows laboratory testing using external equipment.

#### Host Self-Test Loopback Modes

Since the CS4215 is a mixed-signal device, it is equipped with an internal register that will enable the host to perform a two-tiered test on power-up or as needed. The loopback test is enabled by setting the Enable Loopback bit, ENL, in control register 4. The first tier of loopback is a digital-digital loopback, DD, which is selected by clearing the DAD bit in control register 4. DD loopback checks the interface between the host and the CS4215 by taking the data on SDIN and looping it back onto SDOUT, with the data on SDOUT being one frame delayed from the data on SDIN. The host can verify that the data received is exactly the same as the data sent, thereby indicating the interface between the two devices and the digital interface on the CS4215 are operating properly. The output DAC's are functional in DD loopback. Now that the interface has been verified, the rest of the CS4215 can be tested using the second tier of loopback.

The second tier of loopback is a digital-analog-digital loopback, DAD, which is selected by setting the DAD bit in control register 4. DAD loopback checks the analog section of the CS4215 by connecting the right and left analog outputs, after the output attenuator, to the analog inputs of the gain stage. This allows testing of most of the CS4215 from the host by sending a known digital signal to the DACs and monitoring the digital signal from the ADCs. During DAD loopback, the monitor attenuator must be set at maximum (full mute), and the

analog outputs may be individually muted. The analog inputs are disconnected internally. The flow of test data for both DD and DAD loopback modes is illustrated in the top portion of Figure 12.

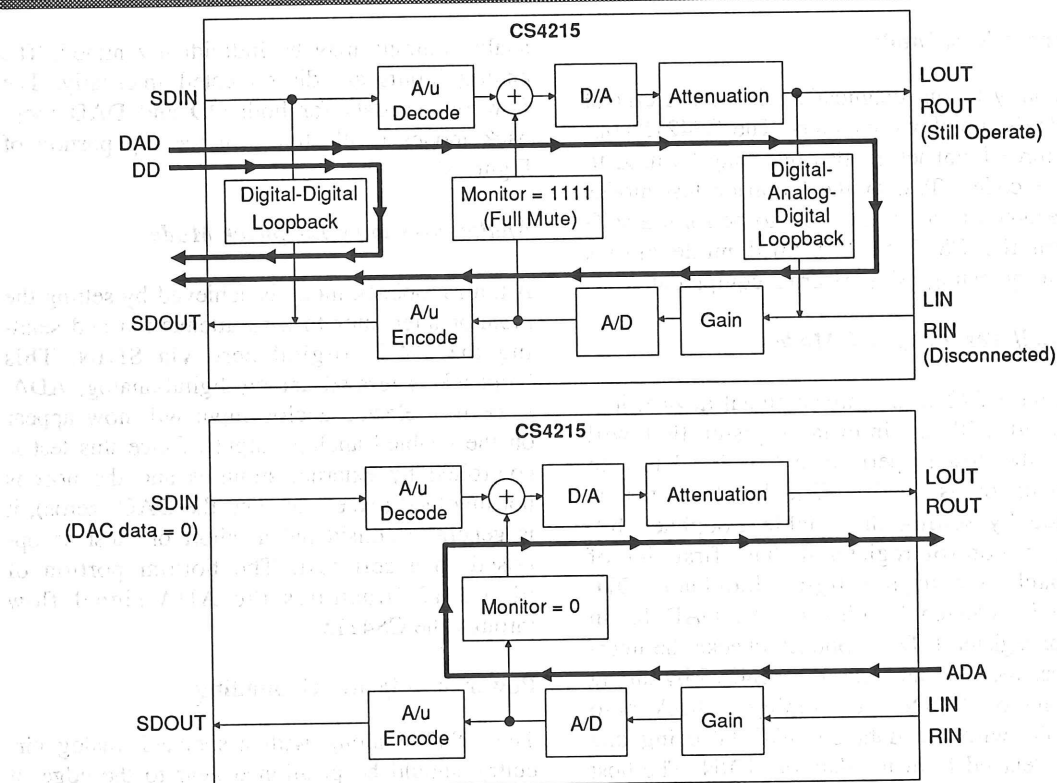
#### Analog-to-Analog Loopback Mode

A third loopback mode is achieved by setting the monitor attenuator to zero attenuation and sending the DACs digital zero via SDIN. This loopback is termed analog-digital-analog, ADA, since the selected analog input will now appear on the enabled analog outputs. Since this test is controlled by external stimulus and the host is not involved (except to send the DACs zeros), it is generally considered a laboratory test as opposed to a self test. The bottom portion of Figure 12 illustrates the ADA signal flow through the CS4215.

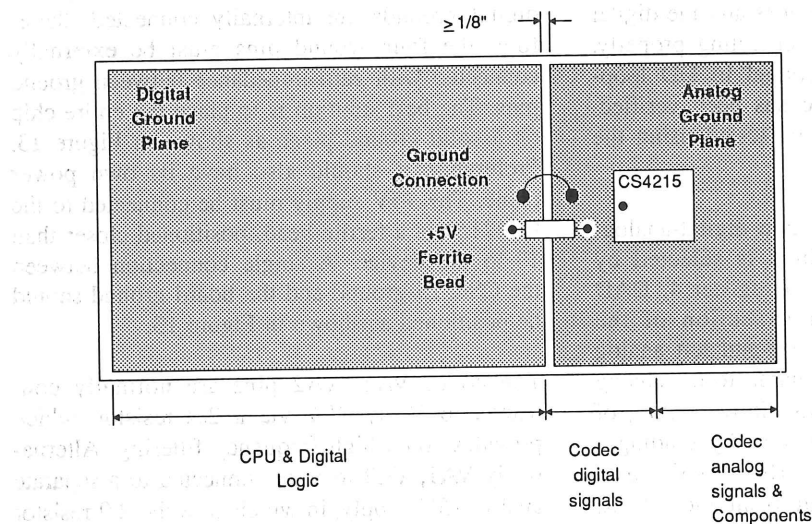
#### Power Supply and Grounding

The CS4215 along with associated analog circuitry, should be positioned near to the edge of the circuit board, and have its own, separate, ground plane. On the CS4215, the analog and digital grounds are internally connected; therefore, the four ground pins must be externally connected with zero impedance between ground pins. The best solution is to place the entire chip on a solid ground plane as shown in Figure 13. Preferably, it should also have its own power plane. The +5V supply must be connected to the CS4215 via a ferrite bead, positioned closer than 1" to the device. A single connection between the CS4215 ground and the board ground should be positioned as shown in Figure 13.

The codec VA1, VA2 pins are normally connected to VD1, VD2 via a 2Ω resistor, which provides some high frequency filtering. Alternatively VA1, VA2 may be connected to a separate analog +5V supply, in which case the 2.0 resistor is removed (see Figure 1).



**Figure 12. DD, DAD & ADA Loopback Paths**



Note that the CS4215 is oriented with its digital pins towards the digital end of the board.

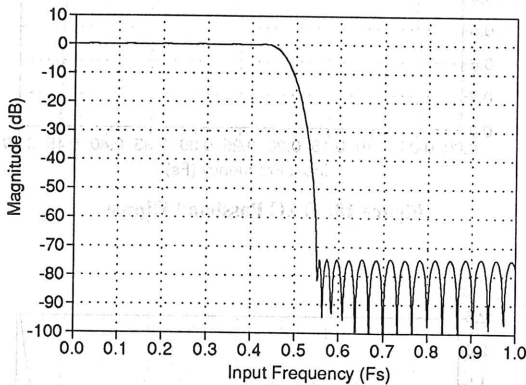
**Figure 13. Suggested Layout Guideline**

## ADC and DAC Filter Response Plots

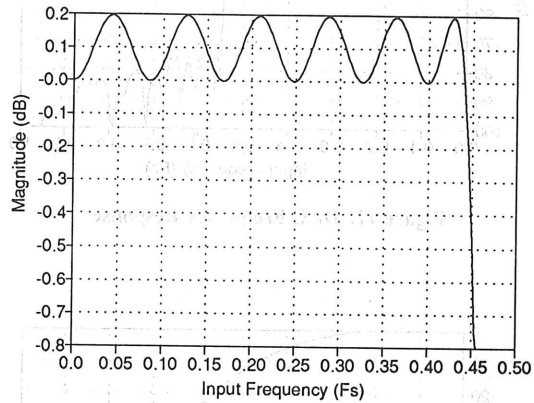
Figures 14 through 19 show the overall frequency response, passband ripple and transition band

for the CS4215 ADCs and DACs. Figure 20 shows the DACs' deviation from linear phase.

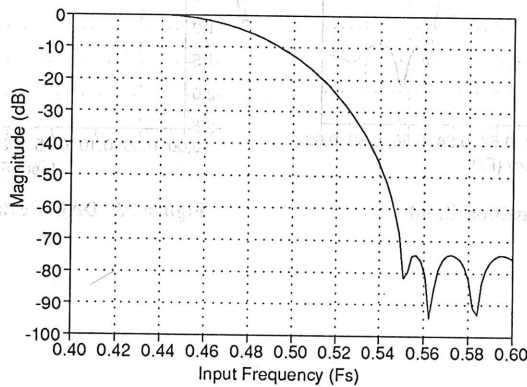
2



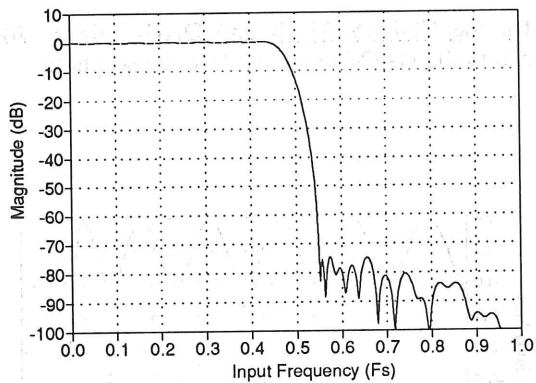
**Figure 14. ADC Frequency Response**



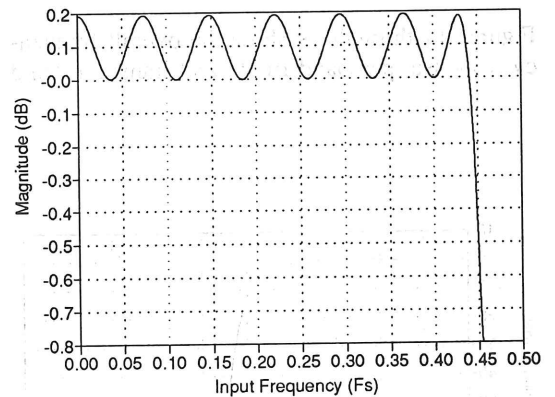
**Figure 15. ADC Passband Ripple**



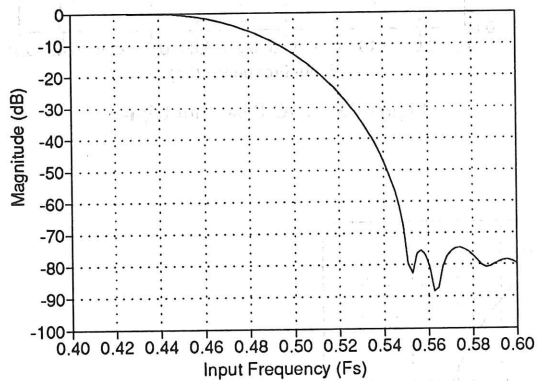
**Figure 16. ADC Transition Band**



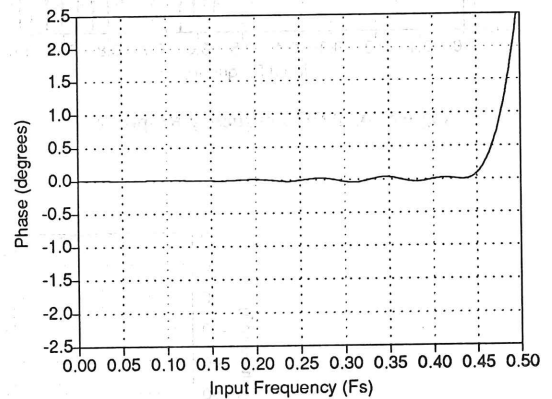
**Figure 17. DAC Frequency Response**



**Figure 18. DAC Passband Ripple**



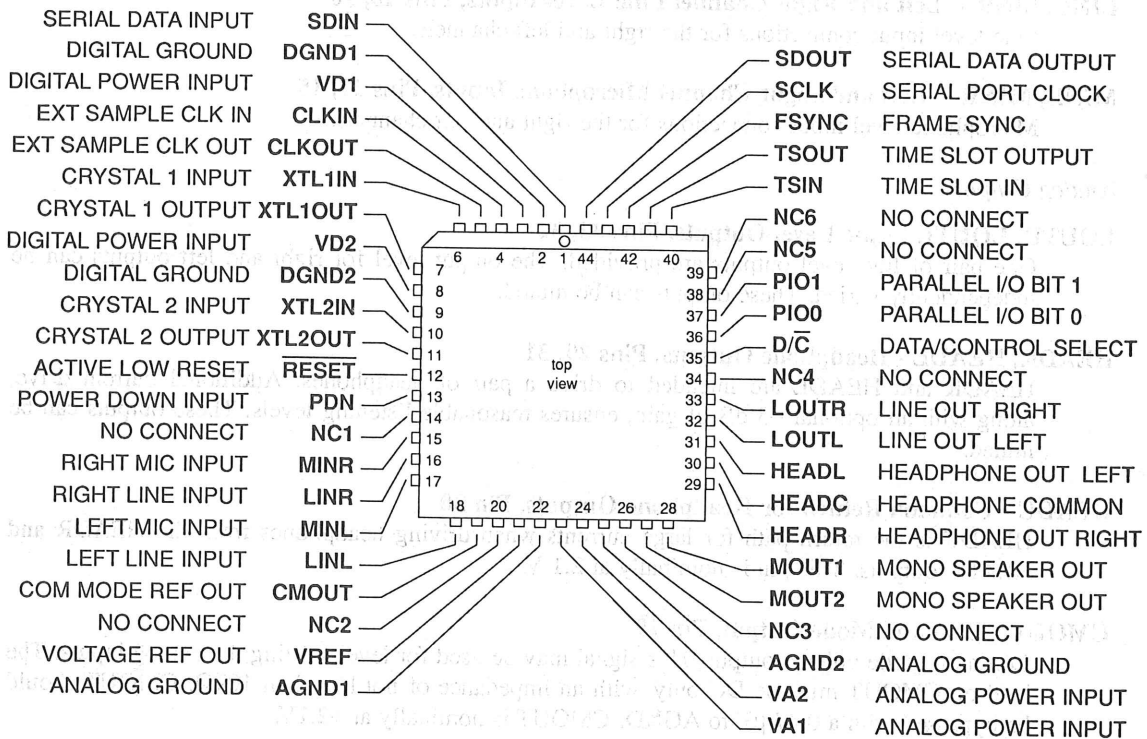
**Figure 19. DAC Transition Band**



**Figure 20. DAC Deviation from Linear Phase**



### PIN DESCRIPTIONS



2

#### Power Supply

**VA1, VA2 - Analog Power Input, Pins 23, 24**  
+5 V analog supply.

**AGND1, AGND2 - Analog Ground, Pins 22, 25**  
Analog ground. Must be connected to DGND1, DGND2 with zero impedance.

**VD1, VD2 - Digital Power Input, Pins 3, 8**  
+5 V digital supply.

**DGND1, DGND2 - Digital Ground, Pin 2, 9**  
Digital ground. Must be connected to AGND1, AGND2 with zero impedance.

### *Analog Inputs*

#### **LINL, LINR - Left and Right Channel Line Level Inputs, Pins 18, 16**

Line level input connections for the right and left channels.

#### **MINL, MINR - Left and Right Channel Microphone Inputs, Pins 17, 15**

Microphone level input connections for the right and left channels.

### *Analog Outputs*

#### **LOUTR, LOUTL - Line Level Outputs, Pins 33, 32**

One pair of line level outputs are provided. The output level for right and left outputs can be independently varied. These outputs can be muted.

#### **HEADR, HEADL - Headphone Outputs, Pins 29, 31**

HEADR and HEADL are intended to drive a pair of headphones. Additional current drive, along with an optional +3 dB of gain, ensures reasonable listening levels. These outputs can be muted.

#### **HEADC - Common Return for Headphone Outputs, Pin 30**

HEADC is the return path for large currents when driving headphones from the HEADR and HEADL outputs. This pin is nominally at 2.1 V.

#### **CMOUT - Common Mode Output, Pin 19**

Common mode voltage output. This signal may be used for level shifting the analog inputs. The load on CMOUT must be DC only, with an impedance of not less than 10k $\Omega$ . CMOUT should be bypassed with a 0.47  $\mu$ F to AGND. CMOUT is nominally at +2.1V.

#### **MOUT1, MOUT2 - Mono Speaker Outputs, Pins 28, 27**

Mono external loudspeaker differential output connections. The loudspeaker output is a mix of left and right line outputs. Independent muting of the speaker is provided. MOUT1 and MOUT2 output voltage is nominally at 2.1 V with no signal.

#### **VREF - Voltage Reference Output, Pin 21**

The on-chip generated ADC/DAC reference voltage is brought out to this pin for decoupling purposes. This output must be bypassed with a 10  $\mu$ F capacitor in parallel with a 0.1  $\mu$ F capacitor to the adjacent AGND1 pin. No other external load may be connected to this output.

### *Digital Interface Signals*

#### **SDIN - Serial Data Input, Pin 1**

Audio data for the DACs and control information for all functions is presented to the CS4215 on this pin.

#### **SDOUT - Serial Data Output, Pin 44**

Audio data from the ADCs and status information concerning all functions is written out by the CS4215 onto this pin.

**SCLK - Serial Port Clock, Pin 43**

SCLK causes the data on SDOUT to be updated. SCLK latches the data on SDIN into the CS4215. The SCLK signal can be generated off-chip, and input into the CS4215. Alternatively, the CS4215 can generate and output SCLK in data mode.

**FSYNC - Frame Sync Signal, Pin 42**

The Frame Synchronising Signal is sampled by SCLK, with a rising edge indicating a new frame is about to start. FSYNC frequency is always the system sample rate. Each frame may have 64, 128 or 256 data bits, allowing for 1, 2 or 4 CS4215's connected to the same bus. FSYNC may be input to the CS4215, or may be generated and output by the CS4215 in data mode. When FSYNC is an input, it must be high for at least 1 SCLK period. FSYNC can stay high for the rest of the frame, but must return low at least 1 SCLK before the next frame starts.

**TSIN - Time Slot Input, Pin 40**

TSIN high for at least 1 SCLK cycle indicates to the CS4215 that the next time slot is allocated for it to use. TSIN is normally connected to the TSOUT pin of the previous device in the chain. TSIN should be connected to FSYNC for the 1st CS4215 in the chain.

**TSOUT - Time Slot Output, Pin 41**

TSOUT goes high for 1 SCLK cycle, indicating that the CS4215 is about to release the data bus. Normally connected to the TSIN pin on the next device in the chain.

**D/C - Data/Control Select Input, Pin 35**

When D/C is low, the information on SDIN and SDOUT is control information. When D/C is high, the information on SDIN and SDOUT is data information.

**PDN - Power Down Input, Pin 13**

When high, the PDN pin puts the CS4215 into the power down mode. In this mode HEADC and, CMOUT will not supply current. Power down causes all the control registers to change to the default reset state. In the power down mode, the TSOUT pin remains active, and follows TSIN delayed by less than 10 ns.

**RESET - Active Low Reset Input, Pin 12**

Upon reset, the values of the control information (when D/C = 0) will be initialized to the values given in the Reset Description section of this data sheet.

***Clock and Crystal Pins*****XTL1IN, XTL1OUT, XTL2IN, XTL2OUT - Crystals 1 and 2 Inputs and Outputs, Pins 6, 7, 10, 11**

Input and output connections for crystals 1 and 2. One of these oscillators may provide the master clock to run the CS4215.

**CLKIN - External Clock Input, Pin 4**

External clock input optionally used to clock the CS4215. The CLKIN frequency must be 256 times the system sample rate (FSYNC frequency).

**CLKOUT - Master Clock Output, Pin 5**

Master clock output, whose frequency is always 256 X the system sample rate (FSYNC frequency). CLKOUT is active only in data mode and is low during control mode.

**Miscellaneous Pins****NC1, NC2, NC3, NC4, NC5, NC6 - No Connect, Pins 14, 20, 26, 34, 38, 39**

These pins should be left floating.

**PIO0, PIO1 - Parallel Input/Output, Pins 36 and 37**

These pins are provided as general purpose digital parallel input/output and have open drain outputs. An external pull-up resistor is required. They can be read in control mode, and read and written to in data mode.



## PARAMETER DEFINITIONS

2

### Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

### Differential Nonlinearity

The worst case deviation from the ideal codewidth. Units in LSB.

### Dynamic Range

The  $S/(N+D)$  with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal renders harmonic distortion components of the noise insignificant compared to the noise. Units in dB.

### Signal-to-(Noise + Distortion)

$S/(N+D)$  is the ratio of the rms value of the input signal to the rms sum of all other spectral components within the measurement bandwidth (10 Hz to 20 kHz). Units in dB.

### Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

### Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

### Frequency Response

Worst case variation in output signal level versus frequency over 10 Hz to 20 kHz. Units in dB.

### Offset Error

For the ADCs, the deviation in LSB's of the output from mid-scale with the selected input at CMOUT. For the DAC's, the deviation of the output from CMOUT with mid-scale input code. Units in volts.

**APPENDIX A**

This data sheet describes version 1 of the CS4215. Therefore, this appendix is included to describe the differences between version 0 and version 1. This information is only useful for users that still have version 0 devices since version 1 devices will supplant the earlier version. The revision number can be found in control mode, time slot 7. The revision can also be identified by the revision letter stamped on the top of the actual chip. The revision letter immediately precedes the data code in the package marking. Version 0 corresponds to chip revision C and version 1 corresponds to chip revision D. Future chip revisions (ie. E, F, G) may still be version 1 since the version number only changes if there is a software change to the part.

The functional differences between the two revisions are as follows:

1. FSYNC on rev. 0 MUST be only one SCLK period high, whereas on rev. 1 FSYNC must be AT LEAST one SCLK period high.
2. When driving an external CMOS clock into one of the XTALIN pins, rev. 0 devices must have a series resistor of at least  $1k\Omega$  between the CS4215 and the clock source. The resistor is needed because the codec will put XTALIN to ground (on rev. 0 only) when that crystal is not selected, as is the case on power-up.
3. The OLB and ITS bits do not exist on rev. 0. Writing these bits as zero makes both versions function identically; therefore, version 1 is backwards compatible with version 0.
4. When entering control mode, CLKOUT stops 4 to 12 clocks later and may start up briefly when switching master clock sources on rev. 0. On rev. 1 CLKOUT stops within two clocks and doesn't start up until data mode is entered.
5. In rev. 0 the headphone and speaker outputs were not short-circuit protected, whereas in rev. 1 they are.

## CS4215 Evaluation Board

### Features

- Easy DSP Hook-up
- Correct Grounding and Layout
- Microphone pre-amplifier
- Line Input buffer
- Digital Patch Area

### General Description

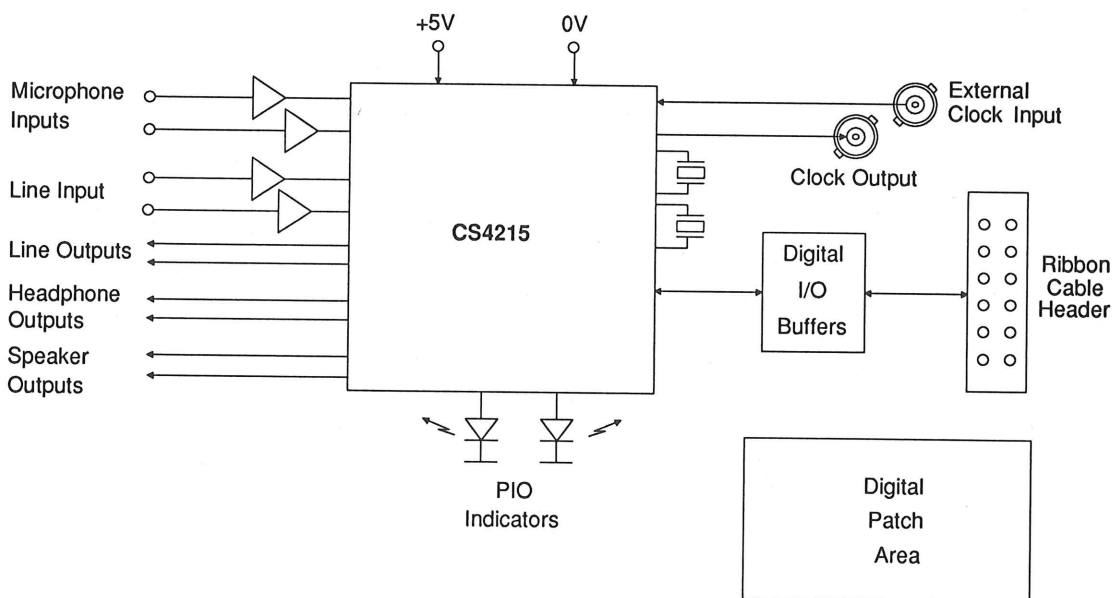
The CDB4215 evaluation board allows easy evaluation of the CS4215 audio multimedia codec. Analog inputs provided include 2 1/4" microphone jacks and 2 BNC line inputs. Analog outputs provided are 2 BNC line outputs, 1 stereo 1/4" headphone jack and 1 pair of speaker terminals.

Digital interfacing is facilitated by a fully buffered ribbon cable header.

ORDERING INFORMATION: CDB4215

2

### Block Diagram



**•Notes•**



## Stereo Audio Codec

### Features

- CMOS Stereo Audio Input/Output System
  - Delta-Sigma A/D Converters
  - Delta-Sigma D/A Converters
  - Input Anti-Alias and Output Smoothing Filters
  - Programmable Input Gain and Output Attenuation
- Frame Rates of 4 kHz to 50 kHz
- CD Quality Noise and Distortion
  - > 80 dB Dynamic Range
- Internal 64X Oversampling
- Low Power Dissipation: 80 mA
  - 1 mA power-down mode for portable applications

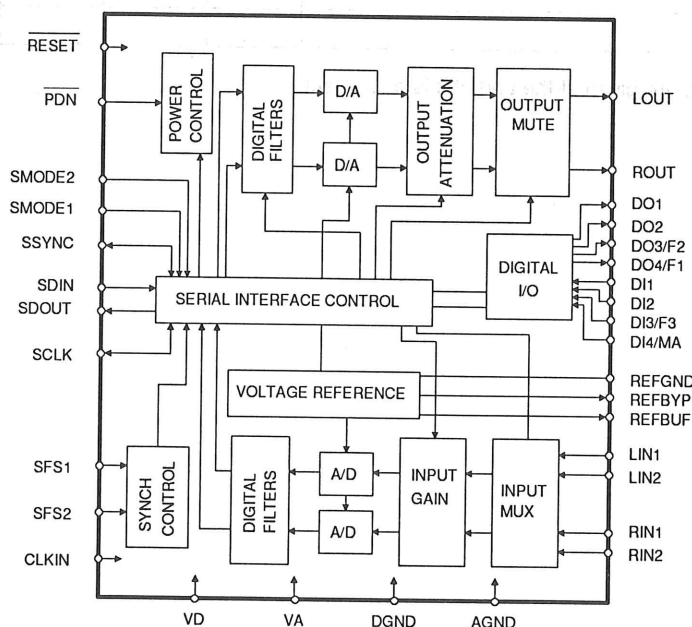
### General Description

The CS4216 Stereo Audio Codec is a monolithic CMOS data conversion device for computer multimedia, automotive stereo, and portable digital audio tape (DAT) applications. It performs A/D and D/A conversion, filtering, and level setting, creating 2 audio inputs and 2 audio outputs for a digital computer system. The digital interfaces of left and right channels are multiplexed into a single serial data bus with word rates up to 50 kHz per channel. Up to 4 CS4216 devices can be attached to a single hardware bus.

Both the ADC's and the DAC's use delta-sigma modulation with 64X oversampling. The ADC's include a digital decimation filter which eliminates the need for an external anti-alias filter. The DAC's include output smoothing filters on-chip. Input gain can be adjusted from 0 to +22.5 dB and output attenuation can be adjusted from 0 to -46.5 dB, both in 1.5 dB steps.

The CS4216 is packaged in a 44-pin PLCC.

Ordering Information: CS4216-KL



### Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation  
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(512) 445-7222 FAX: (512) 445-7581

MAR '92  
DS83PP4  
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**ANALOG CHARACTERISTICS** (  $T_A = 25^\circ\text{C}$ ;  $V_A, V_D = +5\text{V}$ ; Input Levels: Logic 0 = 0V, Logic 1 =  $V_D$ ; Full Scale Input Sine wave, 1 kHz; CLKIN = 24.576 MHz; Conversion Rate = 48 kHz; SCLK = 12.288 MHz; Measurement Bandwidth is 10 Hz to 20 kHz; Unless otherwise specified.)

Parameter *	Symbol	Min	Typ	Max	Units
<b>Analog Input Characteristics</b> - Minimum gain setting (0 dB); unless otherwise specified.					
ADC Resolution		16	-	-	Bits
ADC Differential Nonlinearity		-	-	$\pm 0.9$	LSB
Dynamic Range		80	84	-	dB
Signal-to-(Noise + Distortion)	S/(N+D)	80	-	-	dB
Interchannel Isolation		-	80	-	dB
Interchannel Gain Mismatch		-	-	0.1	dB
Frequency Response		-0.5	-	+0.2	dB
Programmable Input Gain		-0.2	-	22.7	dB
Gain Step		1.3	1.5	1.7	dB
Gain Drift		-	100	-	ppm/ $^\circ\text{C}$
Offset Error		-	10	-	LSB
Full Scale Input Voltage (No gain)		2.66	2.8	2.94	$V_{pp}$
Input Resistance		20	-	-	$k\Omega$
Input Capacitance		-	-	15	pF

\* Parameter definitions are given at the end of this data sheet.

Specifications are subject to change without notice.

## ANALOG CHARACTERISTICS (Continued)

Parameter *	Symbol	Min	Typ	Max	Units
<b>Analog Output Characteristics</b> - Minimum Attenuation; Unless Otherwise Specified.					
DAC Resolution		16	-	-	Bits
DAC Differential Nonlinearity		-	-	±0.9	LSB
Dynamic Range		80	85	-	dB
Signal-to-(Noise + Distortion) (Note 1)		80	-	-	dB
Interchannel Isolation (Note 1)		-	80	-	dB
Interchannel Gain Mismatch		-	-	0.2	dB
Frequency Response		-0.5	-	+0.2	dB
Programmable Attenuation		-0.2	-	-46.5	dB
Attenuation Step		1.3	1.5	1.7	dB
Gain Drift		-	100	-	ppm/°C
REFBUF Output Voltage (Note 2) Maximum output current= 400 µA		1.9	2.1	2.3	V
Offset Voltage		-	10	-	mV
Full Scale Output Voltage (No Attenuation) (Note 1)		2.66	2.8	2.94	V <sub>pp</sub>
Deviation from Linear Phase		-	-	1	Degree
Out of Band Energy (22 kHz to 100 kHz)		-	-60	-	dB
<b>Power Supply</b>					
Power Supply Current (Note 3)	Operating	-	80	100	mA
	Power Down	-	-	1	mA
Power Supply Rejection (1 kHz)		-	40	-	dB

Notes: 1. 10 kΩ, 100 pF load.

2. REFBUF load current must be DC. To drive dynamic loads, REFBUF must be buffered. AC variations in REFBUF current may degrade ADC and DAC performance.

3. Typically operating VA current is 30mA, VD current is 50mA. Power supply current does not include output loading.

### A/D Decimation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.2	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		80	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.0	µs

### D/A Interpolation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.1/Fs	µs

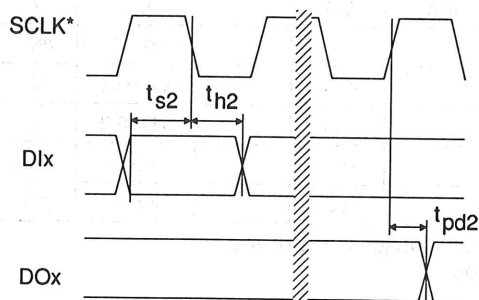
### DIGITAL CHARACTERISTICS (TA = 25°C; VA, VD = 5V)

Parameter	Symbol	Min	Typ	Max	Units
High-level Input Voltage	V <sub>IH</sub>	VD-1.0	-	-	V
Low-level Input Voltage	V <sub>IL</sub>	-	-	1.0	V
High-level Output Voltage at I <sub>O</sub> = -2.0 mA	V <sub>OH</sub>	VD-0.3	-	-	V
Low-level Output Voltage at I <sub>O</sub> = +2.0 mA	V <sub>OL</sub>	-	-	0.1	V
Input Leakage Current (Digital Inputs)		-	-	10	µA
Output Leakage Current (High-Z Digital Outputs)		-	-	10	µA
Output Capacitance	C <sub>OUT</sub>	-	-	15	pF
Input Capacitance	C <sub>IN</sub>	-	-	15	pF



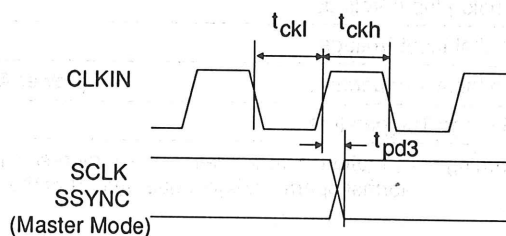
### SWITCHING CHARACTERISTICS (T<sub>A</sub> = 25°C; V<sub>A</sub>, V<sub>D</sub> = +5V, outputs loaded with 30 pF; Input Levels: Logic 0 = 0V, Logic 1 = V<sub>D</sub>)

Parameter	Symbol	Min	Typ	Max	Units
Input clock (CLKIN) frequency	SM1: CLKIN SM2, SM3: CLKIN	2.048 1.024	24.576 12.288	25.6 12.8	MHz MHz
CLKIN low time	t <sub>ckl</sub>	15	-	-	ns
CLKIN high time	t <sub>ckh</sub>	15	-	-	ns
Sample Rate	F <sub>s</sub>	4	-	50	kHz
Digital Inputs setup time to SCLK edge	t <sub>s2</sub>	10	-	-	ns
Digital Inputs hold time from SCLK edge	t <sub>h2</sub>	8	-	-	ns
Digital Outputs delay from SCLK edge	t <sub>pd2</sub>	30	-	-	ns
SCLK and SSYNC output delay from CLKIN rising (Master Mode)	t <sub>pd3</sub>	-	-	50	ns
SCLK period	t <sub>sckw</sub>	75	-	-	ns
SCLK high time	t <sub>sckh</sub>	25	-	-	ns
SCLK low time	t <sub>sckl</sub>	25	-	-	ns
SDIN, SSYNC setup time to SCLK edge	t <sub>s1</sub>	15	-	-	ns
SDIN, SSYNC hold time from SCLK edge	t <sub>h1</sub>	10	-	-	ns
SDOUT delay from SCLK edge	t <sub>pd1</sub>	-	-	30	ns
Output to Hi-Z state	bit 64	t <sub>hz</sub>	-	12	ns
Output to non-Hi-Z	bit 1	t <sub>nz</sub>	15	-	ns
RESET pulse width low		500	-	-	ns

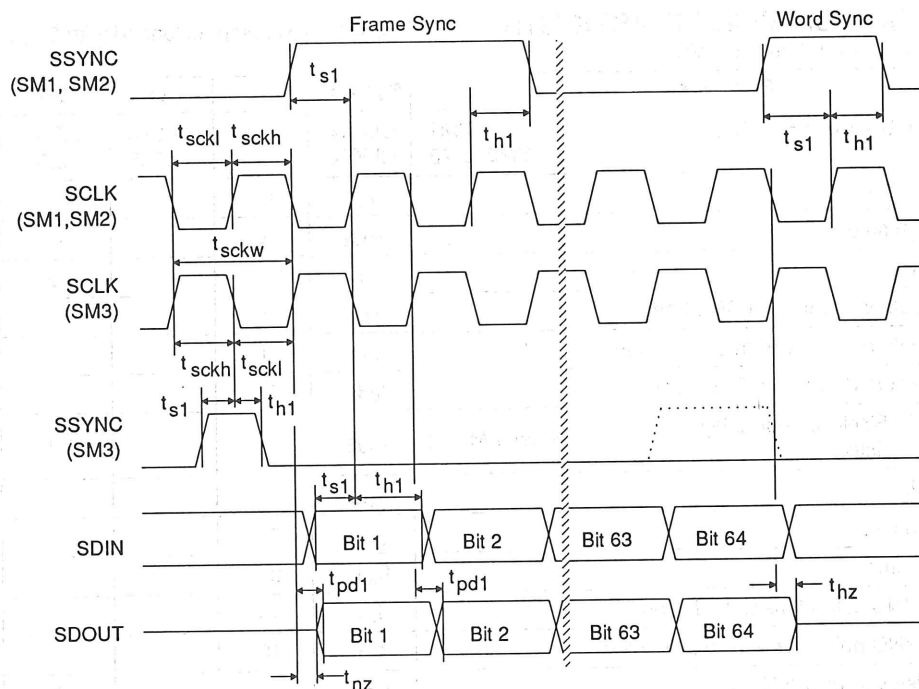


\* SCLK is inverted for SM1 and SM2

DI/DO Timing



SCLK & SSYNC Output Timing (Master Mode)



**Serial Data Plus SSYNC and SCLK Input Timing**

**ABSOLUTE MAXIMUM RATINGS** (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter	Symbol	Min	Typ	Max	Units	
Power Supplies:	Digital	VD	-0.3	-	6.0	V
	Analog	VA	-0.3	-	6.0	V
Input Current	(Except Supply Pins)		-	-	±10.0	mA
Analog Input Voltage			-0.3	-	VA+0.3	V
Digital Input Voltage			-0.3	-	VD+0.3	V
Ambient Temperature	(Power Applied)		-55	-	+125	°C
Storage Temperature			-65	-	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS** (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital	VD	4.75	5.0	5.25	V
	Analog	VA	4.75	5.0	5.25	V
Operating Ambient Temperature		TA	0	25	70	°C

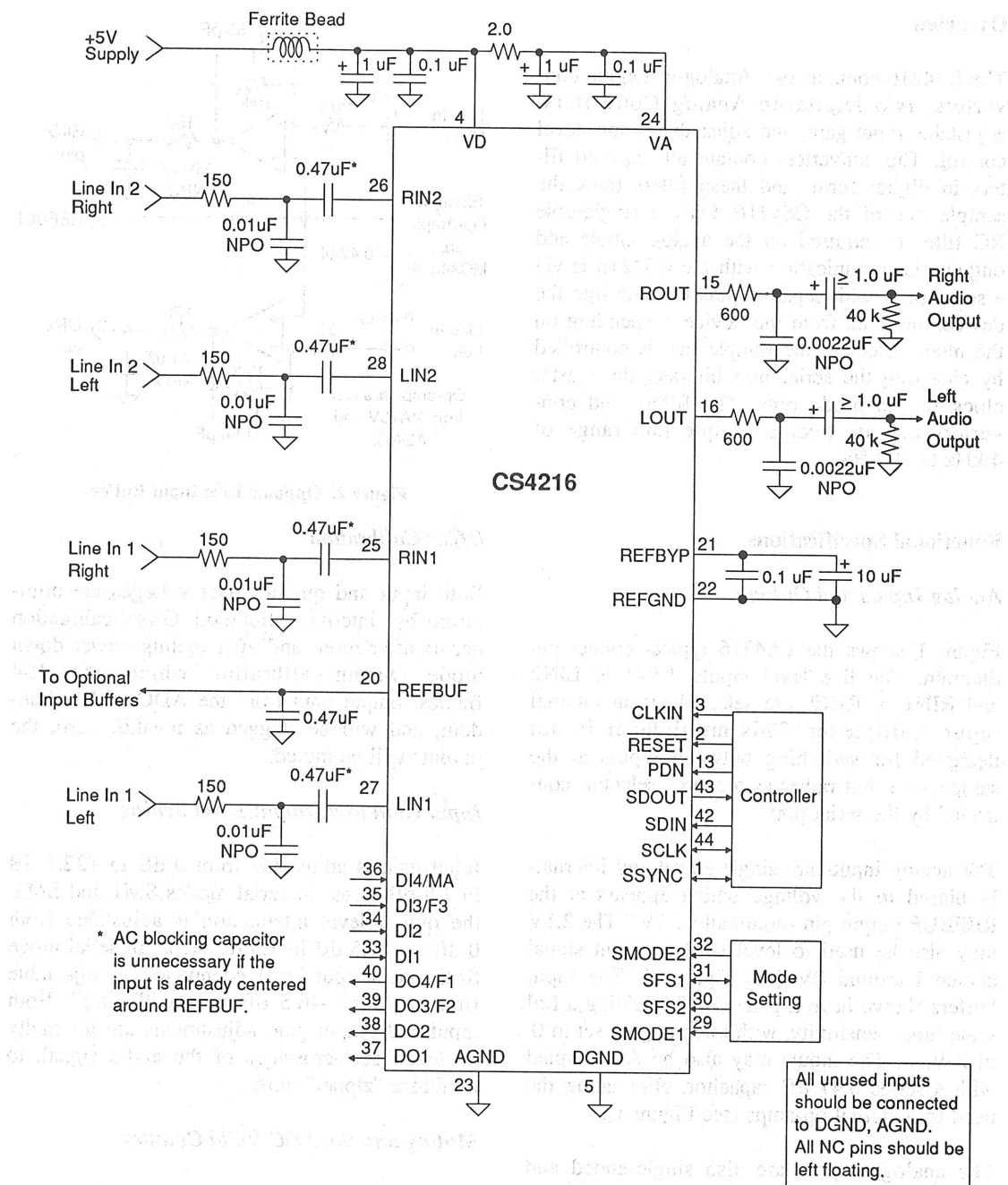


Figure 1. Typical Connection Diagram

## Overview

The CS4216 contains two Analog-to-Digital converters, two Digital-to-Analog Converters, adjustable input gain, and adjustable output level control. The converters contain all required filters in digital form, and these filters track the sample rate of the CS4216. Only a single-pole RC filter is required on the analog inputs and outputs. Communication with the CS4216 is via a serial port, with separate pins for data into the device, and data from the device. Depending on the mode selected, the sample rate is controlled by changing the serial port bit rate, the master clock or via mode pins. The filters and converters operate over a sample rate range of 4 kHz to 50 kHz.

## Functional Specifications

### Analog Inputs and Outputs

Figure 1 shows the CS4216 typical connection diagram. The line level inputs, LIN1 or LIN2 and RIN1 or RIN2, are selected by an internal input multiplexer. This multiplexer is not designed for switching between inputs at the sample rate, but rather as a source selector, controlled by the serial port.

The analog inputs are single-ended and internally biased to the voltage which appears at the REFBUF output pin (nominally 2.1V). The 2.1V may also be used to level shift an input signal centered around 0V (see Figure 2). The input buffers shown have a gain of 0.5, yielding a full scale input sensitivity, with internal gain set to 0, of 2 V<sub>rms</sub>. The inputs may also be AC coupled with a series 0.47  $\mu$ F capacitor, eliminating the need for external op-amps (see Figure 1).

The analog outputs are also single-ended and referenced to the REFBUF pin. AC coupling capacitors of >1  $\mu$ F are recommended.

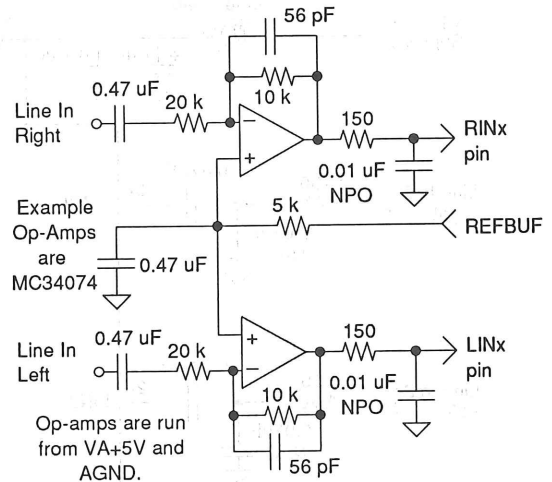


Figure 2. Optional Line Input Buffer

### Offset Calibration

Both input and output offset voltages are minimized by internal calibration. Offset calibration occurs after reset, and after exiting power down mode. During calibration, which takes 194 frames, output data from the ADC will be random, and will be flagged as invalid. Also, the outputs will be muted.

### Input Gain and Output Level Setting

Input gain is adjustable from 0 dB to +22.5 dB in 1.5 dB steps. In serial modes SM1 and SM2, the output level attenuation is adjustable from 0 dB to -22.5 dB in 1.5 dB steps. In serial mode SM3, the output level attenuation is adjustable from 0 dB to -46.5 dB in 1.5 dB steps. Both input and output gain adjustments are internally made on zero-crossings of the audio signal, to minimize "zipper" noise.

### Muting and the ADC Valid Counter

The mute function allows the output channels to be silenced. It is the controlling CPU responsibility to reduce the signal level to a low value



before muting, to avoid an audible click. The outputs should be muted before a sample rate change is initiated by the serial channel.

A "Valid Data" indicator for the A/D converters is included, and it is false until enough clocks have passed since reset, or low-power (power down mode) operation to have valid A/D data from the filters, i.e., the full latency of the digital filters has passed.

### Parallel Digital Input/Output Pins

In serial mode 1 and 2, there are 4 digital input and 4 digital output pins on the codec. In serial mode 3, there are 2 digital input and 2 digital output pins. These pins may be used to control output devices, or to sense input conditions. These pins are controlled and sensed by the serial port data. Figure 3 shows when the DI pins status is latched, and when the DO pins are updated in SM3. Alternate SSYNC timing is possible, depending on the serial mode selected.

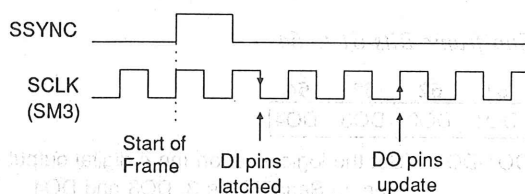


Figure 3. Digital Input/Output Timing

### Power Down Modes

Hard power down mode may be initiated by bringing the  $\overline{\text{PDN}}$  pin low. All analog output pins will be driven to the REFBUF voltage and all digital outputs will go to a Hi-Z state. Minimum power consumption will occur if CLKIN is set low.

Alternatively, soft power down may be initiated, in slave mode, by reducing SCLK frequency below the minimum CLKIN/12. In this case, the output is muted, and the CS4216 goes into soft

power-down mode. The serial data out from the codec will indicate invalid data and the appropriate error code. Note that in this mode, the parallel bit I/O is still functional. This is in effect a low power mode with only the parallel bit I/O unit functioning.

### Serial Interface

#### Overview

The serial port uses 4 pins: SDOUT, SDIN, SCLK and SSYNC. SDIN carries the D/A converters' input data and control bits. Input data is ignored for frames not allocated to the selected CS4216. SDOUT carries the A/D converters' output data and status bits. SDOUT goes to a Hi-Z state during frames not allocated to the selected CS4216. SCLK clocks data in and out of the CS4216. The rising edge of SCLK clocks data out on SDOUT. The falling edge latches data on SDIN into the port (SCLK polarity is inverted in Serial Mode 1&2). SSYNC indicates the start of a frame and/or sub-frame.

The serial port protocol is based on frames consisting of 1, 2 or 4, 64-bit sub-frames. The frame rate is the system sample rate. Each sub-frame is used by one CS4216 device. Up to 4 CS4216's may be attached to the same serial control lines. SFS1 and SFS2 are tied low or high to indicate to each CS4216 which sub-frame is allocated for it to use.

#### Serial Data Format

A sub-frame consists of 64 bits; two 16-bit audio values plus two 16-bit auxiliary fields. The audio data is MSB first, 2's complement format. The sub-frame bit assignments, numbered 1 through 64, are shown in Figures 4 and 5.

## INPUT DATA BIT DEFINITIONS

### Sub-frame bits 1 to 16

Left DAC Audio Data, MSB first, 2's complement coded.

### Sub-frame Bits 17 to 24

17	18	19	20	21	22	23	24
0	0	0	0	0	MUTE	ISL	ISR

**MUTE** Mute D/A Outputs  
0 - Normal Outputs  
1 - Mute Outputs

**ISL** Select Left Input Mux  
0 - Select LIN1  
1 - Select LIN2

**ISR** Select Right Input Mux  
0 - Select RIN1  
1 - Select RIN2

### Sub-frame Bits 25 to 32

25	26	27	28	29	30	31	32
LG3	LG2	LG1	LG0	RG3	RG2	RG1	RG0

**LG3-LG0** Sets left input gain.  
LG3 is the MSB. LG0 represents 1.5 dB.  
0000 = no gain.  
1111 = +22.5 dB gain

**RG3-RG0** Sets right input gain.  
RG3 is the MSB. RGO represents 1.5 dB.  
0000 = no gain  
1111 = +22.5 dB gain

### Sub-frame Bits 33 to 48

Right DAC audio data MSB first, 2's complement coded.

### Sub-frame Bits 49 to 50

Must be zero.

### Sub-frame Bits 51 to 60

51	52	53	54	55	56	57	58	59	60
*LA4	LA3	LA2	LA1	LA0	RA4	RA3	RA2	RA1	RA0
†0	0	LA3	LA2	LA1	LA0	RA3	RA2	RA1	RA0

LA4-LA0 Sets left output attenuation

†SM1, 2	*SM3
LA3 is the MSB. 0000 = no attenuation 1111 = -22.5 dB	LA4 is the MSB. 00000 = no attenuation 11111 = -46.5 dB

LA0 represents 1.5 dB.

RA4-RA0 Sets right output attenuation

†SM1, 2	*SM3
RA3 is the MSB. 0000 = no attenuation 1111 = -22.5 dB	RA4 is the MSB. 00000 = no attenuation 11111 = -46.5 dB

RA0 represents 1.5 dB.

### Sub-frame Bits 61 to 64

61	62	63	64
DO1	DO2	DO3	DO4

**DO1-DO4** Set the logic level on the 4 digital output pins. In Serial Mode 3, DO3 and DO4 are used for mode selection, and are not available for digital outputs.

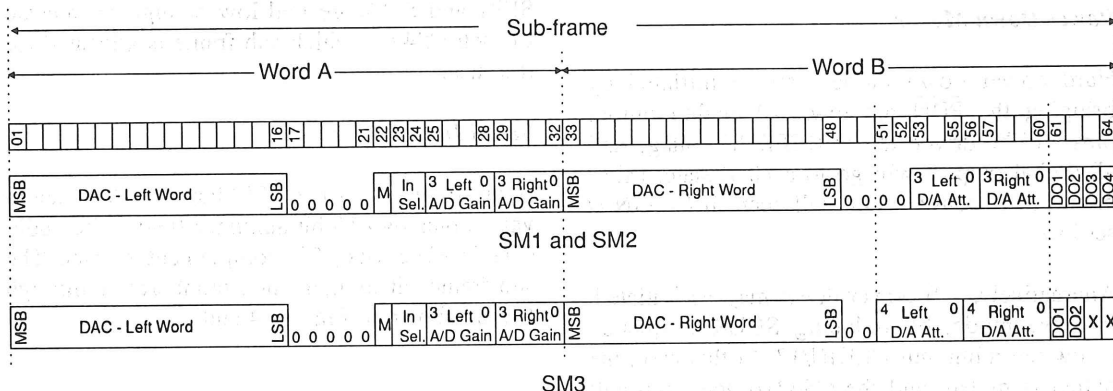


Figure 4. Serial Data Input Format

## OUTPUT DATA BIT DEFINITIONS

### Sub-frame Bits 1 to 16

Left ADC Audio Data, MSB first, 2's complement coded.

### Sub-frame Bits 17 to 24

17	18	19	20	21	22	23	24
RESERVED				0	ADV	LCL	RCL

**ADV** ADC Valid data bit.  
0 - Invalid ADC data  
1 - Valid ADC data  
Indicates ADC has completed initialization after power-up, low power mode, or mute.

**LCL** Left ADC clipping indicator

0 - Normal  
1 - Clipping

**RCL** Right ADC clipping indicator

0 - Normal  
1 - Clipping

**RESERVED** bits can be 0 or 1

### Sub-frame Bits 25 to 32

25	26	27	28	29	30	31	32
ER3	ER2	ER1	ER0	RV3	RV2	RV1	RV0

**ER3-ER0** Error Word

0000 - Normal - No errors.  
0001 - Sub-frame Bit 1 is set.  
0010 - Sync Pulse is incorrect.  
Causes the analog output to mute.  
0011 - Serial clock frequency is outside the allowable range. Causes the analog output to mute.

**RV3-RV0** Revision Level

0000 = 1st revision

### Sub-frame Bits 33 to 48

Right ADC Audio Data, MSB first, 2's complement coded.

### Sub-frame Bits 49 to 60

These bits are reserved, and can be 0 or 1.

### Sub-frame Bits 61 to 64

61	62	63	64
DI1	DI2	DI3	DI4

**DI1-DI4** These bits follow the state of the Digital Input pins. In Serial Mode 3, DI3 and DI4 are used for mode setting and are not available as input bits.

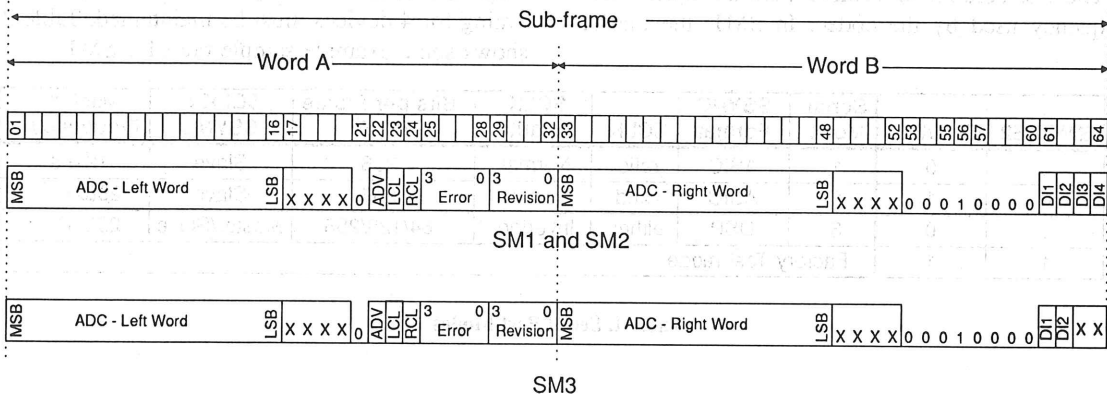


Figure 5. Serial Data Output Format

## CS4216 SERIAL INTERFACE MODES

The CS4216 has 3 serial port modes, selected by the SMODE1 & SMODE2 pins. In all modes, CLKIN, SCLK and SSYNC must be derived from the same clock source. Table 1 lists the serial port formats available, along with some of the differences between modes. The first two columns in Table 1 select the serial mode. The SSYNC Format column describes the type of interface SSYNC is designed for. The ASIC format of SSYNC has a frame sync and an embedded word sync providing a simple interface when designing ASIC's. The DSP format of SSYNC has a single start-of-frame pulse one SCLK period before the start of a frame and is compatible with industry standard DSP's. The SCLK column describes how SCLK is used. In Serial Mode 1, SM1, the ratio of SCLK to CLKIN is sensed and used internally to select the sample frequency. In SM2, SCLK is fixed at 256 times the sample frequency and SCLK is used as the master clock. In SM3, SCLK could be a ratio to CLKIN or fixed at  $256 \times F_s$  based on a sub-mode which is described later. In both SM1 and SM2, there are 256 bits per frame which allows up to four codecs to occupy the same bus. In SM3, the number of bits per frame is programmable. In SM1 and SM2, SCLK and SSYNC must be generated externally; whereas, in SM3 the CS4216 can optionally generate those signals. The last column in Table 1 lists the master frequency used by the codec. In SM1, the master

frequency, input on CLKIN, is 512 times the highest sample frequency available. In SM2, the master frequency is 256 times the sample frequency and in this mode SCLK is the master clock. In SM3, the master frequency is 256 times the highest frequency available and is input on CLKIN or SCLK, based on the sub-mode used. In SM3, SCLK is inverted compared to SM1 and SM2

### SERIAL MODE 1, SM1

Serial Mode 1 is selected by connecting SMODE1 and SMODE2 to 0. SM1 uses a word sync combined with a frame sync. In this mode, SSYNC is high for the first two SCLK periods indicating the beginning of a frame, and high for one SCLK period during the first bit of each successive word. In SM1, two clocks control internal operation. These are the master clock (CLKIN) and the serial clock (SCLK). CLKIN should be set to  $512 \times F_{smax}$ , where  $F_{smax}$  is the maximum required sample rate. SCLK must be set externally to a value  $1/N$  of CLKIN, such that SCLK equals 256 times the desired sample rate. The codec senses the ratio between CLKIN and SCLK and will cause the CS4216 to go into soft power down mode if the SCLK drops to  $< CLKIN/12$ . Even if only 1 CS4216 is used, the timing for 4 devices must be maintained. Table 2 shows some example sample rates for SM1.

SMODE2	SMODE1	Serial Mode	SSYNC Format	SCLK	SCLK Polarity	Bits per Frame (BPF)	SCLK & SSYNC	Master Frequency
0	0	1	ASIC	ratio	Normal	256	Slave	$512 \times F_s$
0	1	2	ASIC	fixed	Normal	256	Slave	$256 \times F_s$
1	0	3	DSP	either	Inverted	64/128/256	Master/Slave	$256 \times F_s$
1	1	Factory Test mode						

Table 1. Serial Port Modes

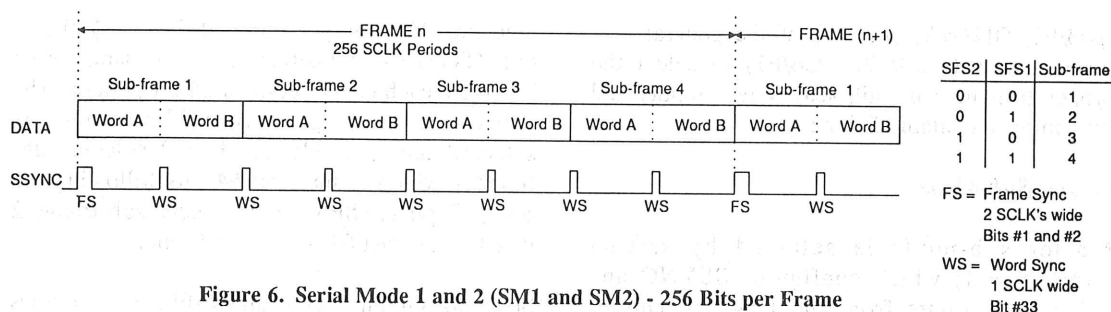


Figure 6. Serial Mode 1 and 2 (SM1 and SM2) - 256 Bits per Frame

Sample Rate kHz	SCLK MHz	CLKIN MHz	N
48	12.288	24.576	2
32	8.192	24.576	3
24	6.144	24.576	4
19.2	4.9152	24.576	5
16	4.096	24.576	6
12	3.072	24.576	8
9.6	2.4576	24.576	10
8	2.048	24.576	12
7.2	1.843	22.116	12
44.1	11.2896	22.5792	2

Table 2. SM1 Example Clock Frequencies

## SERIAL MODE 2, SM2

Serial Mode 2 is enabled by setting  $SMODE1 = 1$  and  $SMODE2 = 0$ . SM2 uses the same format as specified in SM1 except that SCLK is fixed at  $256 \times F_s$  and is used instead of CLKIN. The CLKIN pin is ignored in this mode. Since CLKIN is a CMOS input, it should be tied high or low if not driven by a logic gate. In this mode, the sample frequency will scale linearly with the frequency of SCLK. Up to four codecs may occupy the serial bus since each codec only requires 64 bit periods and there are 256 bit periods per frame.

## SERIAL MODE 3, SM3

Serial Mode 3 is enabled by setting  $SMODE2 = 1$  and  $SMODE1 = 0$ .

### Master Clock Frequency

In SM3, the master clock, CLKIN, must be  $256 \times F_{smax}$ . Therefore, for a 48 kHz maximum sample frequency, the master clock must be 12.288 MHz.

### D/A Attenuation

SM3 has one more bit per channel allocated for D/A attenuation. This added bit doubles the attenuation range. Figure 4 illustrates the serial data in, SDIN line, for all serial port modes. The upper data in this figure shows modes SM1 and SM2 where the D/A attenuation is located in Word B, bits 53 through 60. Four bits allow attenuation on each channel from 0 dB down to 22.5 dB using 1.5 dB steps. In SM3 the attenuation bits are still located in Word B, except in this mode they start at bit 51 of the sub-frame. This allows five bits of attenuation per channel instead of four, thereby allowing attenuation for each channel from 0 dB down to 46.5 dB.

SM3 is divided into two sub-modes, Master and Slave. In Master sub-mode, the CS4216 generates SSYNC and SCLK, while in Slave sub-mode they must be generated externally. SM3 redefines two of the general purpose inputs



(DI3/F3, DI4/MA) and two of the general purpose outputs (DO3/F2, DO4/F1) to select the proper format. This still leaves two inputs and two outputs available for the user.

### Master Sub-Mode

Master sub-mode is selected by setting DI4/MA = 1, which configures SSYNC and SCLK as outputs from the CS4216. During power down, SSYNC and SCLK are driven high impedance, and during reset they both are driven low. The number of bits per frame is programmable and is illustrated in Figure 7.

#### SFS2 - Bits Per Frame

SFS2 selects the number of bits per frame. The two options are SFS2 = 1 which selects 128 bits per frame, and SFS2 = 0 which selects 64 bits per frame.

Selecting 128 bits per frame (SFS2 = 1) allows two CS4216's to operate from the same serial bus since each codec requires 64 bit periods. The sub-frame used by an individual codec is selected using SFS1. SFS1 = 0 selects sub-frame 1 which is the first 64 bits following the SSYNC pulse. SFS1 = 1 selects sub-frame 2 which is the last 64 bits of the frame.

Selecting 64 bits per frame (SFS2 = 0) allows only one CS4216 to occupy the serial port. Since there is only one sub-frame (which is equal to one frame), SFS1 is defined differently in this mode. SFS1 selects the format of SSYNC. SFS1 = 0 selects SSYNC equal to one SCLK period high, directly preceding the data as shown in the center portion of Figure 7. This format is used for all other Master and Slave sub-modes in SM3. If SFS1 = 1, an alternate SSYNC format is chosen in which SSYNC is high during the entire Word A (32 bits) which includes the left sample, and low for the entire Word B (32 bits)

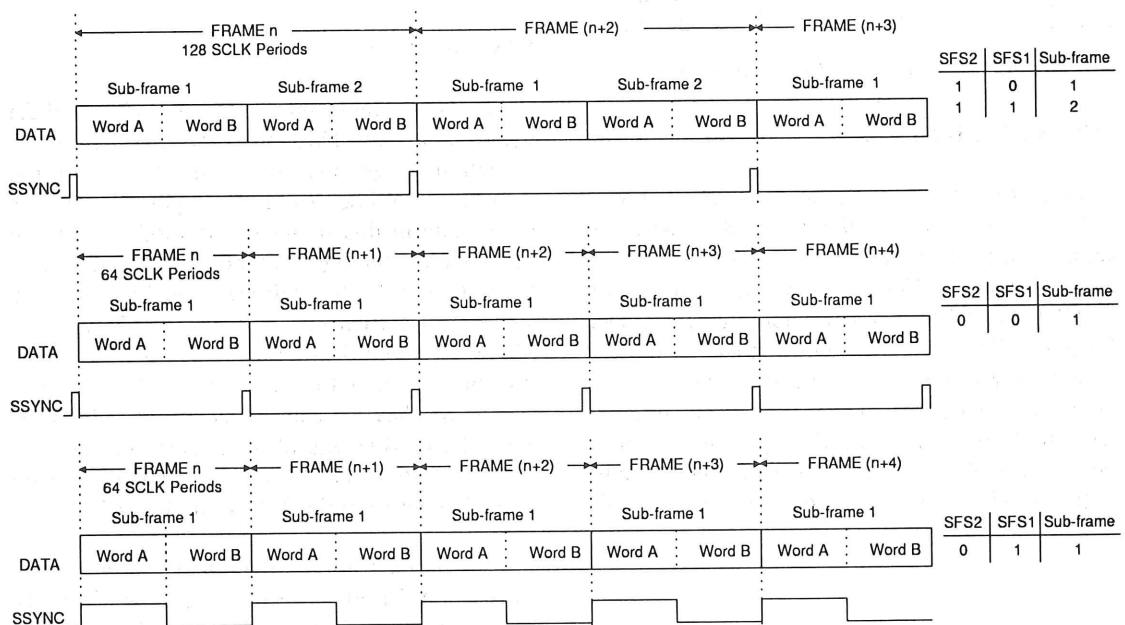


Figure 7. SM3, Master Sub-Mode

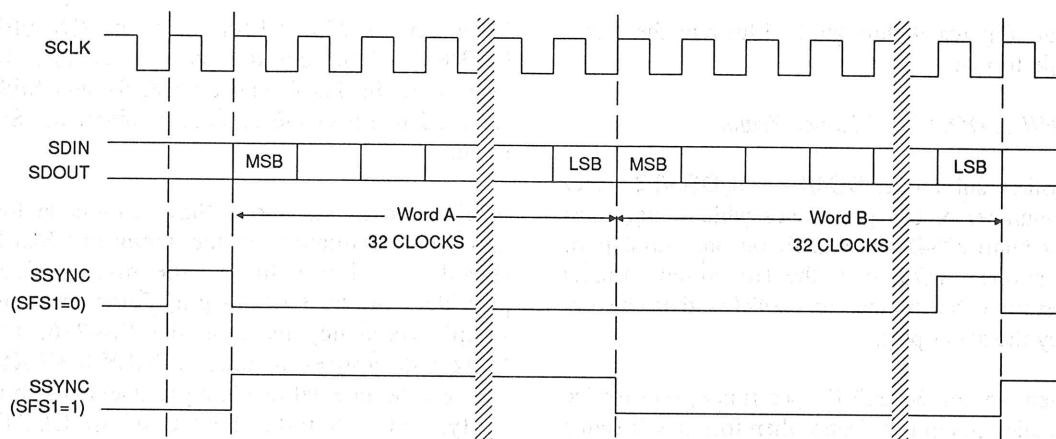


Figure 8. SM3, Detailed Master sub-Mode, 64 BPF

DO4/ F1	DO3/ F2	DI3/ F3	Fs(kHz) with CLKIN 12.288 MHz	Fs(kHz) with CLKIN 11.2896 MHz
0	0	0	48.00	44.10
0	0	1	32.00	29.40
0	1	0	24.00	22.05
0	1	1	19.20	17.64
1	0	0	16.00	14.70
1	0	1	12.00	11.025
1	1	0	9.60	8.82
1	1	1	8.00	7.35

Table 3. SM3, Master Sub-Mode Fs Select

DO4/ F1	DO3/ F2	Bits per Frame	Sample Frequency/ SCLK
0	0	64	ratio to CLKIN sensed
0	1	128	ratio to CLKIN sensed
1	0	256	ratio to CLKIN sensed
1	1	256	fixed. = 256×Fs

Table 4. Slave Mode Bits per Frame

which includes the right sample. This alternate format for SSYNC is illustrated in the bottom portion of Figure 7 and is only available in Master sub-mode with 64 bits per frame. A more detailed timing diagram using 64 bits per frame is shown in Figure 8.

### Sample Frequency Selection

In SM3, Master sub-mode, DO4/F1, DO3/F2, and DI3/F3 are used to select the sample frequency divider. Table 3 lists the decoding for the sample frequency select and lists the sample frequencies obtained by using one of two example

master clocks: either 12.288 MHz or 11.2896 MHz.

### Slave Sub-Mode

In SM3, Slave sub-mode is selected by setting DI4/MA = 0 which configures SSYNC and SCLK as inputs to the CS4216. These two signals must be externally derived from CLKIN. The number of sub-frames on the serial port is selected using DO4/F1 and DO3/F2. In Slave sub-mode DI3/F3 works as a general purpose

input. Figures 9 through 11 illustrate the Slave mode formats.

### DO4/F1, DO3/F2 - Bits per Frame

In Slave sub-mode, DO4/F1 and DO3/F2 select the number of bits per frames which determines how many CS4216's can fit on one serial port. As shown in Table 4, the first three formats determine the number of CS4216s that can occupy the serial port.

When set for 64 SCLKs per frame, one device occupies the entire frame, therefore a sub-frame is equivalent to a frame. See Figure 9.

When set for 128 SCLKs per frame, two devices can occupy the serial port, with SFS1 selecting the particular sub-frame. See Figure 10.

When set for 256 SCLKs per frame (DO4/F1, DO3/F2 = 10), four devices can occupy the serial port. In this format both SFS2 and SFS1 are used to select the particular sub-frame. See Figure 11.

In all three of the above Slave sub-mode formats, the frequency of the incoming SCLK signal, in relationship to the master clock provided on the CLKIN pin, determines the sample frequency used on the CS4216. The CS4216 determines the ratio of SCLK to CLKIN and sets the internal operating frequency accordingly. Table 5 lists the SCLK to CLKIN frequency ratio used to determine the codec's sample frequency. To obtain a given sample frequency, SCLK must equal CLKIN divided by the number in the table, based on the number of bits per frame. As an example, assuming 64 BPF (bits per frame) and CLKIN = 12.288 MHz, if a

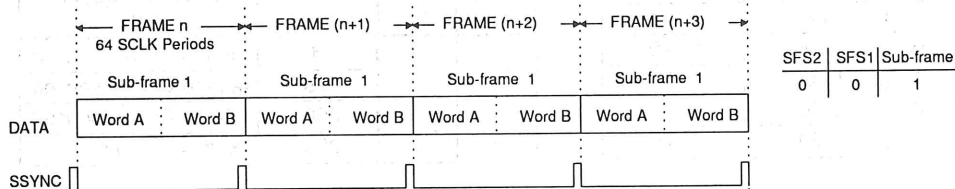


Figure 9. SM3, Slave Mode - 64 Bits per Frame; DO4/F1, DO3/F2 = 00

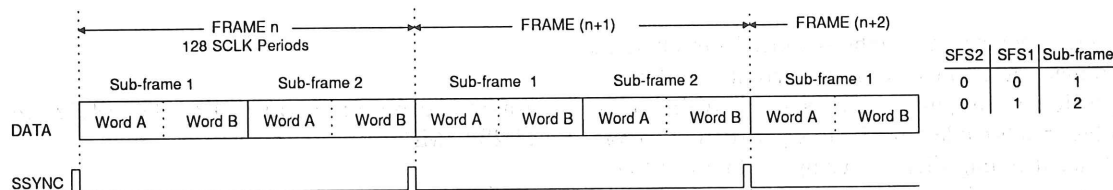


Figure 10. SM3, Slave Mode - 128 Bits per Frame; DO4/F1, DO3/F2 = 01

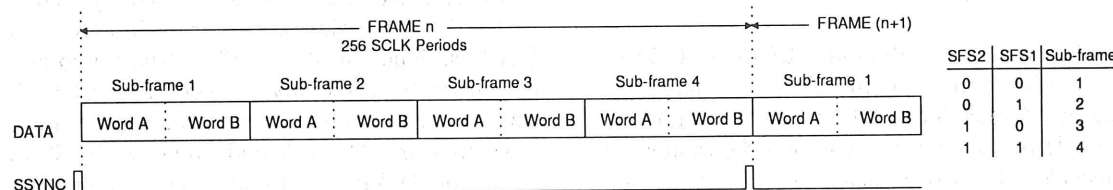


Figure 11. SM3, Slave Mode - 256 Bits per Frame; DO4/F1, DO3/F2 = 10

SCLK to CLKIN Ratio			Fs(kHz) with CLKIN 12.288 MHz	Fs(kHz) with CLKIN 11.2896 MHz
BPF 256	BPF 128	BPF 64		
1	2	4	48.00	44.10
1.5	3	6	32.00	29.40
2	4	8	24.00	22.05
2.5	5	10	19.20	17.64
3	6	12	16.00	14.70
4	8	16	12.00	11.025
5	10	20	9.60	8.82
6	12	24	8.00	7.35

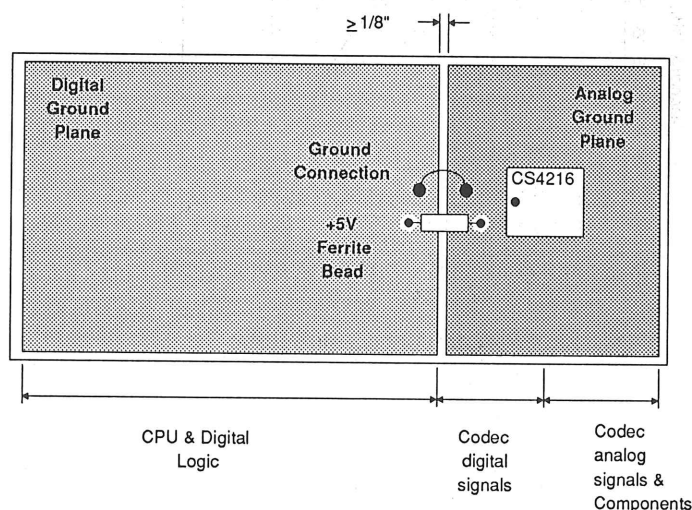
Table 5. SM3, Slave Sub-Mode, Fs Select

sample frequency of 24 kHz is desired, SCLK must equal CLKIN divided by 8 or 1.536 MHz.

When  $DO4/F1 = DO3/F2 = 1$ , SCLK is used as the master clock and is assumed to be 256 times the sample frequency. In this mode, CLKIN is ignored and the sample frequency is linearly scaled with SCLK. (The CLKIN pin must be tied high or low.) This mode also fixes SCLK at 256 bits per frame with SFS1 and SFS2 selecting the particular sub-frame. This format is similar to SM2, with SSYNC being a single pulse at the beginning of each frame.

### Power Supply and Grounding

The CS4216, along with associated analog circuitry, should be positioned near to the edge of your circuit board, and have its own, separate, ground plane. On the CS4216, the analog and digital grounds are internally connected; therefore, the AGND and DGND pins must be externally connected with no impedance between them. The best solution is to place the entire chip on a solid ground plane as shown in Figure 12. Preferably, it should also have its own power plane. The +5V supply must be connected to the CS4216 via a ferrite bead, positioned closer than 1" to the device. The VA supply can be derived from VD, as shown in Figure 1. Alternatively, a separate +5V analog supply may be used for VA, in which case, the  $2.0\Omega$  resistor between VA and VD is not required. A single connection between the CS4216 ground and the board ground should be positioned as shown in Figure 12.



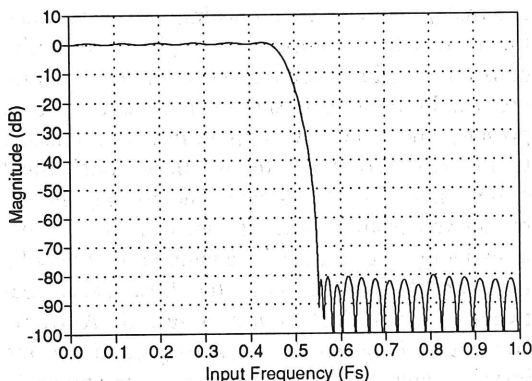
Note that the CS4216 is oriented with its digital pins towards the digital end of the board.

Figure 12. Suggested Layout Guideline

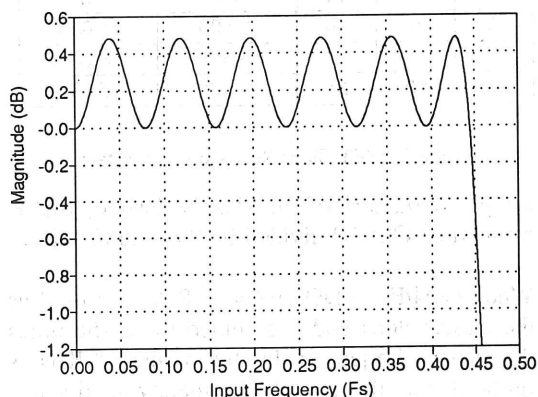
## ADC and DAC Filter Response Plots

Figures 13 - 18 shows the overall frequency response, passband ripple and transition band for

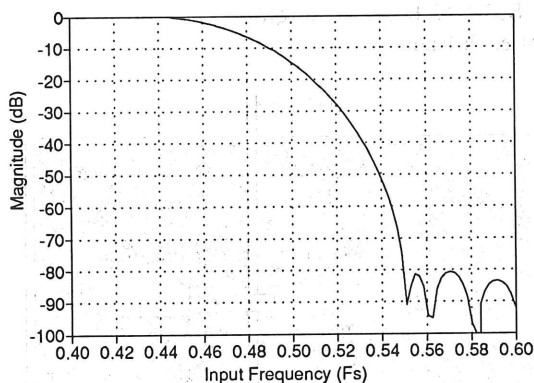
the CS4216 ADC's and DAC's. Figure 19 shows the DACs' deviation from linear phase.



**Figure 13. CS4216 ADC Frequency Response**

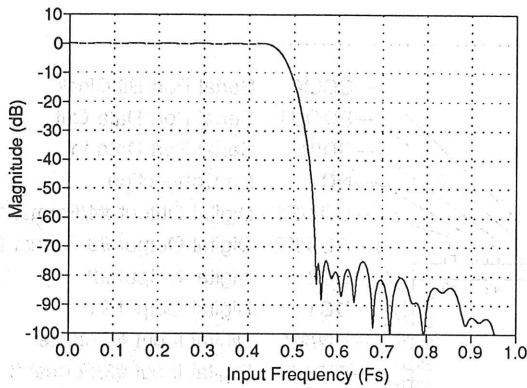


**Figure 14. CS4216 ADC Passband Ripple**

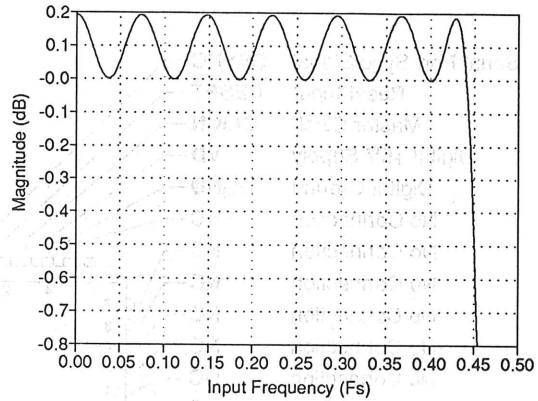


**Figure 15. CS4216 ADC Transition Band**

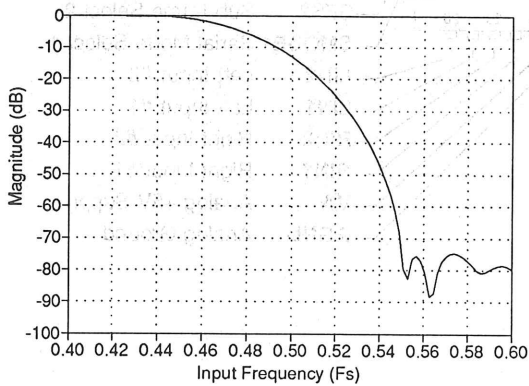




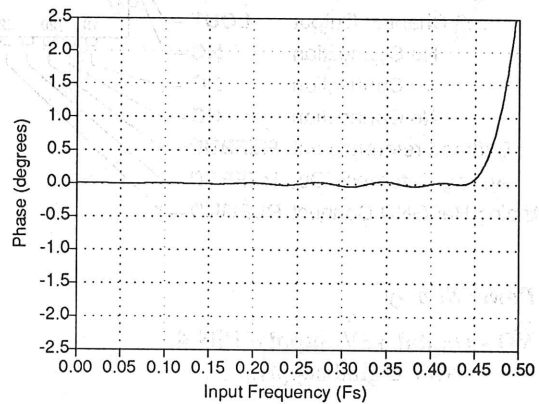
**Figure 16. CS4216 DAC Frequency Response**



**Figure 17. CS4216 DAC Passband Ripple**

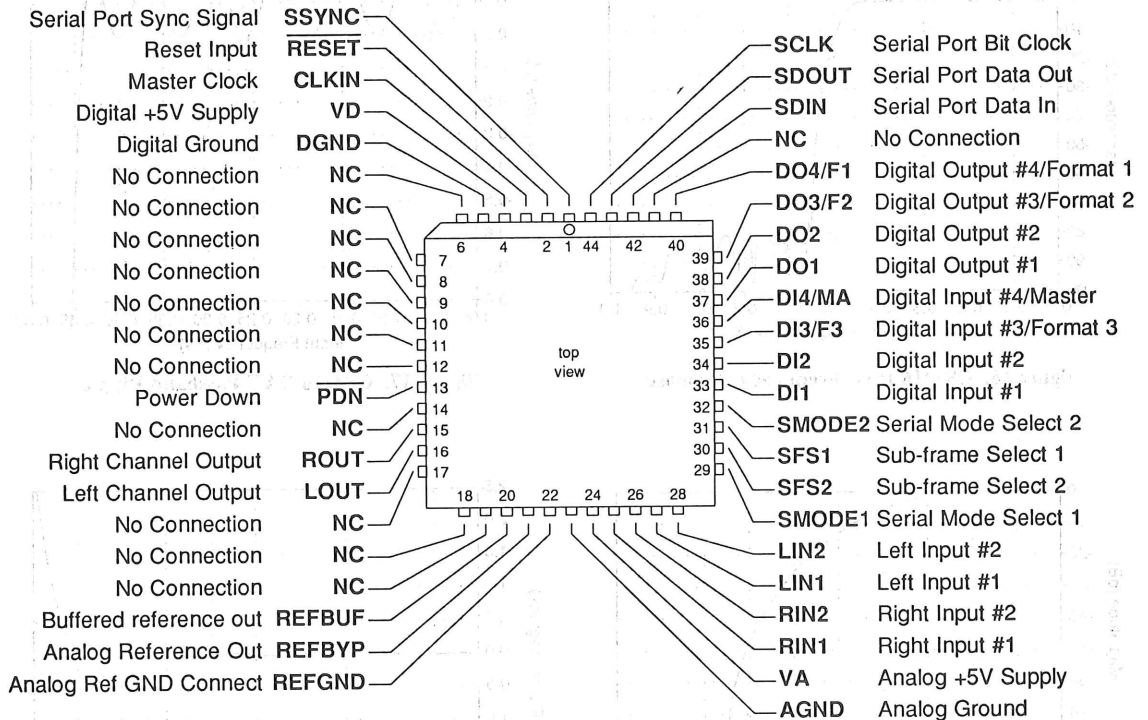


**Figure 18. CS4216 DAC Transition Band**



**Figure 19. CS4216 Deviation From Linear Phase**

## PIN DESCRIPTIONS



### Power Supply

**VD - Digital +5V Supply, PIN 4.**  
+5V digital supply.

**VA - Analog +5V Supply, PIN 24.**  
+5V analog supply.

**DGND - Digital Ground, PIN 5.**  
Digital ground. Must be connected to AGND with zero impedance.

**AGND - Analog Ground, PIN 23.**  
Analog ground. Must be connected to DGND with zero impedance.

### Analog Inputs

**RIN1 - Right Input #1, PIN 25.**  
Right analog input #1. Full scale input, with no gain, is 1Vrms, centered at REFBUF.

**RIN2 - Right Input #2, PIN 26.**  
Right analog input #2. Full scale input, with no gain, is 1Vrms, centered at REFBUF.

**LIN1 - Left Input #1, PIN 27.**

Left analog input #1. Full scale input, with no gain, is 1Vrms, centered at REFBUF.

**LIN2 - Left Input #2, PIN 28.**

Left analog input #2. Full scale input, with no gain, is 1Vrms, centered at REFBUF.

**Analog Outputs****ROUT - Right Channel Output, PIN 15.**

Right channel analog output. Maximum signal is 1 Vrms centered at REFBUF.

**LOUT - Left Channel Output, PIN 16.**

Left channel analog output. Maximum signal is 1 Vrms centered at REFBUF.

**REFBYP - Analog Reference Decoupling, PIN 21.**

A 10  $\mu$ F and 0.1  $\mu$ F capacitor must be attached between REFBYP and REFGND.

**REFGND - Analog Reference Ground Connection, PIN 22.**

Connect to AGND.

**REFBUF - Buffered Reference Out, PIN 20.**

A nominal +2.1V output for setting the bias level for external analog circuits.

**Serial Digital Interface Signals****SSYNC - Serial Port Sync Signal, PIN 1.**

Indicates the start of a frame in SM3, and also the start of a word in SM1 & SM2.

**SMODE1 - Serial Mode Select, PIN 29.**

Selects alternate serial modes.

**SMODE2 - Serial Mode Select, PIN 32**

Selects alternate serial modes.

**SFS1 - Sub-frame Select 1, PIN 31.**

SFS1 selects to which sub-frame this particular CS4216 is allocated.

**SFS2 - Sub-frame Select 2, PIN 30.**

SFS2 selects to which sub-frame this particular CS4216 is allocated.

**SDIN - Serial Port Data In, PIN 42.**

Digital audio data to the DACs and level control information is received by the CS4216 via SDIN.

**SDOUT - Serial Port Data Out, PIN 43.**

Digital audio data from the ADCs and status information is output from the CS4216 via SDOUT.

**SCLK - Serial Port Bit Clock, PIN 44.**

SCLK controls the data on SDOUT and latches the data on SDIN.

**Miscellaneous****RESET - Reset Input, PIN 2.**

Resets the CS4216 into a known state, and must be initiated after power up.

**CLKIN - Master Clock, PIN 3.**

CLKIN is the master clock that operates the internal logic.

**NC - No Connection, PINS 6, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19, 41.****PDN - Power Down, PIN 13.**

This pin causes the CS4216 to go into a power down state.

**DI1 - Parallel Digital Bit Input #1, PIN 33.**

Parallel port input bit #1.

**DI2 - Parallel Digital Bit Input #2, PIN 34.**

Parallel port input bit #2.

**DI3/F3 - Parallel Digital Bit Input #3/Format bit 3, PIN 35.**

Parallel port input bit #3. In Serial Mode 3, this pin is used to select alternate serial port formats.

**DI4/MA - Parallel Digital Bit Input #4/Master, PIN 36.**

Parallel port input bit #4. In Serial Mode 3, this pin is used to select master or slave mode.

**DO1 - Parallel Digital Bit Output #1, PIN 37.**

Parallel port output bit #1.

**DO2 - Parallel Digital Bit Output #2, PIN 38.**

Parallel port output bit #2.

**DO3/F2 - Parallel Digital Bit Output #3/Format bit 2, PIN 39.**

Parallel port output bit #3. In Serial Mode 3, this pin is used to select alternate serial port formats.

**DO4/F1 - Parallel Digital Bit Output #4/Format bit 1, PIN 40.**

Parallel port output bit #4. In Serial Mode 3, this pin is used to select alternate serial port formats.

**PARAMETER DEFINITIONS****2****Resolution**

The number of bits in the input words to the DACs, and in the output words in the ADCs.

**Differential Nonlinearity**

The worst case deviation from the ideal codewidth. Units in LSB.

**Dynamic Range**

The  $S/(N+D)$  with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces to harmonic distortion components of the noise to insignificance. Units in dB.

**Signal-to-(Noise + Distortion)**

$S/(N+D)$  is the ratio of the rms value of the input signal to the rms sum of all other spectral components within the measurement bandwidth (10 Hz to 20 kHz). Units in dB.

**Interchannel Isolation**

The amount of 1 kHz signal present on the output of the grounded input channel, with 1 kHz 0 dB signal present on the other channel. Units in dB.

**Interchannel Gain Mismatch**

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

**Frequency Response**

Worst case variation in output signal level versus frequency over 10 Hz to 20 kHz. Units in dB.

**Gain Error**

The deviation in output signal from ideal with a full scale input signal. Units in dB.

**Offset Error**

For the ADCs, the deviation (in LSB's) of the output from mid-scale with the selected input at REFBUF. For the DAC's, the deviation of the output from REFBUF with mid-scale input code. Units in volts.



## **CS4216 Evaluation Board**

### **Features**

- Easy DSP Hook-up
- Correct grounding and layout
- Line Input Buffers
- Patch Areas

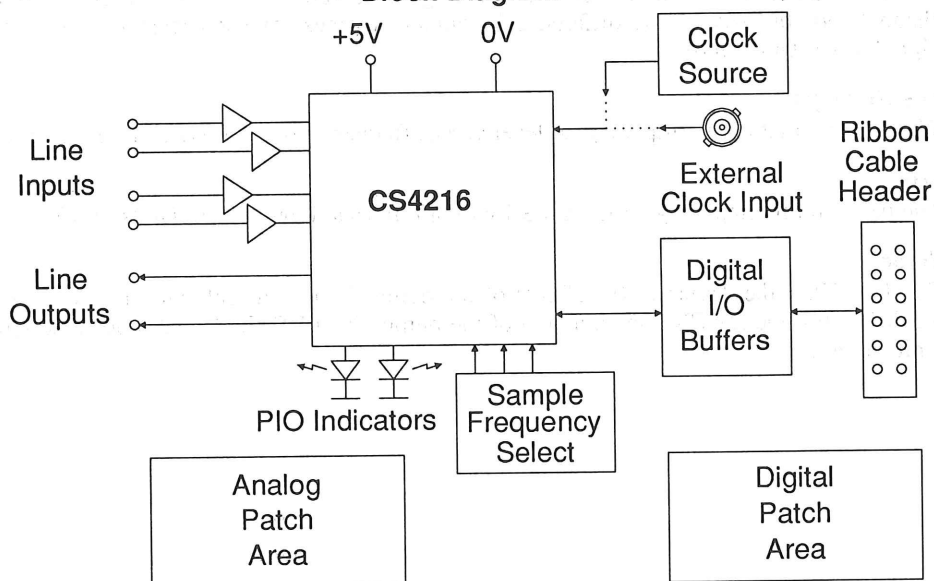
### **General Description**

The CDB4216 evaluation board allows easy evaluation of the CS4216 Audio codec. Four line level input BNC connectors are provided, along with 2 line level output BNC connectors.

Digital interfacing is via a fully buffered ribbon cable header.

**ORDERING INFORMATION:** CDB4216

### **Block Diagram**



## 107 dB, D/A Converter for Digital Audio

### Features

- Stereo Delta-Sigma D/A converter  
8x Interpolation Filter  
64x Delta-Sigma DAC
- Single +5V Operation
- Adjustable System sampling Rates  
including 32 kHz, 44.1 kHz and 48 kHz
- 107 dB Dynamic Range Over the  
Audio Bandwidth, A-Weighted
- 0.001 dB Passband Ripple
- Flexible Serial Input Port  
Supports Multiple Input Formats  
16 or 18 Bit Input Words

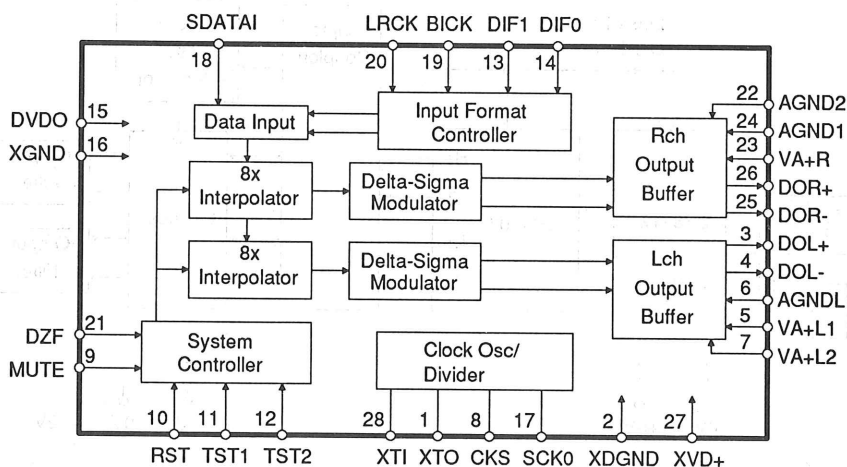
### General Description

The CS4303 is a high performance delta-sigma D/A converter for digital audio systems which require wide dynamic range. The CS4303 includes 8x interpolation and a 64x oversampled delta-sigma modulator that outputs a 1 bit signal to an external analog low pass filter. The 1's density of the 1 bit signal is proportional to the digital input.

The CS4303 has a selectable input serial port that provides four interface modes. The master clock rate can be either 256 or 384 times the input word rate, supporting various audio environments.

### Ordering Information:

Model	Temp. Range	Package Type
CS4303-KS	0° to 70°C	28-pin plastic SOIC
CS4303-KP	0° to 70°C	28-pin plastic DIP



### Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

**Crystal Semiconductor Corporation**  
P.O. Box 17847, Austin, TX 78760  
(512) 445-7222 FAX: (512) 445-7581

APR '92  
DS81PP1  
2-63

## CS4303 DAC Evaluation Board

### Features

- Low Noise Analog Filter
- Opto-coupled Analog Section
- VCXO Clock Jitter Attenuator
- Off-chip Latches
- Correct Power Supply and Grounding

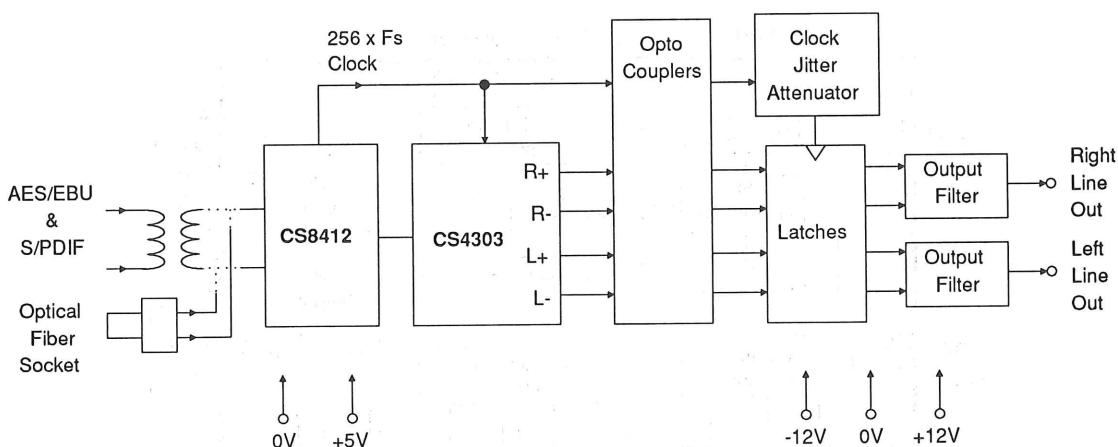
### General Description

The CDB4303 evaluation board provides all the required support circuitry to realize a high performance D/A converter system using the CS4303. Included on the board are: CS8412 AES/EBU & S/PDIF receiver, CS4303 I.C., opto-couplers, off-chip 1-bit data latches, clock jitter attenuator using a VCXO and a low noise analog reconstruction/anti-imaging filter.

Connectors are provided for fiber or coax digital inputs & RCA phono analog outputs.

ORDERING INFORMATION: CDB4303

### Block Diagram



# 18-Bit, Stereo D/A Converter for Digital Audio

## Features

- Complete Stereo DAC System  
8x Interpolation Filter  
64x Delta-Sigma DAC  
Analog Post Filter
- Adjustable System Sampling Rates  
including 32kHz, 44.1kHz & 48kHz
- 120 dB Signal-to-Noise Ratio
- Low Clock Jitter Sensitivity
- Completely Filtered Line-Level Outputs  
Linear Phase Filtering  
Zero Phase Error Between Channels  
No External Components Needed
- Flexible Serial Interface for Either 16 or 18 bit Input Data

## General Description

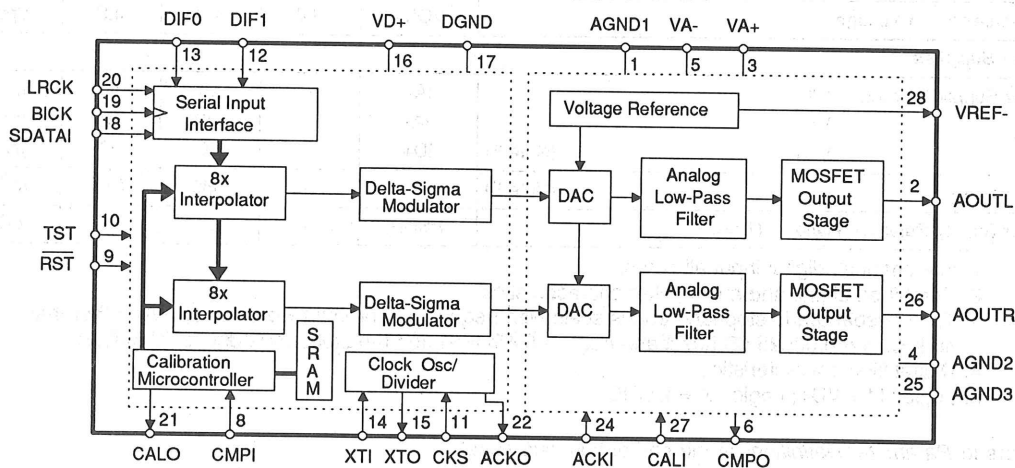
The CS4328 is a complete stereo digital-to-analog output system. In addition to the traditional D/A function, the CS4328 includes an 8x digital interpolation filter followed by a 64x oversampled delta-sigma modulator. The modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 kHz and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4328 also includes an extremely flexible serial port utilizing two select pins to support four different interface modes.

The master clock can be either 256 or 384 times the input word rate, supporting various audio environments.

## ORDERING INFORMATION:

CS4328-KP	0 to 70 °C	28-pin Plastic DIP
CS4328-KS	0 to 70 °C	28-pin Plastic SOIC



**ANALOG CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ;  $V_{A+}, V_{D+} = 5\text{V}$ ;  $V_{A-} = -5\text{V}$ ; Full-Scale Output Sinewave, 991 Hz; Input Word Rate = 48 kHz; Input Data = 18 Bits; BICK = 3.072 MHz;  $R_L = 10\text{k}\Omega$ ; Measurement Bandwidth is 10 Hz to 20 kHz, unweighted; unless otherwise specified.)

Parameter*	Symbol	Min	Typ	Max	Units
<b>Dynamic Performance</b>					
Signal-to-Noise Ratio (A-weighted) (Note 1)	SNR	120	-	-	dB
Total Harmonic Distortion + Noise (A-Weighted)	THD+N	-	-93	-90	dB
0 dB Output,		-	-77	-73	dB
-20 dB Output,		-	-37	-33	dB
-60 dB Output,		-			
Deviation From Linear Phase (Note 2)	-	-	$\pm 0.5$	-	deg
Passband: to -3 dB corner (Notes 3, 4)	-	0	to	23.5	kHz
to 0.00025 dB corner (Notes 3, 4)	-	0	to	21.6	kHz
Passband Ripple (Note 4)	-	-	-	0.00025	dB
StopBand (Note 3)	-	26.4	-	-	kHz
StopBand Attenuation (Note 2)	-	90	-	-	dB
Group Delay (IWR = Input Word Rate)	tg $\delta$	-	33/IWR	-	s
Interchannel Isolation (1 kHz)	-	-100	-110	-	dB
<b>dc Accuracy</b>					
Interchannel Gain Mismatch	-	-	0.1	-	dB
Gain Error	-	-	-	$\pm 5$	%
Gain Drift	-	-	150	-	ppm/ $^\circ\text{C}$
Offset Error (after calibration)	-	-	-	$\pm 1$	mV
<b>Analog Output</b>					
Full Scale Output Voltage	V <sub>OUT</sub>	3.8	4.0	4.2	V <sub>pp</sub>
<b>Power Supplies</b>					
Power Supply Current: V <sub>A+</sub>	I <sub>A+</sub>	-	40	55	mA
V <sub>A-</sub>	I <sub>A-</sub>	-	-40	-55	mA
V <sub>D+</sub> (Note 5)	I <sub>D+</sub>	-	50	60	mA
Power Dissipation (Note 5)	-	-	650	850	mW
Power Supply Rejection Ratio (1 kHz)	PSRR	-	50	-	dB

- Notes:
1. Idle channel, digital input all zeros.
  2. Combined digital and analog filter characteristics.
  3. The passband and stopband edges scale with frequency. For input word rates, IWR, other than 48 kHz, the 0.00025 dB passband edge is  $0.45 \times \text{IWR}$  and the stopband edge is  $0.55 \times \text{IWR}$ .
  4. Digital filter characteristics.
  5. Logic "1" = V<sub>D+</sub>; Logic "0" = DGND.

\* Refers to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.



## DIGITAL CHARACTERISTICS

(TA = 25 °C; VA+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V <sub>IH</sub>	70%VD+	-	-	V
Low-Level Input Voltage	V <sub>IL</sub>	-	-	30%VD+	V
High-Level Output Voltage at I <sub>O</sub> = -20μA	V <sub>OH</sub>	4.4	-	-	V
Low-Level Output Voltage at I <sub>O</sub> = 20μA	V <sub>OL</sub>	-	-	0.1	V
Input Leakage Current (Note 6)	I <sub>in</sub>	-	-	1.0	μA

Note: 6. TST, DIF0 & DIF1 have internal pull-down devices, nominally 90kΩ.

## ABSOLUTE MAXIMUM RATINGS (AGND1-3, DGND = 0V, all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supplies:				
Positive Digital	VD+	-0.3	6.0	V
Positive Analog	VA+	-0.3	6.0	V
Negative Analog	VA-	0.3	-6.0	V
VA+  -  VD+		-	0.4	V
Input Current, Any Pin Except Supplies	I <sub>in</sub>	-	±10	mA
Digital Input Voltage	V <sub>IND</sub>	-0.3	(VD+)+0.4	V
Ambient Operating Temperature (power applied)	T <sub>A</sub>	-55	125	°C
Storage Temperature	T <sub>stg</sub>	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device  
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(AGND1, AGND2, AGND3, DGND = 0V; all voltages with respect to ground)

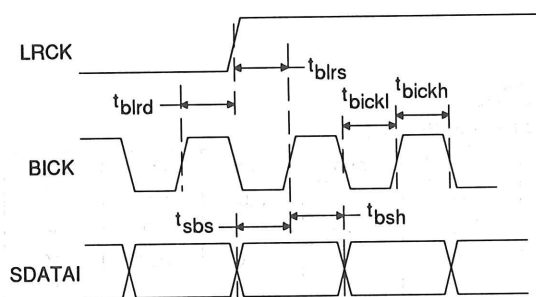
Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:					
Positive Digital	VD+	4.75	5.0	5.25	V
Positive Analog	VA+	4.75	5.0	5.25	V
Negative Analog	VA-	-4.75	-5.0	-5.25	V
VA+  -  VD+		-	-	0.4	V

# SWITCHING CHARACTERISTICS

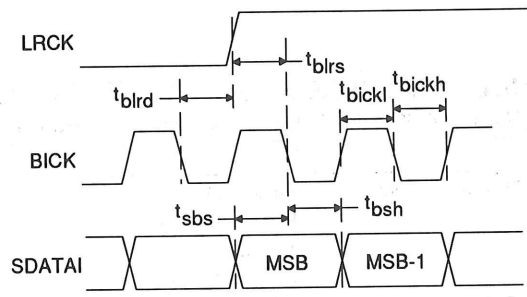
( $T_A = 25\text{ }^\circ\text{C}$ ;  $V_{A+}, V_{D+} = 5V \pm 5\%$ ;  $V_{A-} = -5V \pm 5\%$ ; Inputs: Logic 0 = 0V, Logic 1 =  $V_{D+}$ ,  $C_L = 20\text{ pF}$ )

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency using Internal Oscillator:					
CKS=H	XTI/XTO	10.7	-	19.2	MHz
CKS=L	-	7.1	-	13.9	MHz
Master Clock Frequency using External Clock:					
CKS=H	XTI/XTO	0.384	-	19.2	MHz
CKS=L	-	0.256	-	13.9	MHz
XTI/XTO Pulse Width Low	-	21	-	-	ns
XTI/XTO Pulse Width High	-	21	-	-	ns
BICK Pulse Width Low	$t_{bickl}$	30	-	-	ns
BICK Pulse Width High	$t_{bickh}$	30	-	-	ns
BICK Period	$t_{bickw}$	80	-	-	ns
BICK rising to LRCK edge delay	(Note 7) $t_{blr d}$	35	-	-	ns
BICK rising to LRCK edge setup time	(Note 7) $t_{blr s}$	35	-	-	ns
SDATAI valid to BICK rising setup time	(Note 7) $t_{sbs}$	35	-	-	ns
BICK rising to SDATAI hold time	(Note 7) $t_{bsh}$	35	-	-	ns
$\overline{\text{RST}}$ Minimum Pulse Width Low	2 periods of XTI/XTO				

Note: 7. "BICK rising" refers to modes 0, 1, and 3. For mode 2, replace "BICK rising" with "BICK falling."



Serial Input Timing (Modes 0, 1, & 3)



Serial Input Timing (Mode 2)

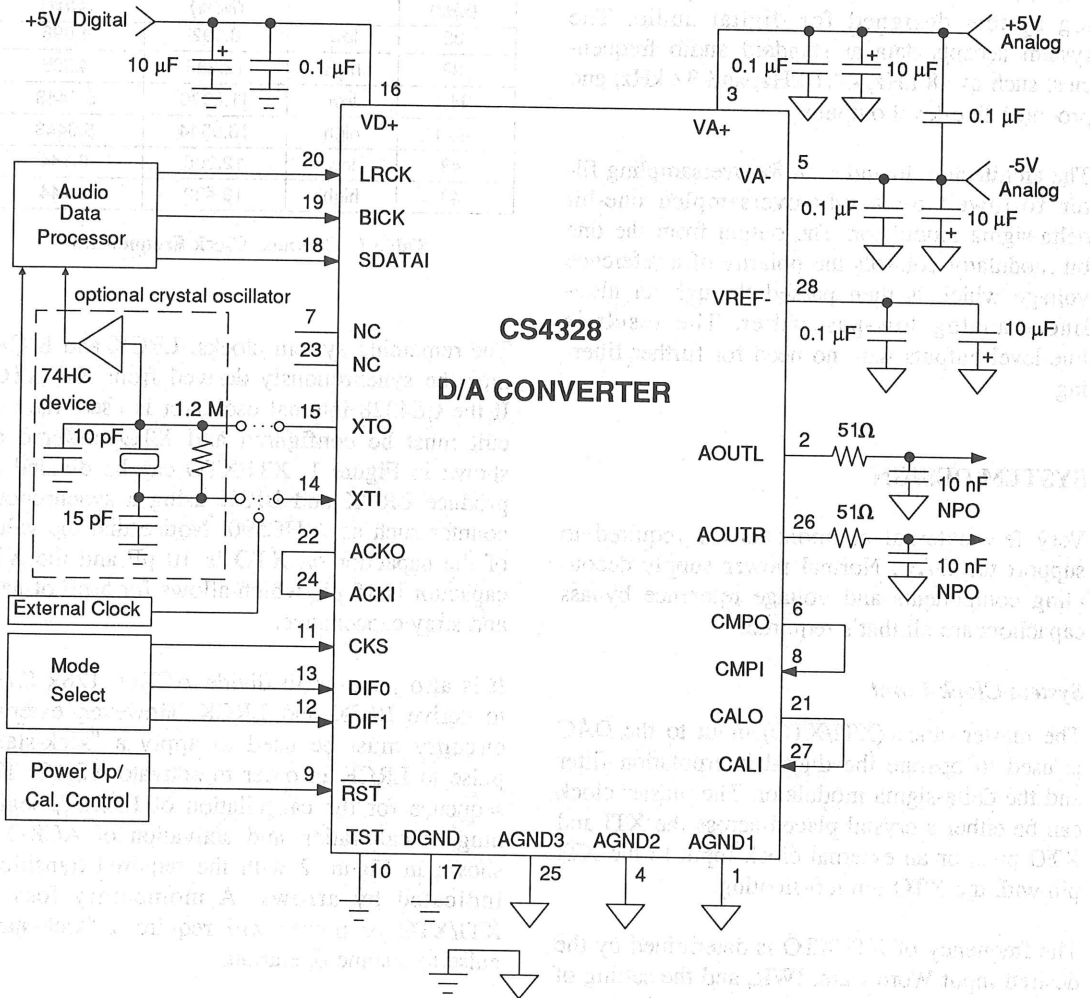


Figure 1. Typical Connection Diagram

## GENERAL DESCRIPTION

The CS4328 is a complete stereo digital-to-analog system designed for digital audio. The system accepts data at standard audio frequencies, such as 48 kHz, 44.1 kHz, and 32 kHz; and produces line-level outputs.

The architecture includes an 8× oversampling filter followed by a 64× oversampled one-bit delta-sigma modulator. The output from the one bit modulator controls the polarity of a reference voltage which is then passed through an ultra-linear analog low-pass filter. The result is line-level outputs with no need for further filtering.

## SYSTEM DESIGN

Very few external components are required to support the DAC. Normal power supply decoupling components and voltage reference bypass capacitors are all that's required.

### System Clock Input

The master clock (XTI/XTO) input to the DAC is used to operate the digital interpolation filter and the delta-sigma modulator. The master clock can be either a crystal placed across the XTI and XTO pins, or an external clock input to the XTI pin with the XTO pin left floating.

The frequency of XTI/XTO is determined by the desired Input Word Rate, IWR, and the setting of the Clock Select pin, CKS. IWR is the frequency at which words for each channel are input to the DAC and is equal to LRCK frequency. Setting CKS low selects an XTI/XTO frequency of 256× IWR while setting CKS high selects 384× IWR. The ACKO pin will always be 128× IWR and is used by the analog low-pass smoothing filter. Table 1 illustrates various audio word rates and corresponding frequencies used in the DAC.

LRCK (kHz)	CKS	XTI/XTO (MHz)	ACKO (MHz)
32	low	8.192	4.096
32	high	12.288	4.096
44.1	low	11.2896	5.6448
44.1	high	16.9344	5.6448
48	low	12.288	6.144
48	high	18.432	6.144

Table 1. Common Clock Frequencies

The remaining system clocks, LRCK and BICK, must be synchronously derived from XTI/XTO. If the CS4328 internal oscillator is used, the circuit must be configured and XTO buffered as shown in Figure 1. XTI/XTO can be divided to produce LRCK and BICK using a synchronous counter such as 74HC590. Notice that the value of the capacitor on XTO is 10 pF and the XTI capacitor is 15 pF, which allows for 5 pF of gate and stray capacitance.

It is also possible to divide ACKO, 128× IWR, to derive BICK and LRCK. However, external circuitry must be used to apply a "kick-start" pulse to LRCK in order to activate ACKO. The sequence for the cancellation of RESET, beginning of calibration and activation of ACKO is shown in Figure 2 with the required transitions indicated by arrows. A momentary loss of XTI/XTO or power will require a "kick-start" pulse to resume operation.

### Serial Data Interface

Data is input to the CS4328 via three serial input pins; SDATAI is the serial data input, BICK is the serial data clock and LRCK defines the channel and delineation of data. The DAC supports four serial data formats which are selected via the digital input format pins DIF0 and DIF1. The different formats control the relationship of LRCK to SDATAI and the edge of BICK used to

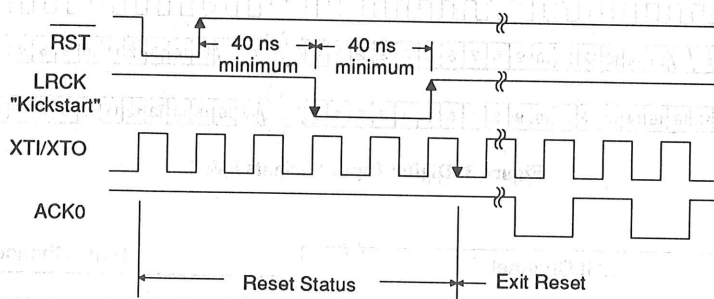


Figure 2. RESET Cancellation Timing

latch data. Table 2 lists the four formats, along with the associated figure number. Format 0 is compatible with existing 16-bit D/A converters and digital filters. Format 1 is an 18-bit version of format 0. Format 2 is similar to Crystal ADCs and many DSP serial ports. Format 3 is compatible with the I<sup>2</sup>S serial data protocol. Formats 2 and 3 support 18-bit input or 16-bit followed by two zeros. In all four serial input modes, the serial data is MSB-first and 2's-complement format.

Formats 0, 2 and 3 will operate with 16-bit data and 16 BICK pulses as well. See Figure 6 for 16-bit timing. However, the use of BICK = 64 × IWR is recommended to minimize the possibility of performance degradation resulting from BICK coupling into VREF.

DIF1	DIF0	Mode	Figure
0	0	0	3
0	1	1	3
1	0	2	4
1	1	3	5

Table 2. Digital Input Formats

### Reset and Offset Calibration

$\overline{\text{RST}}$  is an active low signal that resets the digital filter and the delta-sigma modulator, synchronizes LRCK with internal control signals and starts an offset calibration cycle upon exiting reset. When  $\overline{\text{RST}}$  goes low, CALO goes high and stays high until the end of an offset calibration cycle. An offset calibration cycle takes 1024 IWR cycles to complete. CALO must be connected to CALI and CMPO must be connected to CMPI for offset calibration. During an offset calibration the analog output is forced to zero.

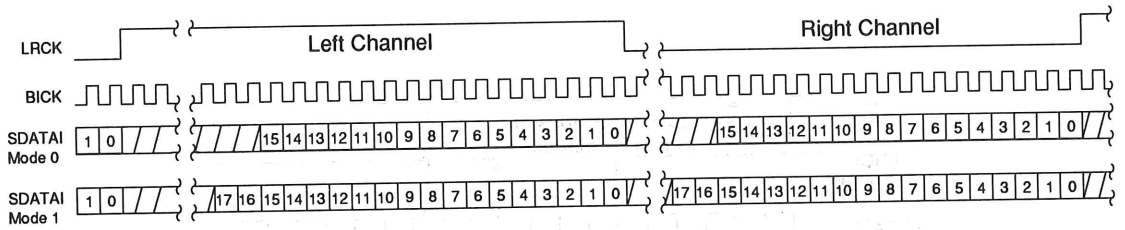
### Power-Up Considerations

Upon initial application of power to the DAC, offset calibration and digital filter registers will be indeterminate.  $\overline{\text{RST}}$  should be low during power-up to activate an internal mute and prevent this erroneous information from being output from the DAC. Bringing  $\overline{\text{RST}}$  high will begin a calibration cycle and initialize these registers.

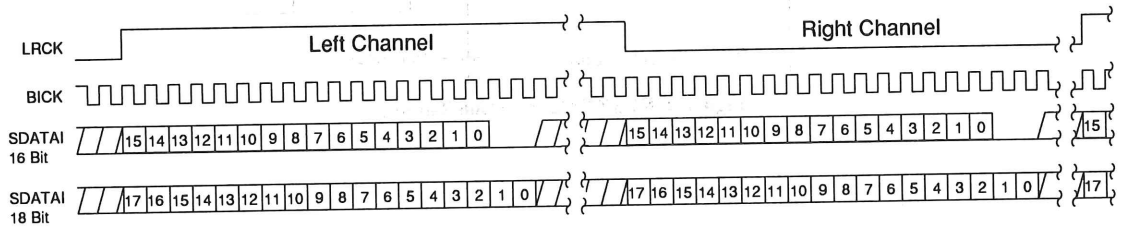
### Muting

There are two types of mutes that can be implemented with the CS4328. The first is a -50 dB

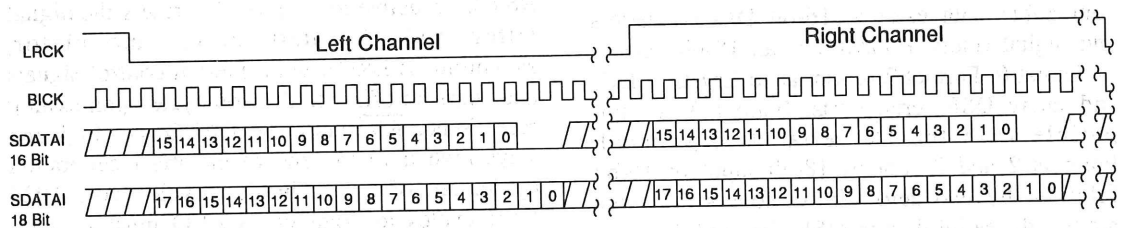




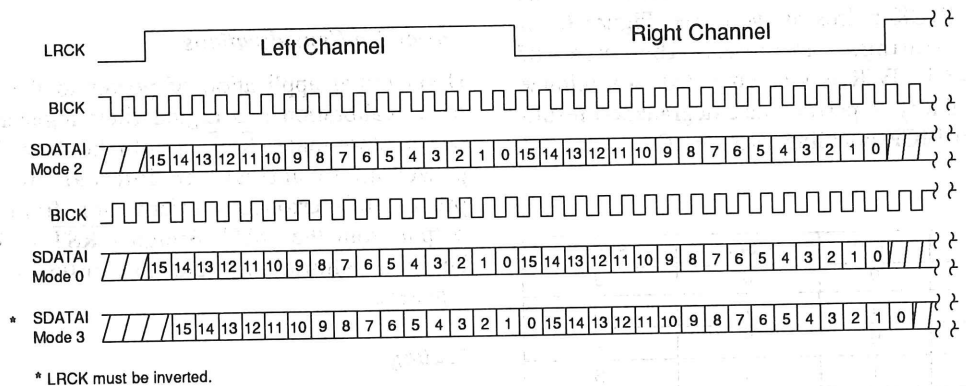
**Figure 3. Digital Input Formats 0 & 1**



**Figure 4. Digital Input Format 2**



**Figure 5. Digital Input Format 3**



\* LRCK must be inverted.

**Figure 6. Digital Input Formats 0, 2 and 3 with 16 BICK Periods**

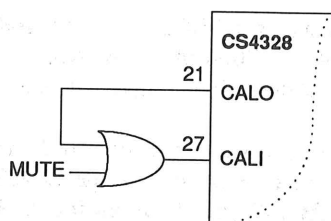


Figure 7. -50dB Muting

mute which can be activated by forcing the CALI pin high. Figure 7 shows how to implement a -50 dB mute using an OR gate. The propagation of the gate will be the only delay in moving the CS4328 to a muted state.

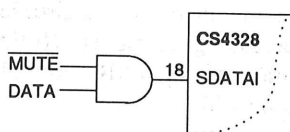


Figure 8. -120 dB Muting

The second mute option is a two stage operation which involves forcing SDATAI to 0 using an AND gate as shown in Figure 8. The first mute occurs following 33 LRCK cycles when the 0 input data propagates to the output of the DAC. The rms noise present at the output will typically be 93 dB below fullscale. Following a total of 4096 LRCK cycles with 0 input data the output of the CS4328 will mute and lower the output rms noise to a minimum of 120 dB below fullscale. Upon release of the MUTE command and non-zero input data the CS4328 output mute will immediately release. However, 33 LRCK cycles are required for input data to propagate to the output of the CS4328.

### Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4328 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 1 shows the recommended power arrangements with VA+ connected to a clean +5 volt supply and VA- connected to a

clean -5 volt supply. VD+, which powers the digital interpolation filter and delta-sigma modulator, may be powered from the system +5 volt logic supply. Decoupling capacitors should be located as near to the CS4328 as possible.

The printed circuit board layout should have separate analog and digital regions with individual ground planes. The CS4328 should straddle the ground plane break as shown on the CDB4328 Evaluation board. Optional jumpers for connecting these planes should be included near the DAC, where power is brought on to the board and near the regulators. All signals, especially clocks, should be kept away from the VREF- pin to avoid unwanted coupling into the CS4328. The VREF- decoupling capacitors, particularly the 0.1  $\mu$ F, must be positioned to minimize the electrical path from VREF- to Pin 1 AGND and to minimize the path between VREF- and the capacitors. Extensive use of ground plane fill on both the analog and digital sections of the circuit board will yield large reductions in radiated noise effects. An application note "Layout and Design Rules for Data Converters" is printed in the Application Note section of this book.

### Analog Output and Filtering

Full scale analog output for each channel is typically 4V peak-to-peak. The analog outputs can drive load impedances as low as 600 $\Omega$  and are short-circuit protected to 20mA.

The CS4328 analog filter is a 5th order switched-capacitor filter followed by a second-order continuous-time filter. The switched-capacitor filter is clock dependent and will scale with the IWR frequency. The continuous-time filter is fixed and not related to IWR. A low-pass filter consisting of a 51 $\Omega$  resistor and a .01  $\mu$ F NPO capacitor is recommended on the analog outputs.

## Performance Plots

The following collection of CS4328 measurement plots (IWR = 48 kHz) were taken with an Audio Precision Dual Domain System One. All FFT plots are 16,384 point.

Figure 9 shows the **frequency response** with a 48 kHz input word rate. The response is very flat out to half the input word rate.

Figure 10 shows the **muted noise** with all zeros data into the CS4328. This plot is dominated by the noise floor of the System One.

Figure 11 shows the **unmuted noise**. This data was taken by feeding the CS4328 continuous zeros, but pulling CALI low. This unmutes the output stage of the CS4328. This plot shows the noise shaping characteristics of the delta-sigma modulator combined with the analog filter.

Figure 12 shows the **A-weighted THD+N vs signal amplitude** for a dithered 1kHz input signal. Notice that there is no increase in distortion as the signal level decreases. This indicates very good low-level linearity, one of the key benefits of the delta-sigma technique.

Figure 13 shows the **fade-to-noise linearity** test result using track 20 of the CBS CD-1. The input test signal is a dithered 500 Hz sine wave which gradually fades from -60 dB level to -120 dB. During the fading, the output level from the CS4328 is measured and compared to the ideal level. Notice the very close tracking of the output level to the ideal, even at low level inputs of -90 dB. The gradual shift of the plot away from zero at signal levels < -100 dB is caused by the background noise starting to dominate the measurement.

Figure 14 shows the **impulse response**, taken from the single positive full scale value on track 17 of the CD-1 test disk. Notice the high degree of symmetry, indicating good phase linearity.

Figure 15 shows a **16K FFT plot result, with a 1 kHz -90 dB dithered input**. Notice the complete lack of distortion components and tones.

Figure 16 shows a **bandlimited, 10 Hz to 22 kHz, time domain plot** of the CS4328 output with a **1 kHz, -90 dB dithered input**. Notice the clear residual sine wave shape, in the presence of noise.

Figure 17 shows the **monotonicity test** result plot. The input data to the CS4328 is +1 LSB, -1 LSB four times, then +2 LSB, -2 LSB four times and so on, until +10 LSB, -10 LSB. This data pattern is taken from track 21 of the CD-1 test disk. Notice the increasing staircase envelope, with no decreasing elements. Notice also the clear resolution of the LSB. For this test, one LSB is a 16-bit LSB.

The following tests were done by filtering the analog output of the CS4328 with the System One analyzer 1 kHz notch filter to reduce the peak signal level. The resulting signal was then amplified and applied to the DSP module, avoiding distortion in the System One A/D converter.

Figure 18 shows a **16K FFT Plot with a 1 kHz, 0 dB input**. Notice the low order harmonic distortion at < -100 dB.

Figure 19 shows a **16K FFT Plot with a 1 kHz, -10 dB input**. Notice the almost complete absence of distortion, with a small residual 2nd harmonic at -110 dB.

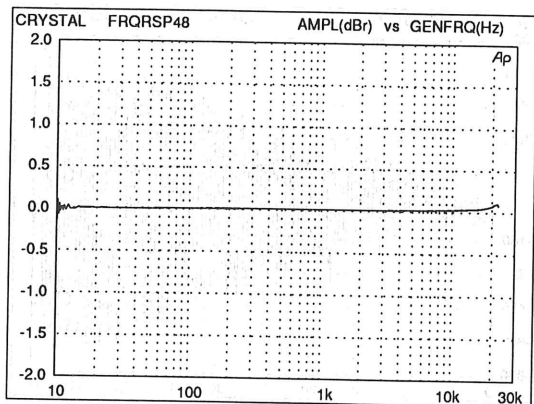


Figure 9. Frequency Response (48 kHz word rate)

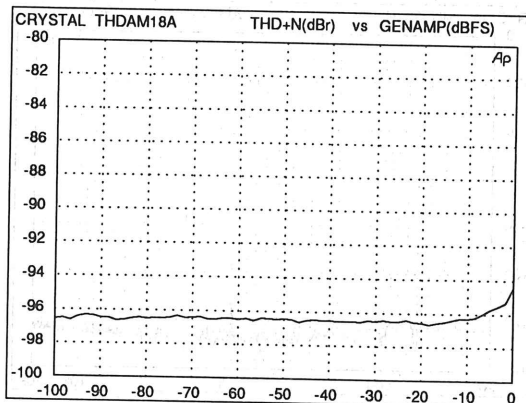


Figure 12. THD+N vs 18-bit Input Signal Level

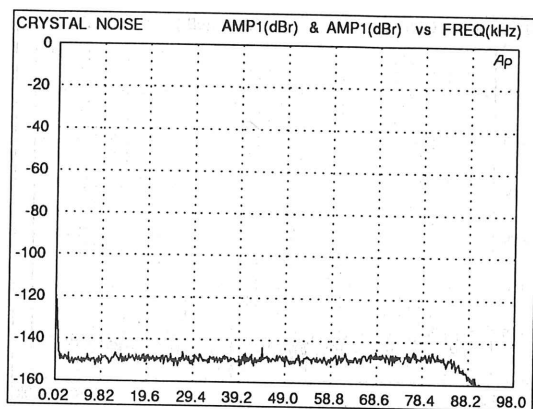


Figure 10. Muted Idle Channel Noise

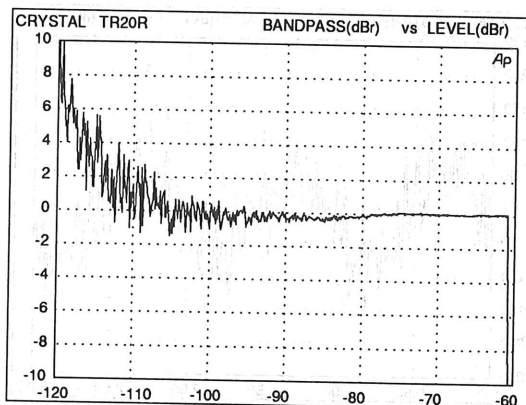


Figure 13. Fade-to-Noise Linearity

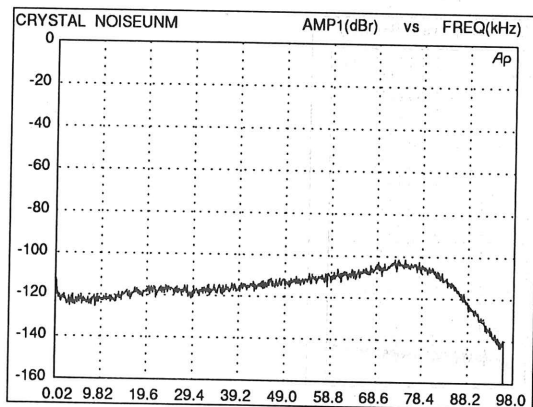


Figure 11. Unmuted Idle Noise

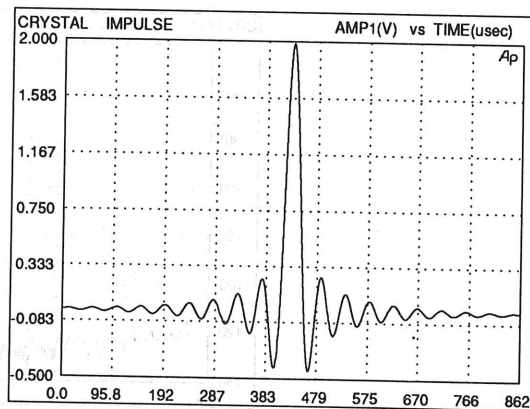
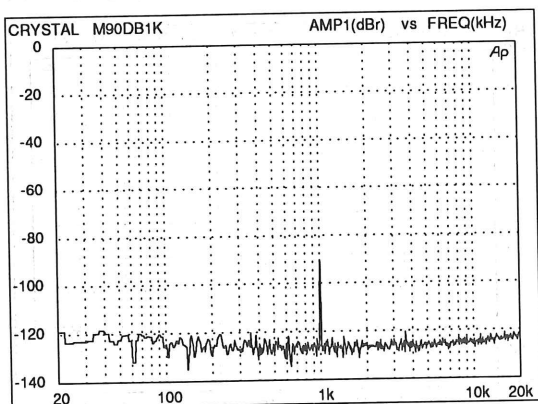
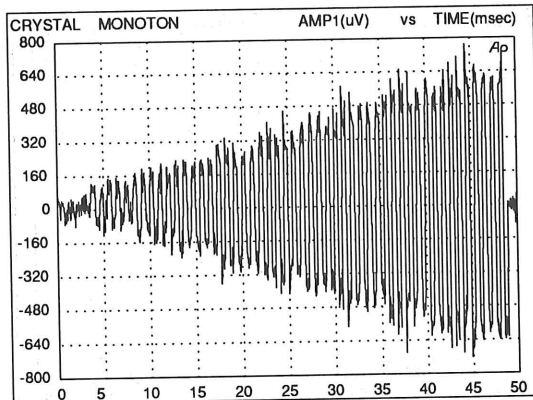


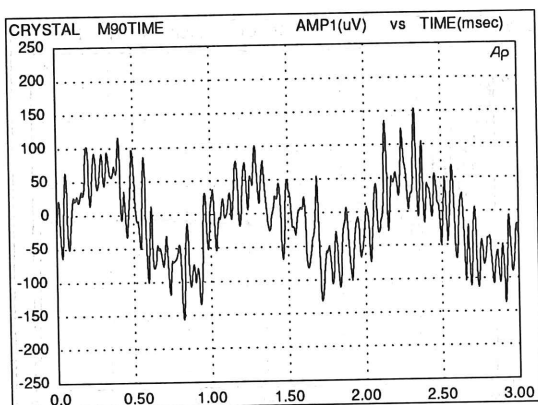
Figure 14. Impulse Response



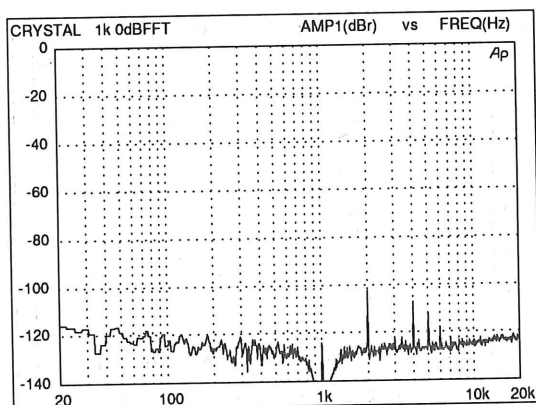
**Figure 15. 1 kHz, -90 dB Input FFT Plot**



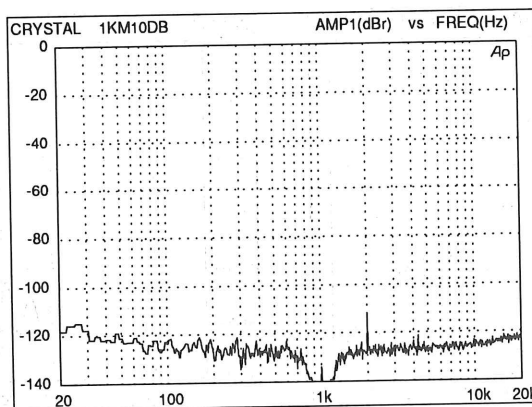
**Figure 17. Monotonicity Test (16-bit data)**



**Figure 16. 1 kHz, -90 dB Input Time Domain Plot**



**Figure 18. 1 kHz, 0 dB Input FFT Plot**



**Figure 19. 1 kHz, -10 dB Input FFT Plot**

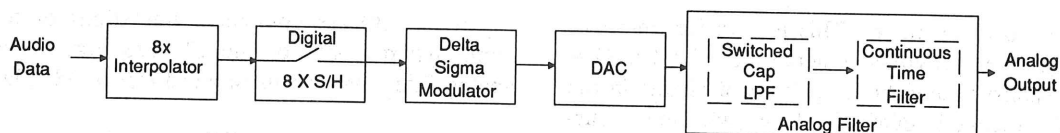


Figure 20. CS4328 Architecture

2

### THEORY OF OPERATION

The CS4328 architecture can be considered in five blocks: Interpolation, sample/hold, delta-sigma modulation, D/A conversion, and analog filtering.

Audio data is input to the CS4328 digital interpolation filter which removes images of the input signal that are present at multiples of the input sample frequency,  $F_s$  (Figure 21). Following the interpolation stage, the resulting frequency spectrum has images of the input signal at multiples of eight times the input sample frequency,  $8 \times F_s$  (Figure 22). Eliminating the images between  $F_s$  and  $8 \times F_s$  greatly relaxes the requirements of the analog filtering, allowing the suppression of images while leaving the audio band of interest unaltered.

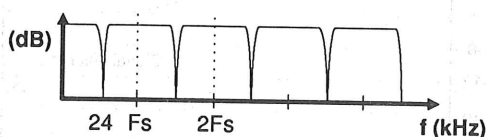


Figure 21. Input Data Spectrum

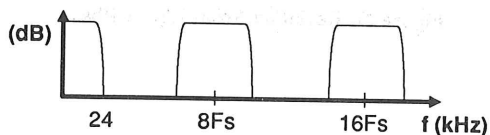


Figure 22. 8X Interpolated Data Spectrum

The CS4328 interpolation stage is followed by a sample-and-hold function where the data points from the interpolator are held for eight ( $64 \times F_s$ ) clock cycles. The resulting frequency response is a  $\text{sinc}/x$  characteristic with zeros at  $8 \times F_s$  multiples. The  $\text{sinc}/x$  zeros completely attenuate

signals at  $8 \times F_s$  and largely suppress the remaining energy of the images (Figure 23). The  $8 \times$  interpolation followed by the  $8 \times$  sample-and-hold results in data at a rate of  $64 \times F_s$ .

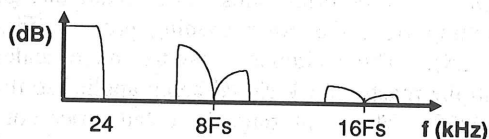


Figure 23. Spectrum After S/H

The delta-sigma modulator takes in the  $64 \times F_s$  data (3.072 MHz for 48kHz sampled systems) and performs fifth-order noise shaping. In the digital modulator of the CS4328, 18-bit audio data is modulated to a 1-bit,  $64 \times F_s$  signal. The 5th-order noise shaper allows 1-bit quantization to support 18-bit audio processing by suppressing quantization noise in the bandwidth of interest. Figure 24 shows the frequency spectrum of the modulator output.

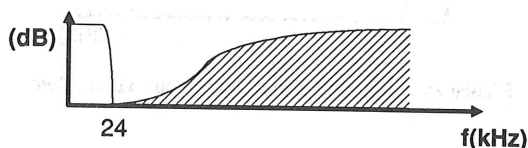


Figure 24. Modulator Output Spectrum

The CS4328's digital modulator is followed by a D-to-A converter that translates the 1-bit signal into a series of charge packets. The magnitude of the charge in each packet is determined by sampling of a voltage reference onto a switched capacitor, where the polarity of each packet is controlled by the 1-bit signal. The result is a 1-bit D/A conversion process that is very insen-



sitive to clock jitter. This is a major improvement over previous generations of 1-Bit D/A converters where the magnitude of charge in the D/A process is determined by switching a current reference for a period of time defined by periods of the master clock.

The final stage of the CS4328 is made up of a 5th order switched-capacitor low pass filter and a 2nd order continuous time filter. The switched-capacitor filter eliminates out-of-band energy resulting from the noise shaping process (Figure 25). The switched-capacitor stage scales with the master clock signal being applied to the CS4328. The final stage is a 2nd order continuous time filter that eliminates high frequency energy that appears at multiples of the  $64 \times F_s$  sample rate (Figure 26).

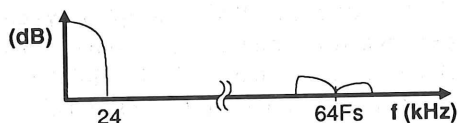


Figure 25. Spectrum After Switched-Capacitor Filter



Figure 26. Spectrum After Continuous Time Filter

Figures 27-30 are computer simulations of the combined response of the CS4328 digital and analog filters with an input word rate of 48 kHz.

Figure 27 shows the individual and combined phase response of the CS4328 filters. Notice the digital filter equalization of the analog filter to produce a linear phase response.

Figures 28-30 are plots of the CS4328 magnitude response.

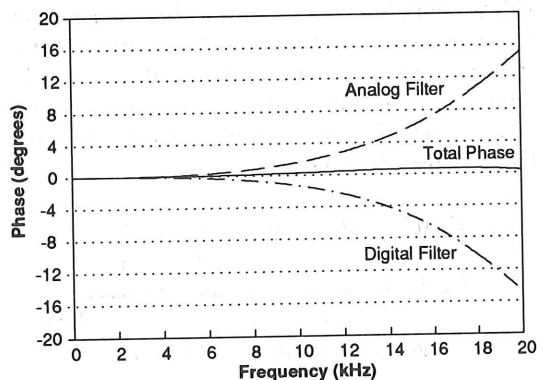
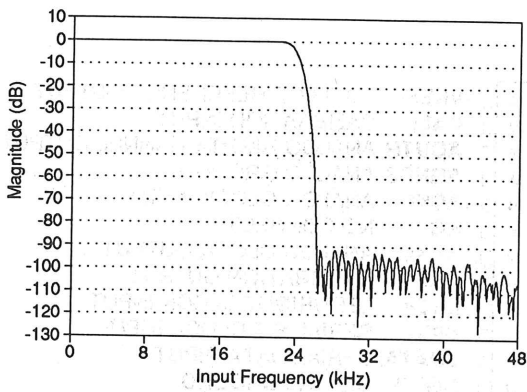
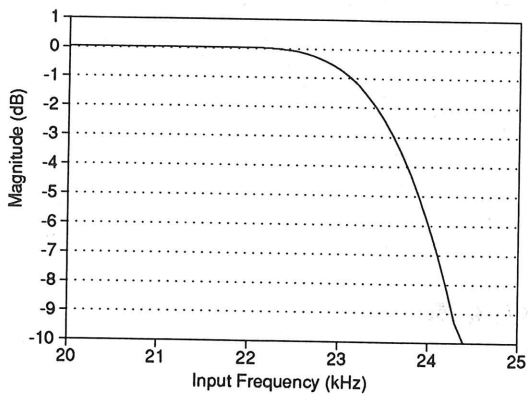


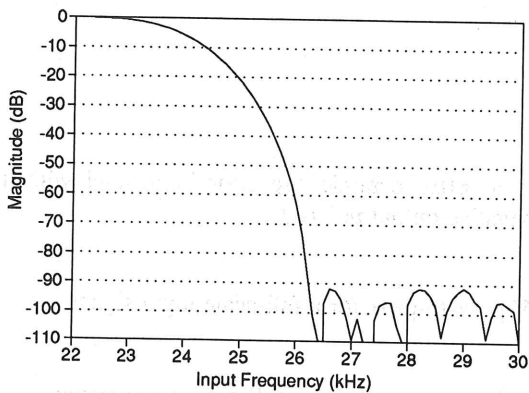
Figure 27. Deviation From Linear Phase



**Figure 28. Combined Digital and Analog Filter Frequency Response**



**Figure 29. Combined Digital and Analog Filter Frequency Response**



**Figure 30. Combined Digital and Analog Filter Transition Band**

## **PIN DESCRIPTIONS**

ANALOG GROUND	<b>AGND1</b>	1	28	<b>VREF-</b>	VOLTAGE REFERENCE OUTPUT
ANALOG LEFT CHANNEL OUTPUT	<b>AOUTL</b>	2	27	<b>CALI</b>	CALIBRATION INPUT
ANALOG POWER	<b>VA+</b>	3	26	<b>AOUTR</b>	ANALOG RIGHT CHANNEL OUTPUT
ANALOG GROUND	<b>AGND2</b>	4	25	<b>AGND3</b>	ANALOG GROUND
NEGATIVE ANALOG POWER	<b>VA-</b>	5	24	<b>ACKI</b>	ANALOG CLOCK INPUT
COMPARATOR OUTPUT	<b>CMPO</b>	6	23	<b>NC</b>	NO CONNECT
NO CONNECT	<b>NC</b>	7	22	<b>ACKO</b>	ANALOG CLOCK OUTPUT
COMPARATOR INPUT	<b>CMPI</b>	8	21	<b>CALO</b>	CALIBRATION OUTPUT
RESET	<b>RST</b>	9	20	<b>LRCK</b>	LEFT/RIGHT CLOCK INPUT
TEST	<b>TST</b>	10	19	<b>BICK</b>	SERIAL BIT CLOCK INPUT
CLOCK SELECT	<b>CKS</b>	11	18	<b>SDATAI</b>	SERIAL DATA INPUT
DIGITAL INPUT FORMAT 1	<b>DIF1</b>	12	17	<b>DGND</b>	DIGITAL GROUND
DIGITAL INPUT FORMAT 0	<b>DIF0</b>	13	16	<b>VD+</b>	DIGITAL POWER
CRYSTAL OR CLOCK INPUT	<b>XTI</b>	14	15	<b>XTO</b>	CRYSTAL OSCILLATOR OUTPUT

### **Power Supply Connections**

#### **VA+ - Positive Analog Power, PIN 3.**

Positive analog supply. Nominally +5 volts.

#### **VA- - Negative Analog Power, PIN 5.**

Negative analog supply. Nominally -5 volts.

#### **AGND1, AGND2, AGND3 - Analog Grounds, PINS 1, 4, 25.**

Analog ground reference.

#### **VD+ - Positive Digital Power, PIN 16.**

Positive supply for the digital section. Nominally +5 volts.

#### **DGND - Digital Ground, PIN 17.**

Digital ground for the digital section.

### **Analog Outputs**

#### **VREF- - Voltage Reference Output, PIN 28.**

Nominally -3.68 volts. Normally connected to a 0.1 $\mu$ F ceramic capacitor in parallel with a 10 $\mu$ F or larger electrolytic capacitor. Note the negative output polarity.

#### **AOUTL - Analog Left Channel Output, PIN 2.**

Analog output for the left channel. Typically 4V peak-to-peak for a full-scale input signal.

#### **AOUTR - Analog Right Channel Output, PIN 26.**

Analog output for the right channel. Typically 4V peak-to-peak for a full-scale input signal.

### Digital Inputs

#### XTI - Crystal or Clock Input, PIN 14.

A crystal oscillator can be connected between this pin and XTO, or an external CMOS clock can be input on XTI. The frequency must be either 256× or 384× the input word rate based on the clock select pin, CKS.

#### ACKI - Analog Clock Input, PIN 24.

This is the master clock input for the analog section of the chip and must be 128× the input word rate. ACKI is typically connected to the Analog Clock Output pin, ACKO.

#### CALI - Calibration Input, PIN 27.

Input to the analog section that is used during offset calibration. Normally connected to the Calibration Output pin, CALO.

#### CMPI - Comparator Input, PIN 8

Input to the digital section that is used during offset calibration. Normally connected to the Comparator Output pin, CMPO.

#### LRCK - Left/Right Clock, PIN 20.

This input determines which channel is currently being input on the Serial Data Input pin, SDATAI. The format of LRCK is controlled by DIF0 and DIF1.

#### BICK - Serial Bit Input Clock, PIN19.

Clocks the individual bits of the serial data in from the SDATAI pin. The edge used to latch SDATAI is controlled by DIF0 and DIF1.

#### SDATAI - Serial Data Input, PIN 18.

Two's complement MSB-first serial data of either 16 or 18 bits is input on this pin. The data is clocked into the CS4328 via the BICK clock and the channel is determined by the LRCK clock. The format for the previous two clocks is determined by the Digital Input Format pins, DIF0 and DIF1.

#### DIF0,DIF1 - Digital Input Format, PINS 13, 12

These two pins select one of four formats for the incoming serial data stream. These pins set the format of the BICK and LRCK clocks with respect to SDATAI. The formats are listed in Table 2.

#### CKS - Clock Speed Select, PIN 11.

Selects the clock frequency input on the XTI pin. CKS low selects 256× the input word rate (LRCK frequency) while CKS high selects 384×.

#### RST - Reset and Calibrate, PIN 9.

When reset is low the filters and modulators are held in reset. When reset goes high, an offset calibration is initiated.

**Digital Outputs****XTO - Crystal Oscillator Output, PIN 15.**

When a crystal oscillator is used, it is tied between this pin and XTI. When an external clock is input, this pin should be left floating.

**ACKO - Analog Clock Output, PIN 22.**

This output is  $128\times$  the input word rate (LRCK frequency). Normally connected to the Analog Clock Input pin, ACKI.

**CALO - Calibration Output, PIN 21.**

Used during offset calibration. Must be connected to the Calibration Input pin, CALI.

**CMPO - Comparator Output, PIN 6.**

Used during offset calibration. Must be connected to the Comparator Input pin, CMPI.

**Miscellaneous****NC - No Connection, PINS 7, 23.**

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

**TST -Test Input, PIN 10.**

Allows access to the CS4328 test modes, which are reserved for factory use. Must be tied to DGND.

## PARAMETER DEFINITIONS

2

**Total Harmonic Distortion + Noise** - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

**Signal-to-Noise Ratio** - The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth with an input of all zeros.

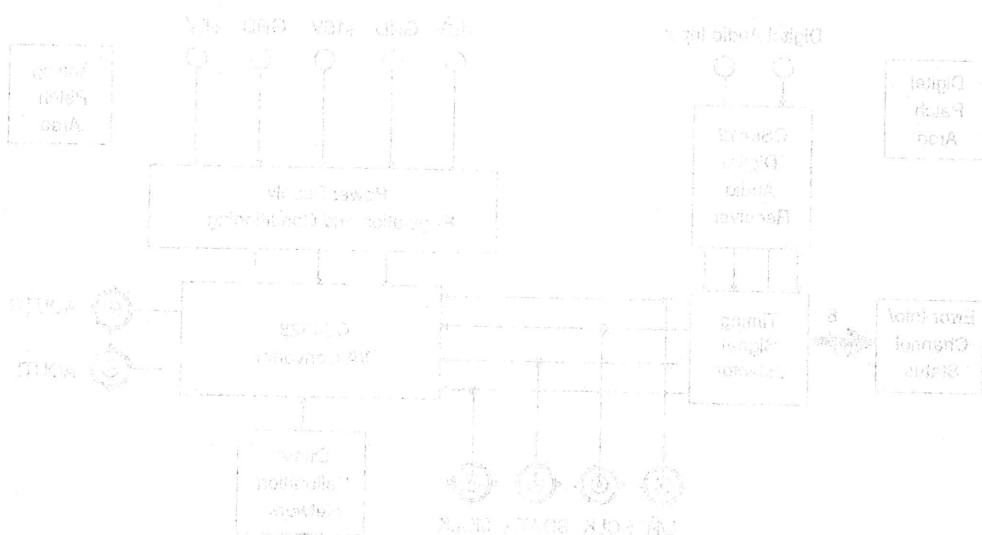
**Interchannel Isolation** - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

**Interchannel Gain Mismatch** - The gain difference between left and right channels. Units in decibels.

**Gain Error** - The deviation from the nominal full scale analog output for a full scale digital input.

**Gain Drift** - The change in gain value with temperature. Units in ppm/°C.

**Offset Error** - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (AGND). Units in mV.





## CS4328 Evaluation Board

### Features

- Demonstrates recommended layout and grounding arrangements
- CS4328 Supports multiple input formats
- CS8412 Receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Digital and Analog Patch Areas
- Operation with on-board CS8412 or externally supplied system timing

### General Description

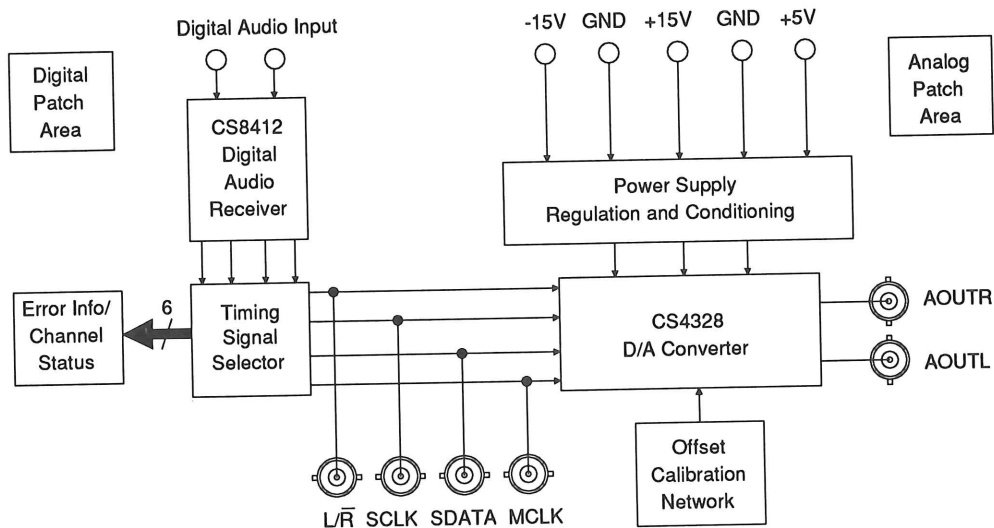
The CDB4328 evaluation board allows fast evaluation of the CS4328 18-bit, stereo D/A converter. The board provides an analog output interface via BNC connectors for both channels. Evaluation requires an analog signal analyzer, a digital signal source, and a power supply.

Also included is a CS8412 digital audio receiver I.C., which will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The CS8412 can provide the system timing necessary to operate the CS4328.

The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

**ORDERING INFORMATION:** CDB4328

### Block Diagram



## Power Supply Circuitry

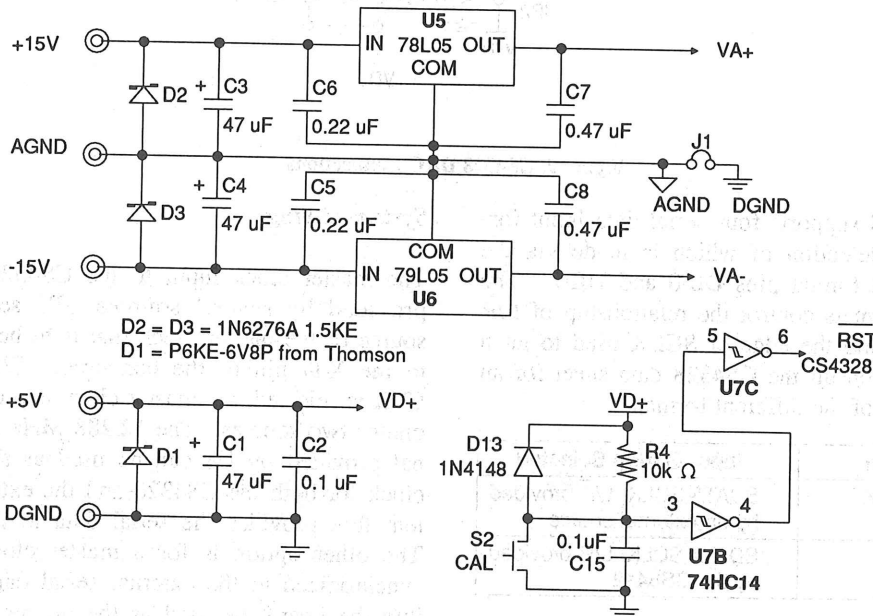
Figure 1 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by five binding posts. The  $\pm 5$  V analog power supply inputs of the converter are derived from  $\pm 15$  V using the voltage regulators U5 and U6. The +5 V digital supply for the converter and the discrete logic on the board is provided by the +5 V and DGND binding posts. D1, D2, and D3 are transient suppressors which also provide protection from incorrectly connected power supply leads. C1-C8 provide general power supply filtering for the analog supplies. As shown in Figure 2, C20-C24 provide localized decoupling for the converter VA+ and VA- pins. Note that C22 is connected between VA- and VA+ and not VA- and AGND. The evaluation board uses both an analog and a digital ground plane which are connected at J1. This ground plane arrangement isolates the board's digital logic from the analog circuitry.

## Offset Calibration & Reset Circuitry

Figure 1, shows the offset calibration circuit provided on the evaluation board. Upon power-up, this circuit provides a pulse on the Digital to Analog Converter's  $\overline{\text{RST}}$  pin initiating an offset calibration cycle. Pressing and releasing S2 also initiates an offset calibration cycle.

## Serial Data Interface

Figure 1 shows that there are two options for inputting serial data into the CS4328. Serial data can be provided via the SDATA BNC connector on the evaluation board. BNC connectors for SCLK, the serial data input clock, and  $\text{L}/\overline{\text{R}}$ , the clock that defines the channel and delineates the data, are also provided on the evaluation board. This information can also be provided by the on-board CS8412. JP3 selects the source of SDATA, SCLK, and  $\text{L}/\overline{\text{R}}$  that will be provided to the converter. JP3 selections are shown in Table 1.



**Figure 1. Power Supply and Reset Circuitry**

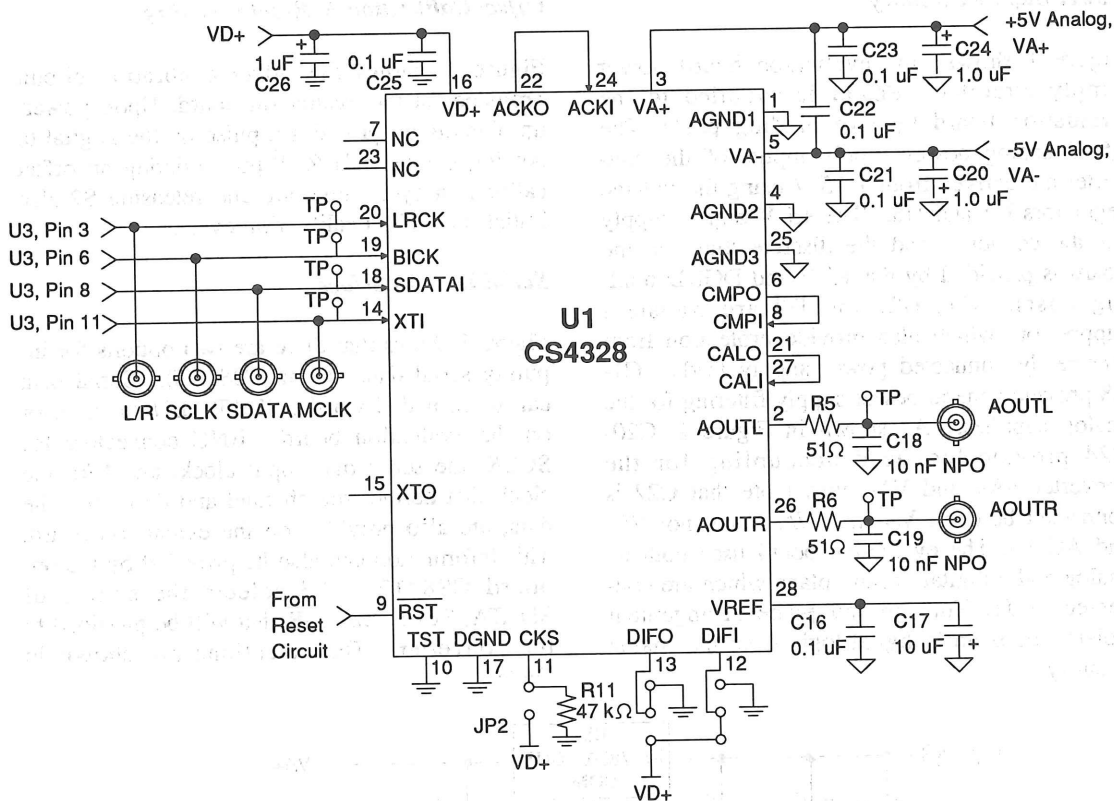


Figure 2. CS4328 DAC Connections

The CS4328 supports four serial data input formats. The selection of which is made via the digital input format pins DIF0 and DIF1. The different formats control the relationship of L/R to SDATA and the edge of SCLK used to latch the data. Consult the CS4328 data sheet for an explanation of the different formats.

Position	Input Option Selected
EXT CLK	SDATA,SCLK, L/R provided by an external source.
8412	SDATA,SCLK, L/R provided by the CS8412

Table 1. JP3 Selectable Options

### System Timing

The master clock input to the CS4328 can be provided by several sources. JP3 selects the source of the master clock that is to be supplied to the XTI pin of the converter. When EXT CLK is selected, the master clock is provided by one of two sources. The 12.288 MHz clock signal provided by U8 can be used as the master clock for both the CS4328 and the external system that provides the serial data to the board. The other option is for a master clock that is synchronized to the external serial data coming into the board, be used as the master clock for the CS4328 as well. However, if an external

master clock is to be used, U8 must be removed from its socket to prevent the two clock signals from interfering with one another. When 8412 is selected by JP3, the master clock for the CS4328 is provided by the MCK output of the CS8412. The CKS pin of the CS4328 can be pulled either high or low via JP2. This determines whether the master clock frequency has to be 384X or 256X the input word rate. Consult the CS4328 data sheet for the common master clock frequencies table.

### Analog Outputs

The analog outputs are available at 2 BNC connectors labeled AOUTL and AOUTR. R5 and C18 remove the remaining very high frequency components from the left channel output signal while R6 and C19 do so for the right channel output signal.

### Digital Audio Standard Interface

Included on the evaluation board is a CS8412 Digital Audio Interface Receiver. This device can receive and decode data according to the AES/EBU, S/PDIF, and EIAJ-340 interface standard. Figure 3 shows the schematic for the CS8412. The input is coupled to the device through a transformer that is included on the board. The input to the device can be configured to accept either professional or consumer input modes. Consult the CS8412 data sheet for an explanation of the two input modes.

The LEDs, D4-D8, perform two functions. When S1 is in the Channel Status position, the LEDs display the channel status information for the channel selected by JP1. When S1 is in the Error Information position, the LEDs D4-D6, display encoded error information that can be decoded by consulting the CS8412 data sheet. Encoded sample frequency information is displayed on LEDs D7-D9 provided a proper clock is being applied to the FCK pin of JP1. When an LED is lit, this indicates a "1" on the cor-

responding pin located on the CS4328. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L or R option should be selected if the FCK pin of JP1 is being driven by a clock signal.

### Serial Output Interface

The SDATA, SCLK, L/R, and MCLK BNC connectors can also be used to provide a serial output interface for the CS8412. With JP3 in the 8412 position, the outputs from the CS8412 can be brought off the board to an external evaluation system. This data can be configured in one of seven selectable formats. These formats are outlined in the CS8412 data sheet.

### CDB5336/7/8/9 Interface to CDB4328

Many users find it informative to evaluate a combined ADC and DAC system connected together yielding analog input and analog output. This can be accomplished by interconnecting a CDB5326/7/8/9 or CDB5336/7/8/9 to a CDB4328 evaluation board. The following information contains several techniques to accomplish this goal. There are two general points which need to be mentioned. An analog input of  $\pm 3.68$  V will produce a full scale digital output from the CS5336/7/8/9 and the CS5326/7/8/9. A full scale digital input to the CS4328 will produce a full scale output of  $\pm 2$  V resulting in an overall loss of approximately 5.2 dB from input to output. Also it is recommended that the power connections for each board are brought directly from the power supply and not in a "daisy-chain" manner from board to board.

Connecting the CDB4328 to the CDB5336/7/8/9 can be accomplished using one of two methods:

#### CDB4328 to CDB5336/7/8/9 - Method 1

This method uses the AES/EBU Digital Audio Interface which is supported by the CS8402

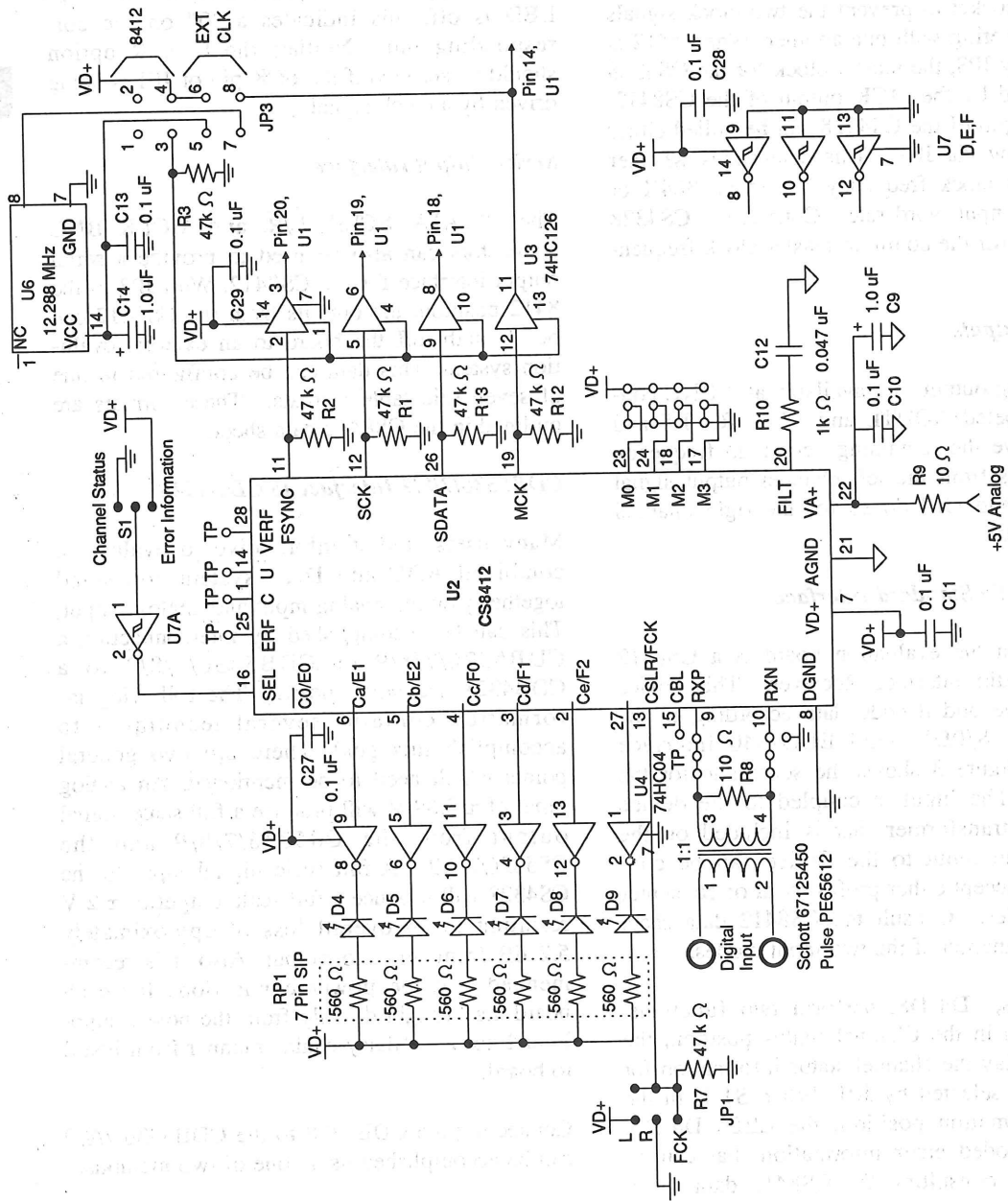


Figure 3. CS8412 Digital Audio Receiver Connections

AES/EBU Transmitter and the CS8412 AES/EBU Receiver. The data and clock information is transmitted from the CDB5336/7/8/9 to the CDB4328 via this interface.

### *CDB4328 Configuration for Method 1*

The CS8412 is configured to output data in Format 0 (M0, M1, M2 and M3 low) and the CDB4328 must be set to receive data in the corresponding Format 2 (DIF1 high and DIF0 low). Modify the jumpers located near pins 12 and 13 of the CS4328. Please note that Format 0 for the CS8412 corresponds to the Format 2 for the CS4328. JP2 sets the clock to sample frequency ratio (CKS) on the CS4328 and is set low for a ratio of 256.

JP3 selects the source of SDATA, SCLK and L/R that will be provided to the converter and should be in the 8412 position to allow the CDB4328 to access the multiple clocks generated from the CS8412 and disable the oscillator U8.

### *CDB5336/7/8/9 Configuration for Method 1*

P4 selects an option to invert the SCLK for the CS8402 and the parallel interface. The positions of P4 are labeled and the jumpers should be in the appropriate position for the ADC being used. P7 should be set to "internal" to allow the use of the master clock on the CDB5336/7/8/9. CMODE is set low for a master clock to sample rate ratio of 256.

### *CDB5336/7/8/9 and CDB4328 Interconnection for Method 1*

Interconnection requires the power supply connections and a shielded twisted pair cable connecting the digital outputs from the CDB5336/7/8/9 to the digital inputs on the CDB4328.

### *CDB4328 to CDB5336/7/8/9 - Method 2*

Method 2 of interfacing the CDB5336/7/8/9 and the CDB4328 requires a direct interface through the EXTCLKIN, SCLK, SDATA, and L/R BNC connectors. This technique also requires minor modifications to the CDB5336/7/8/9.

### *CDB4328 Configuration for Method 2*

The CS4328 is set to accept data in format 3 (DIF0 and DIF1 high). JP2 sets the clock to sample frequency ratio (CKS) on the CS4328 (pin 11) is set low for a ratio of 256.

JP3 selects the source of SDATA, SCLK and L/R that will be provided to the converter and should be removed to access the multiple clocks from the CDB5336/7/8/9 and disable the oscillator U8.

A left channel input will appear as a right channel output in this configuration. To correct this the L/R clock must be inverted prior to the CS4328 L/R input. This can be implemented by modifying the CDB4328 as follows: Cut the trace at the L/R BNC connector on the CDB4328. Cut the trace at U7 pin 9. Place a jumper between U7 pin 9 and the L/R BNC. Place a jumper between U7 pin 8 and U1 pin 20.

### *CDB5336/7/8/9 Configuration for Method 2*

The CS5336/7/8/9 data output contains 16 bits of audio data as well as 3 tag bits and a left/right indicator. These additional bits need to be removed before transmission to the CDB4328. This can be done by making use of the FSYNC pulse which frames the audio data bits. This has been implemented on the CDB5336/7/8/9 and can be utilized with a minor modification: cut the trace at the SDATA BNC connector and place a jumper between the SDATA BNC and U8 pin 11. CMODE is set LOW for a master clock of 256 times the sample rate. P7 must have both the internal and external jumpers in-



stalled. This will route the master clock to the EXTCLKIN BNC for connection to the CDB4328 MCLK.

If a CS5336/8 is installed an additional modification is required to invert the SCLK prior to transmission to the CDB4328. This can be implemented as follows: cut the trace at the SCLK BNC and install a jumper between U7 pin 4 and the SCLK BNC.

#### *CDB5336/7/8/9 and CDB4328 Interconnection for Method 2*

Shielded coaxial cables with BNC connectors should be used to make the following connections: L/R to L/R, SCLK to SCLK, SDATA to SDATA, EXTCKIN to MCLK.

#### *CDB4328 Interfacing to the CDB5326/7/8/9*

A method of interfacing the CDB5326/7/8/9 and the CDB4328 requires a direct interface through the EXTCLKIN, SCLK, SDATA, and L/R BNC connectors. This technique requires modifications to the CDB5326/7/8/9 to derive the proper clock frequencies. This is done by utilizing a 12.288 MHz clock and supplying a clock to the CDB5326/7/8/9 at 6.144 MHz.

#### *CDB4328 Configuration*

The CS4328 must be set to receive data in format 2 (DIF1 high and DIF0 low). Modify the jumpers located near pins 12 and 13 of the CS4328. JP2 sets the clock to sample frequency ratio (CKS) on the CS4328 and is set low for a 256 ratio.

JP3 selects the source of SDATA, SCLK and L/R that will be provided to the converter and should be removed to access the multiple clocks from the CDB5326/7/8/9. Remove the 12.288 MHz oscillator (U8).

#### *CDB5326/7/8/9 Configuration*

Remove the clock source jumper (P2). Remove the 6.144 MHz oscillator (U2) and replace with the 12.288 MHz oscillator from the CDB4328.

Install a divide by 2 function on the CDB5326/7/8/9 digital patch area. Use a 74HC74 with the D input connected to the Q output. Connect the oscillator output to the 74HC74 clock input. Connect the Q output to U1 pin 23.

Position P2 to connect the oscillator output to the EXTCLKIN.

#### *CDB5326/7/8/9 and CDB4328 Interconnection*

Shielded coaxial cables with BNC connectors should be used to make the following connections: L/R to L/R, SCLK to SCLK, SDATA to SDATA, EXTCLKIN to MCLK.

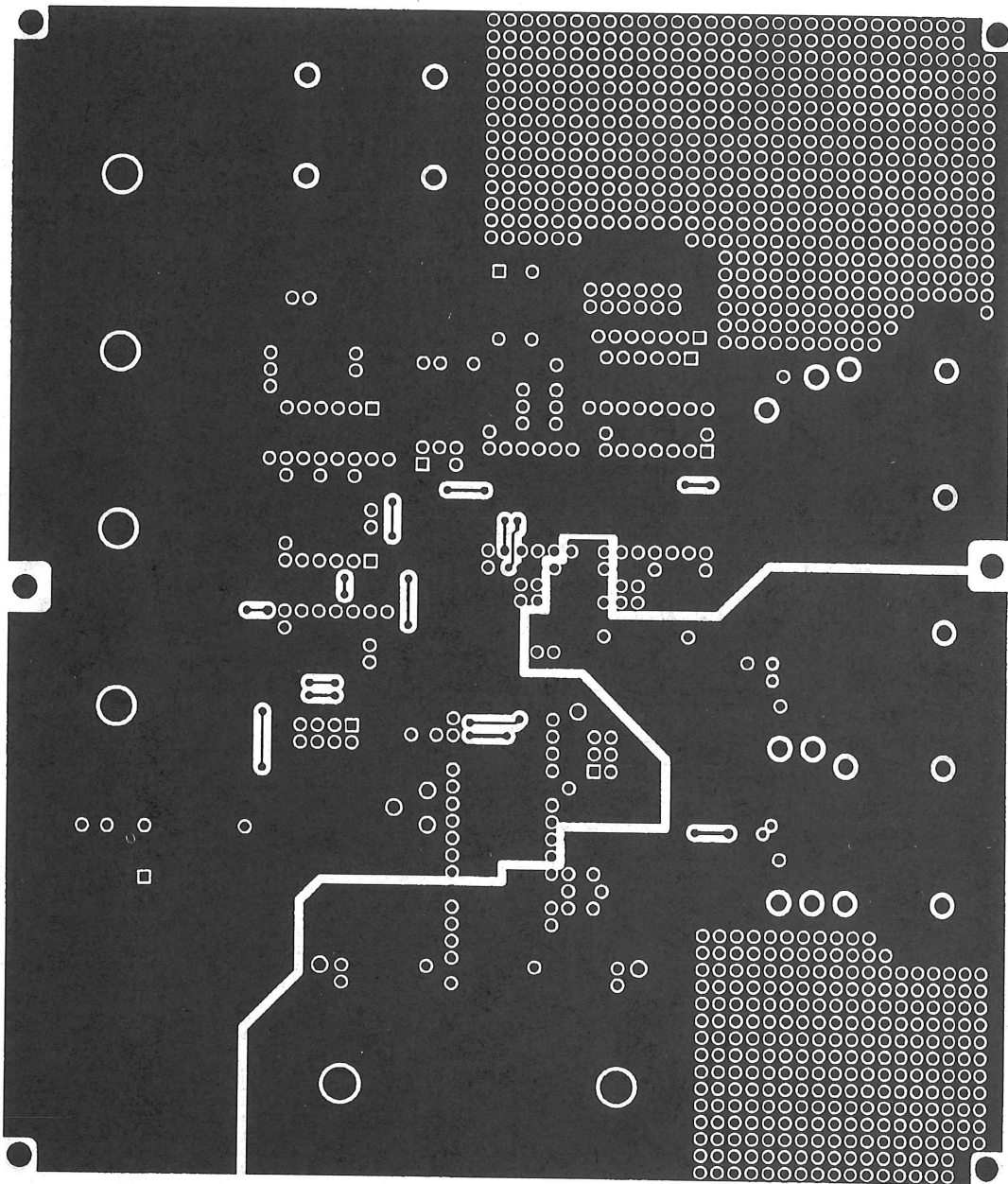


Figure 4. Top Ground Plane Layer (NOT TO SCALE)

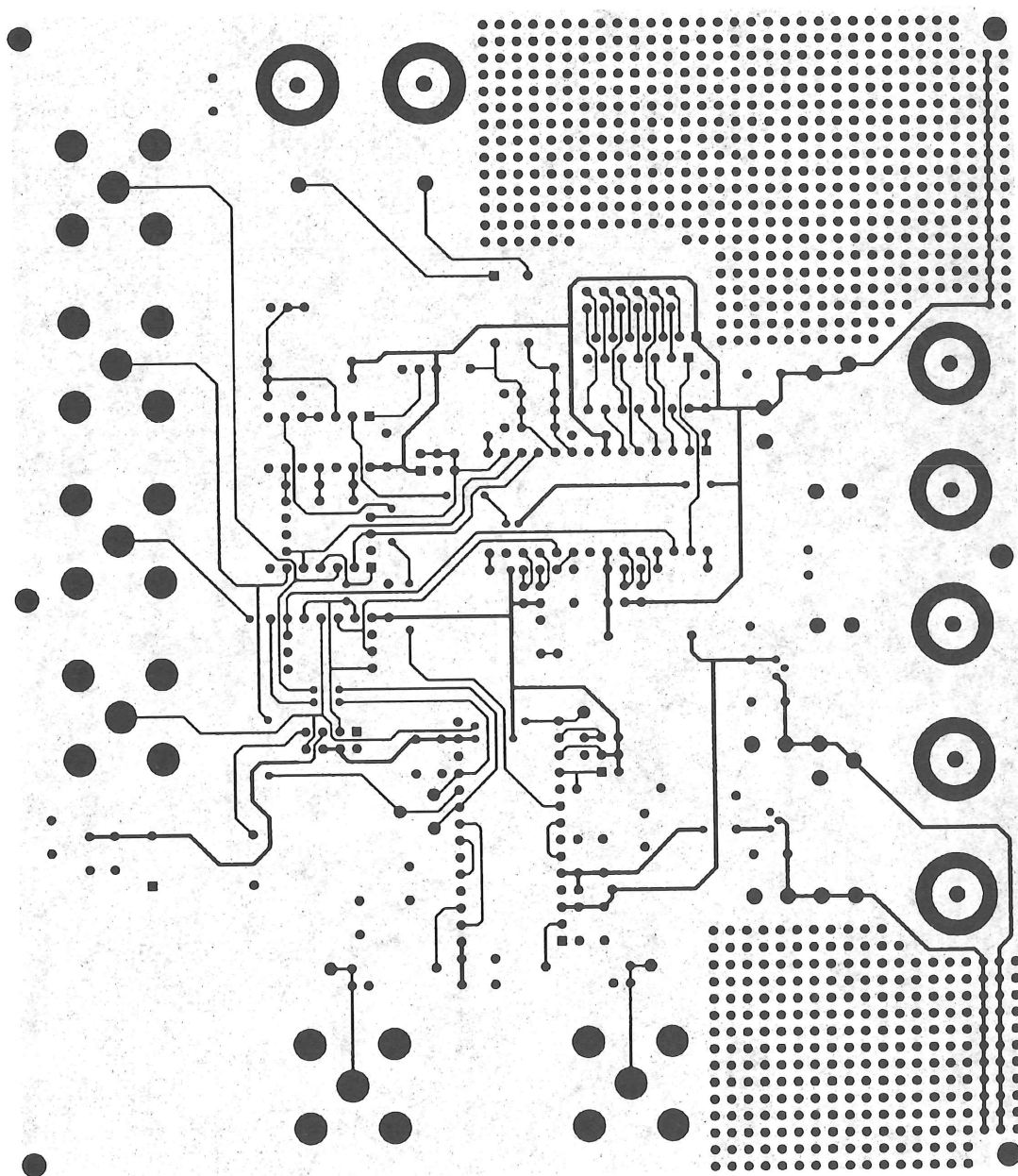
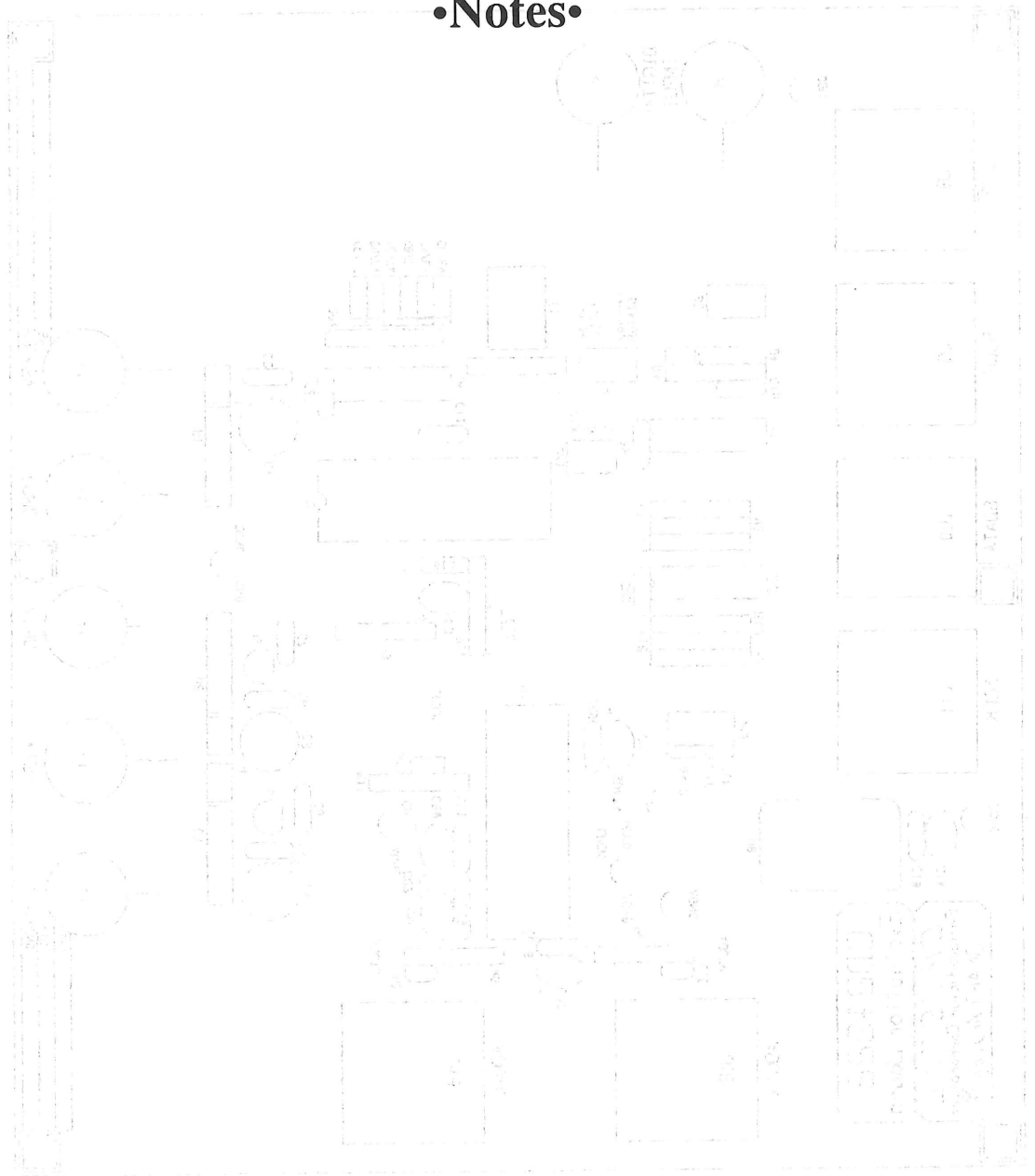


Figure 5. Bottom Trace Layer (NOT TO SCALE)



•Notes•



(This is a preliminary drawing and is not for production)

# 16-Bit, Stereo A/D Converter for Digital Audio

## Features

- Monolithic CMOS A/D Converter  
Inherent Sampling Architecture  
Stereo or Monaural Capability  
Serial Output
- Monaural Sampling Rates up to 100 kHz  
50 kHz/Channel Stereo Sampling
- Signal-to-(Noise+Distortion): 92 dB
- Dynamic Range: 92 dB  
95dB in 2X Oversampling Schemes
- Interchannel Isolation: 90 dB
- 2's Complement or Binary Coding
- Low Power Dissipation: 260 mW  
Power Down Mode for Portable Applications
- Evaluation Board Available

## General Description

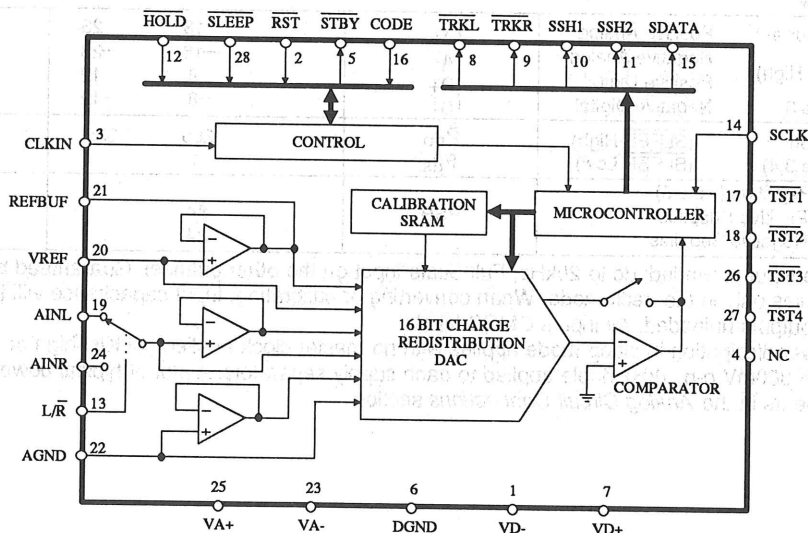
The CS5126 CMOS analog-to-digital converter is an ideal front-end for stereo or monaural digital audio systems. The CS5126 can be configured to handle two channels at up to 50kHz sampling per channel, or it can be configured to sample one channel at rates up to 100kHz.

The CS5126 executes a successive approximation algorithm using a charge redistribution architecture. On-chip self-calibration circuitry has 18-bit resolution thus avoiding any degradation in performance with low-level signals. The charge redistribution technique also provides an inherent sampling function which avoids the need for external sample/hold amplifiers.

Signal-to-(noise+distortion) in stereo operation is 92dB, and is dominated by internal broadband noise (1/2 LSB rms). When the CS5126 is configured for 2X oversampling, digital post-filtering bandlimits this white noise to 20kHz, increasing dynamic range to 95dB.

## ORDERING INFORMATION:

CS5126-KP	0 °C to 70 °C	(was CSZ5126-KP)
CS5126-KL	0 °C to 70 °C	28-Pin Plastic DIP
		28-Pin PLCC





**ANALOG CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ;

$V_{A+}, V_{D+} = 5\text{V}$ ;  $V_{A-}, V_{D-} = -5\text{V}$ ; Full-Scale Input Sinewave, 1kHz;  $f_{\text{clk}} = 24.576\text{MHz}$ ;  $V_{\text{REF}} = 4.5\text{V}$ ;  
 Analog Source Impedance = 200 $\Omega$ ; Stereo operation,  $L/\bar{R}$  toggling at 48 kHz unless otherwise specified.)

Parameter*	Symbol	CS5126-KP			Units
		min	typ	max	
Resolution				16	Bits
<b>Dynamic Performance</b>					
Signal-to-(Noise plus Distortion)					
$V_{\text{IN}} = \pm\text{FS}$ (10Hz to 20kHz)	$S/(N+D)$	90	92		dB
$V_{\text{IN}} = -20\text{dB}$ ( $f = 20\text{kHz}$ )		70	72		dB
Total Harmonic Distortion	THD		0.001		%
Dynamic Range Stereo Mode	DR	90	92		dB
Monaural (20kHz BW)			95		dB
Idle Channel Noise	$V_{n(\text{ic})}$		1/2		LSB rms
Interchannel Isolation (Note 1)	$I_{\text{ic}}$	88	90		dB
Interchannel Mismatch	$M_{\text{ic}}$		0.01		dB
<b>dc Accuracy</b>					
Full-Scale Error	FSE		$\pm 4$		LSB
Bipolar Offset Error	BPO		$\pm 4$		LSB
<b>Analog Input</b>					
Aperture Time	$t_{\text{apt}}$		30		ns
Aperture Jitter	$t_{\text{ajt}}$		100		ps
Input Capacitance (Note 2)	$C_{\text{in}}$		200		pF
<b>Power Supplies</b>					
Power Supply Current	Positive Analog	$I_{A+}$	18	23	mA
(SLEEP High)	Negative Analog	$I_{A-}$	-18	-23	mA
(Note 3)	Positive Digital	$I_{D+}$	8	12	mA
	Negative Digital	$I_{D-}$	-8	-12	mA
Power Dissipation	(SLEEP High)	$P_{\text{do}}$	260	350	mW
(Notes 3,4)	(SLEEP Low)	$P_{\text{ds}}$	1		mW
Power Supply Rejection (Note 5)					
Positive Supplies	PSR		84		dB
Negative Supplies			84		dB

- Notes:
1. One input grounded; dc to 20kHz, Full Scale input on the other channel. Guaranteed by characterisation
  2. Applies only in the track mode. When converting or calibrating, input capacitance will typically be 10 pF
  3. All outputs unloaded. All inputs CMOS levels.
  4. Power dissipation in sleep mode applies with no master clock applied (CLKIN high or low).
  5. With 300mV p-p, 1kHz ripple applied to each supply separately. A plot of typical power supply rejection appears in the *Analog Circuit Connections* section.

Specifications are subject to change without notice.

# DIGITAL CHARACTERISTICS (T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>; V<sub>A+</sub>, V<sub>D+</sub> = 5V±10%; V<sub>A-</sub>, V<sub>D-</sub> = -5V±10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V <sub>IH</sub>	2.0	-	-	V
Low-Level Input Voltage	V <sub>IL</sub>	-	-	0.8	V
High-Level Output Voltage (Note 6)	V <sub>OH</sub>	V <sub>D+</sub> - 1.0V	-	-	V
Low-Level Output Voltage I <sub>out</sub> =1.6mA	V <sub>OL</sub>	-	-	0.4	V
Input Leakage Current - CLKIN pin	I <sub>in</sub>	-	-	10	µA
Input Leakage Current - Except CLKIN pin	I <sub>in</sub>	-	-	TBD	µA

Note: 6. I<sub>OUT</sub> = -100 µA. This specification guarantees that each digital output will drive one TTL load (V<sub>OH</sub> = 2.4V @ I<sub>OUT</sub> = -40 µA).

# RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 7.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	V <sub>D+</sub>	4.5	5.0	V <sub>A+</sub>	V
Negative Digital	V <sub>D-</sub>	-4.5	-5.0	-5.5	V
Positive Analog	V <sub>A+</sub>	4.5	5.0	5.5	V
Negative Analog	V <sub>A-</sub>	-4.5	-5.0	-5.5	V
Analog Reference Voltage	V <sub>REF</sub>	2.5	4.5	V <sub>A+</sub> - 0.5	V
Analog Input Voltage: (Note 8)	V <sub>AIN</sub>	-V <sub>REF</sub>	-	V <sub>REF</sub>	V

Notes: 7. All voltages with respect to ground.

8. The CS5126 can accept input voltages up to the analog supplies (V<sub>A+</sub>, V<sub>A-</sub>). It will produce an output of all 1's for inputs above V<sub>REF</sub> and all 0's for inputs below -V<sub>REF</sub>.

# ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive Digital	V <sub>D+</sub>	-0.3	V <sub>A+</sub> + 0.3	V
Negative Digital	V <sub>D-</sub>	0.3	-6.0	V
Positive Analog	V <sub>A+</sub>	-0.3	6.0	V
Negative Analog	V <sub>A-</sub>	0.3	-6.0	V
Input Current, Any Pin Except Supplies (Note 9)	I <sub>in</sub>	-	±10	mA
Analog Input Voltage (AIN and V <sub>REF</sub> pins)	V <sub>INA</sub>	V <sub>A-</sub> - 0.3	V <sub>A+</sub> + 0.3	V
Digital Input Voltage	V <sub>IND</sub>	-0.3	V <sub>D+</sub> + 0.3	V
Ambient Temperature (power applied)	T <sub>A</sub>	-55	125	°C
Storage Temperature	T <sub>stg</sub>	-65	150	°C

Notes: 9. Transient currents of up to 100 mA will not cause SCR latch-up.

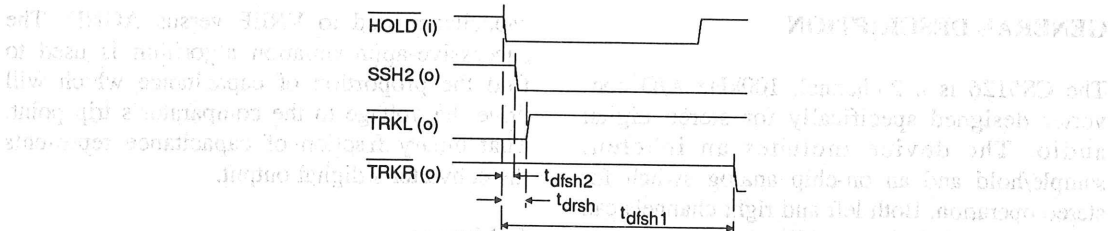
WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

# SWITCHING CHARACTERISTICS

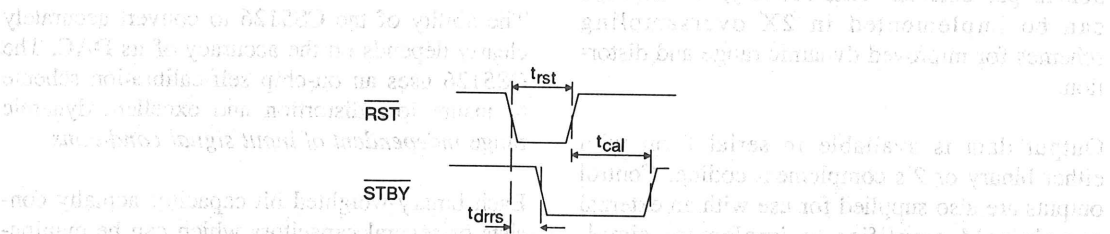
(TA = 25 °C; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; CL = 50 pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Period	t <sub>clk</sub>	40	-	-	ns
HOLD to SSH2 Falling (Note 10)	t <sub>dfsh2</sub>	-	80	-	ns
HOLD to TRKL, TRKR SSH1 Falling	t <sub>dfsh1</sub>	198 t <sub>clk</sub>	-	214 t <sub>clk</sub> + 50	ns
HOLD to TRKL, TRKR SSH1, SSH2 Rising	t <sub>drsh</sub>		80		ns
RST Pulse Width	t <sub>rst</sub>	150	-	-	ns
RST to STBY Falling	t <sub>drss</sub>	-	100	-	ns
RST Rising to STBY Rising	t <sub>cal</sub>	-	34,584,480	-	t <sub>clk</sub>
HOLD Pulse Width	t <sub>hold</sub>	2 t <sub>clk</sub> + 50	-	192 t <sub>clk</sub>	ns
HOLD to L/R Edge (Note 10)	t <sub>dhlri</sub>	- 30	-	192 t <sub>clk</sub>	ns
SCLK period	t <sub>sclk</sub>	200	-	-	ns
SCLK Pulse Width Low	t <sub>sckl</sub>	50	-	-	ns
SCLK Pulse Width High	t <sub>sckh</sub>	50	-	-	ns
SCLK Falling to SDATA Valid	t <sub>dss</sub>	-	100	140	ns
HOLD Falling to SDATA Valid	t <sub>dhs</sub>	-	140	200	ns

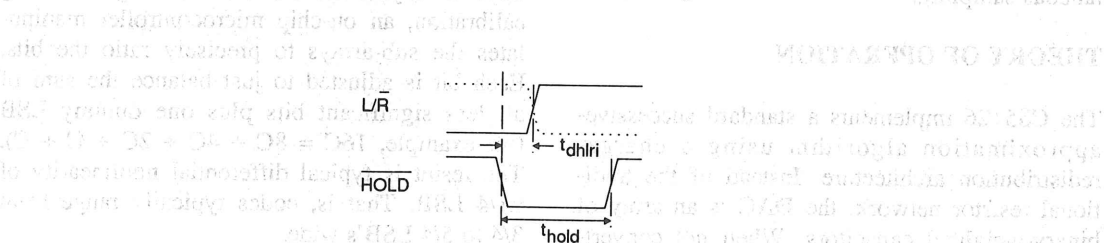
Note: 10. SSH2 only works correctly if HOLD falling edge is within ±30ns of L/R edge OR if HOLD falling edge occurs between 30ns before HOLD rises to 192 t<sub>clk</sub> after HOLD falls.



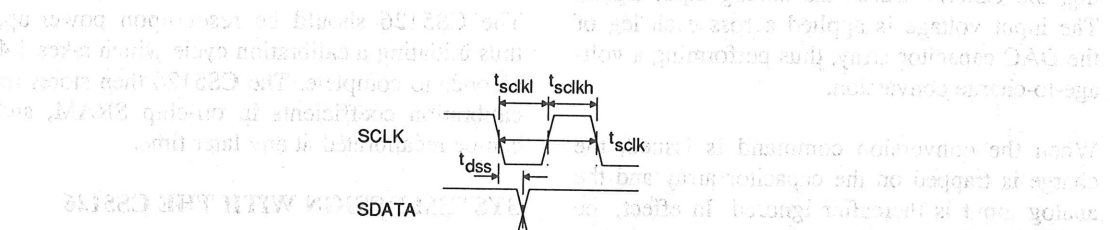
### Control Output Timing



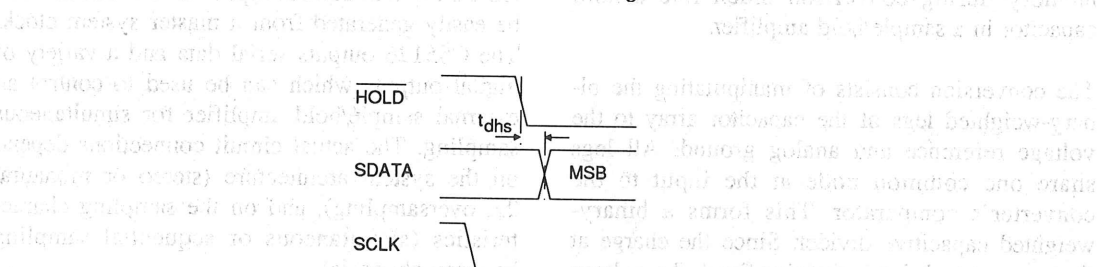
### Reset and Calibration Timing



### Channel Selection Timing



### Serial Data Timing



### Data Transmit Start Timing

## GENERAL DESCRIPTION

The CS5126 is a 2-channel, 100kHz A/D converter designed specifically for stereo digital audio. The device includes an inherent sample/hold and an on-chip analog switch for stereo operation. Both left and right channels can thus be sampled and converted at rates up to 50kHz per channel. Alternatively, the CS5126 can be implemented in 2X oversampling schemes for improved dynamic range and distortion.

Output data is available in serial form with either binary or 2's complement coding. Control outputs are also supplied for use with an external sample/hold amplifier to implement simultaneous sampling.

## THEORY OF OPERATION

The CS5126 implements a standard successive-approximation algorithm using a charge-redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. When not converting, the CS5126 tracks the analog input signal. The input voltage is applied across each leg of the DAC capacitor array, thus performing a voltage-to-charge conversion.

When the conversion command is issued, the charge is trapped on the capacitor array and the analog input is thereafter ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the binary-weighted legs of the capacitor array to the voltage reference and analog ground. All legs share one common node at the input to the converter's comparator. This forms a binary-weighted capacitive divider. Since the charge at the comparator's input remains fixed, the voltage at that point depends on the proportion of

capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance which will drive the voltage to the comparator's trip point. That binary fraction of capacitance represents the converter's digital output.

## Calibration

The ability of the CS5126 to convert accurately clearly depends on the accuracy of its DAC. The CS5126 uses an on-chip self-calibration scheme to insure low distortion and excellent dynamic range *independent of input signal conditions*.

Each binary-weighted bit capacitor actually consists of several capacitors which can be manipulated to adjust the overall bit weight. During calibration, an on-chip microcontroller manipulates the sub-arrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example,  $16C = 8C + 4C + 2C + C + C$ ). The result is typical differential nonlinearity of  $\pm 1/4$  LSB. That is, codes typically range from  $3/4$  to  $5/4$  LSB's wide.

The CS5126 should be reset upon power-up, thus initiating a calibration cycle which takes 1.4 seconds to complete. The CS5126 then stores its calibration coefficients in on-chip SRAM, and can be recalibrated at any later time.

## SYSTEM DESIGN WITH THE CS5126

All timing and control inputs to the CS5126 can be easily generated from a master system clock. The CS5126 outputs serial data and a variety of digital outputs which can be used to control an external sample/hold amplifier for simultaneous sampling. The actual circuit connections depend on the system architecture (stereo or monaural 2X oversampling), and on the sampling characteristics (simultaneous or sequential sampling between channels).

### System Initialization

Upon power up, the CS5126 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5126's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before  $\overline{\text{RST}}$  rises to guarantee an accurate calibration. Later, the CS5126 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5126 will clear and initiate a new calibration cycle mid-conversion or midcalibration.

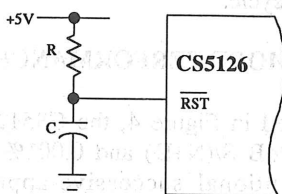


Figure 1. Power-On Reset Circuit

When  $\overline{\text{RST}}$  is brought low all internal logic clears. When it returns high a calibration cycle begins which takes 34,584,480 master clock cycles to complete (approximately 1.4 seconds with a standard 24MHz master clock). The CS5126's  $\overline{\text{STBY}}$  output remains low throughout the calibration sequence, and a rising transition indicates the device is ready for normal operation.

A simple power-on reset circuit can be built using a resistor and capacitor as shown in Figure 1. The RC time constant must be long enough to guarantee the rest of the system is fully powered up and stable by the end of reset.

### Master Clock

The CS5126 operates from an externally-supplied master clock. In stereo operation, the master clock frequency is set at 512 times the per-channel sampling rate (256 in 2X oversampling schemes). The CS5126 can accept master clocks up to 24.576 MHz for 48kHz stereo sampling or 96kHz monaural oversampling.

All timing and control inputs for channel selection, sampling, and serial data transmission may be divided down from the master clock. This yields a completely synchronous system, avoiding sampling and conversion errors due to asynchronous digital noise.

### CIRCUIT CONNECTIONS

#### Stereo Operation

Figure 2 shows the standard circuit connections for operating the CS5126 in its stereo mode. The  $\overline{\text{HOLD}}$ , L/R, and SCLK inputs are derived from the master clock using a binary divider string. A 24.576 MHz master clock is required for a sampling rate of 48kHz per channel.

For 48kHz stereo sampling, the CS5126 must sample and convert at a 96kHz rate to handle both channels. The master clock is divided by 256 and applied to the  $\overline{\text{HOLD}}$  input. A falling transition on the  $\overline{\text{HOLD}}$  pin places the input in the hold mode and initiates a conversion cycle. The  $\overline{\text{HOLD}}$  input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns.

In stereo operation the CS5126 alternately samples and converts the left and right input channels. This alternating channel selection is achieved by dividing the  $\overline{\text{HOLD}}$  input by two (that is, dividing the master clock by 512) and applying it to the L/R input. Upon completion of each conversion cycle, the CS5126 automatically returns to the track mode. The status of L/R as



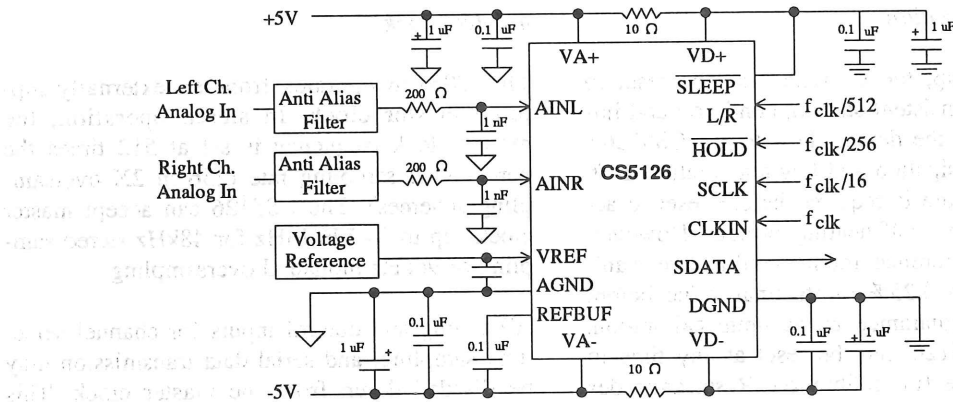


Figure 2. Stereo Mode Connection Diagram

each conversion finishes determines which channel is acquired and tracked. The  $L/\bar{R}$  input must remain valid at least until 30ns before the next falling transition on  $\overline{HOLD}$ .

As shown in the timing diagram in Figure 3, the CS5126 uses pipelined data transmission. That is, data from a particular conversion transmits during the *next* conversion cycle. The serial clock input, SCLK, is derived by dividing the master clock by 16. The MSB (most-significant-bit) will be stable on the first rising edge of SCLK after a falling transition on  $\overline{HOLD}$ . With a serial clock of  $f_{clk}/16$ , transmission of all 16

output bits will span an entire conversion and acquisition cycle.

### STEREO MODE PERFORMANCE

As illustrated in Figure 4, the CS5126 typically provides 92dB S/(N+D) and 0.001% THD. Unlike conventional successive-approximation ADC's, the CS5126's signal-to-noise and dynamic range are not limited by differential nonlinearities (DNL) caused by calibration errors. Rather, the dominant noise source is broadband thermal noise which aliases into the

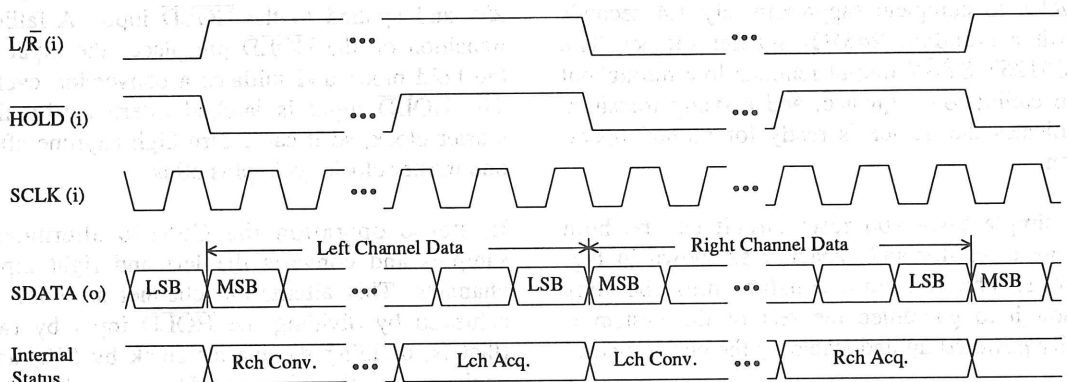
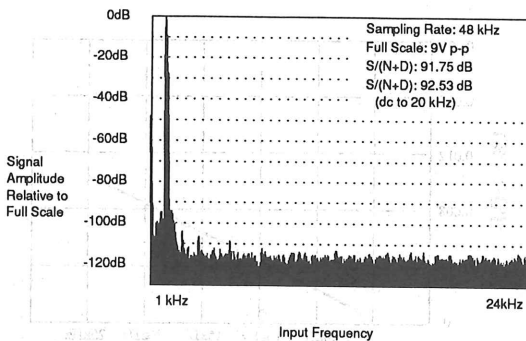


Figure 3. Stereo Mode Timing



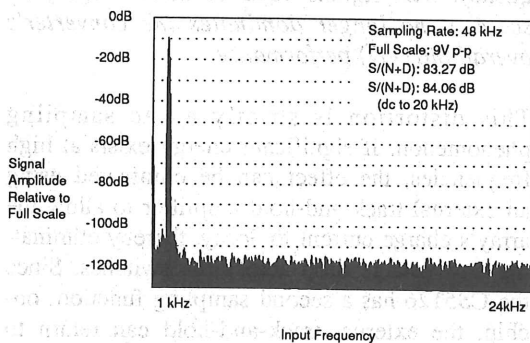
**Figure 4. FFT Plot of CS5126 in Stereo Mode (Left Channel with 1 kHz, Full-Scale Input)**

baseband. This *white* broadband noise also appears as an idle channel noise of 1/2 LSB (rms).

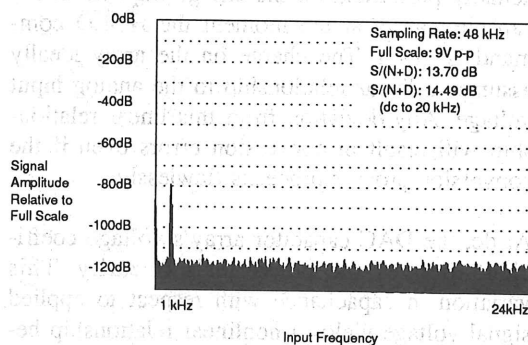
### Differential Nonlinearity

The self-calibration scheme utilized in the CS5126 features a calibration resolution of 1/4 LSB, or 18-bits. This ideally yields DNL of  $\pm 1/4$  LSB, with code widths ranging from 3/4 to 5/4 LSB's. This insures consistent sound quality independent of signal level.

Traditional laser trimmed ADC's have significant differential nonlinearities which are disastrous to



**a. Left Channel with 1 kHz, -10 dB Input**



**b. Left Channel with 1 kHz, -80 dB Input**

**Figure 5. FFT Plots of CS5126 in Stereo Mode**

sound quality with low-level signals. Appearing as wide and narrow codes, DNL often causes entire sections of the transfer function to be missing. Although their affect is minor on S/(N+D) with high amplitude signals, DNL errors dominate performance with low-level signals. For instance, a signal 80dB below full-scale will slew past only 6 or 7 codes. Half of those codes could be missing with a conventional hybrid ADC capable of only 14-bit DNL.

The most common source of DNL errors in conventional ADC's is bit weight errors. These can arise due to accuracy limitations in factory trim stations, thermal or physical stresses after calibration, and/or drifts due to aging or temperature variations in the field. Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions.

Differential nonlinearities in successive-approximation ADC's also arise due to dynamic errors in the comparator. Such errors can dominate if the converter's throughput/sampling rate is

driven too high. The comparator will not be allowed sufficient time to settle during each bit decision in the successive-approximation algorithm. The worst-case codes for dynamic errors are the major transitions (1/2 FS; 1/4, 3/4 FS; etc.). Since DNL effects are most critical with low-level signals, the codes around in mid-scale, (that is, 1/2 FS), are most important. Yet those codes are worst-case for dynamic DNL errors!

With all linearity calibration performed on-chip to 18-bits, the CS5126 maintains accurate bit weights. DNL errors are dominated by residual calibration errors of  $\pm 1/4$  LSB rather than dynamic errors in the comparator. Furthermore, *all* DNL effects on  $S/(N+D)$  are buried by white broadband noise. This yields excellent sound quality *independent of signal level*. (See Figure 5)

### Sampling Distortion

Like most discrete sample/hold amplifier designs, the CS5126's inherent sample/hold exhibits a frequency-dependent distortion due to nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the  $\overline{\text{HOLD}}$  command is given. The charge on the array ideally assumes a linear relationship to the analog input voltage. Any deviation from this linear relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between the charge on the array and the analog input voltage and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 4).

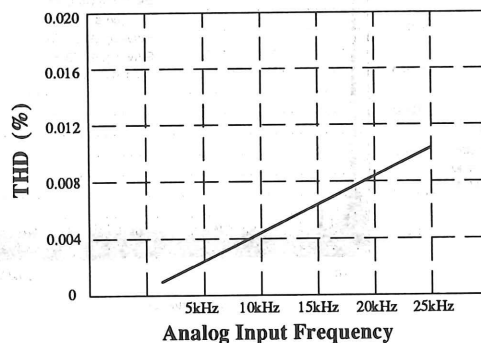


Figure 6. THD vs Input Frequency  
(9V p-p Full-Scale Input)

The ideal relationship between the charge on the array and the input voltage can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency and slew rate as shown in Figure 6 since the magnitude of the steady state current increases. First noticeable at 1kHz, this distortion assumes a linear relationship with input frequency. *With signals 20dB or more below full-scale, it no longer dominates the converter's overall  $S/(N+D)$  performance.*

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the CS5126 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's  $\overline{\text{HOLD}}$  input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

## Simultaneous Sampling

The CS5126 offers four digital output signals, SSH1, SSH2,  $\overline{\text{TRKL}}$ , and  $\overline{\text{TRKR}}$  which can be used to control external sample/hold amplifiers to achieve simultaneous sampling and/or reduce sampling distortion.

Figure 7 shows the timing relationships for SSH1, SSH2,  $\overline{\text{TRKL}}$ , and  $\overline{\text{TRKR}}$ . In the stereo configuration shown in Figure 1 the CS5126 samples the left and right channels 180° out of phase. Simultaneous sampling between the left and right channels can be achieved as shown in Figure 8a using the CS5126's SSH2 output. The external sample/hold will freeze the right channel analog signal as the CS5126 freezes the left channel input at AINL. It will hold that signal valid at AINR until the CS5126 begins a right channel conversion. Once that conversion begins, the sample/hold returns to the sample mode. The acquisition time for the external sample/hold amplifier must not exceed the CS5126's minimum conversion time of 192 master clock cycles (7.8μs for 48kHz stereo sampling).

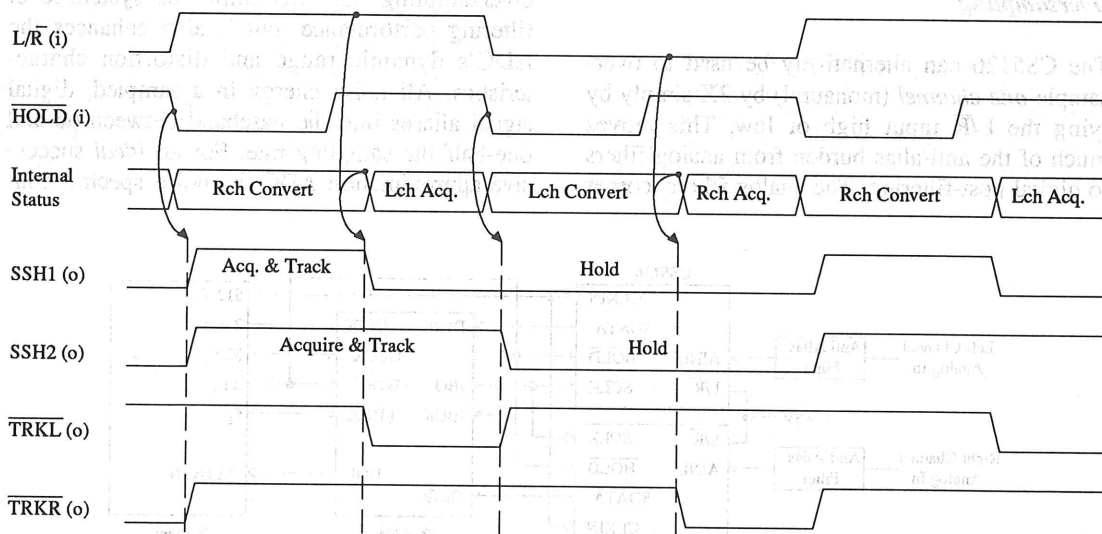
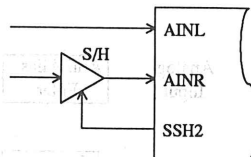
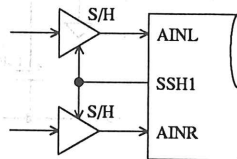


Figure 7. External Sampling Control Output Timing



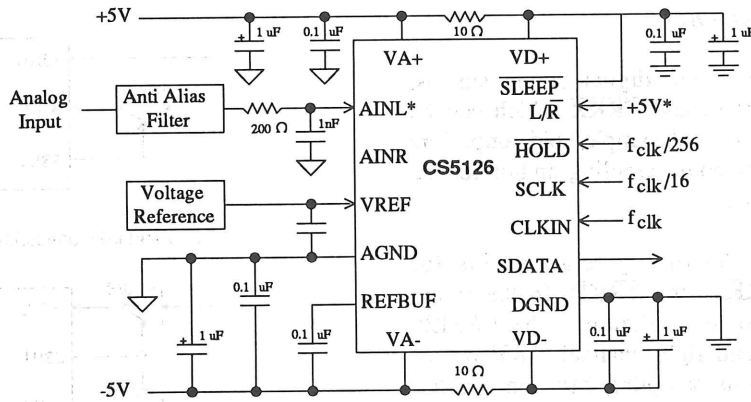
a. Standard Connections



b. High-Slew Conditions

Figure 8. Simultaneous Sampling Connections

The CS5126's sampling distortion with high-frequency, high-amplitude input signals may be improved if a low distortion sample/hold amplifier is used as shown in Figure 8a. The right channel input at AINR will appear as dc to the CS5126 resulting in *no ac current* flowing through the internal MOS switches. Sampling distortion can



\* AINR can alternatively be used with L/R grounded

Figure 9. Monaural 2X Oversampling Connections

likewise be improved for *both channels* using the SSH1 output as shown in Figure 8b. Similarly, the acquisition time for the external sample/hold amplifiers must not exceed the minimum conversion time of 192 master clock cycles (7.8μs for 48kHz stereo sampling).

### Oversampling

The CS5126 can alternatively be used to oversample *one channel* (monaural) by 2X simply by tying the L/R input high or low. This moves much of the anti-alias burden from analog filters to digital post-filtering. The analog filters' corner

can be pushed out in frequency with lower roll-off, allowing lower passband ripple and more linear phase in the audioband. Digital FIR filtering, meanwhile, can be used to implement high roll-off filters with ultra-low passband ripple and perfectly linear phase.

Oversampling not only improves system-level filtering performance, but it also enhances the ADC's dynamic range and distortion characteristics. All noise energy in a sampled, digital signal aliases into the baseband between dc and one-half the sampling rate. For an *ideal* successive-approximation ADC the noise spectral con-

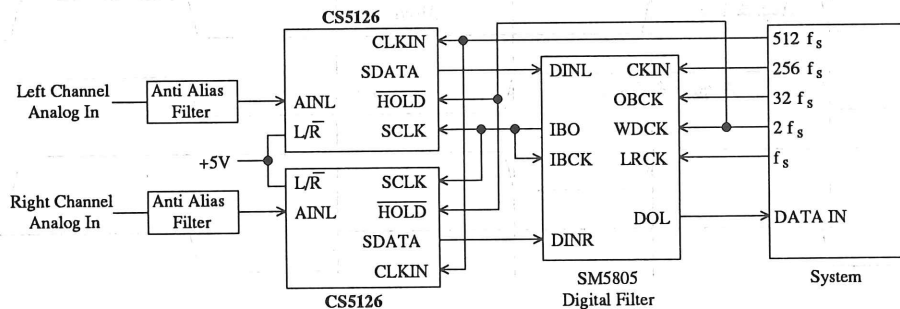


Figure 10. Example Oversampling System Diagram

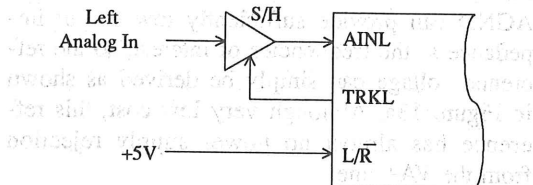


Figure 11. High-Slew Monaural Connections

ment is white. Therefore, in a 2X oversampling scheme such as 96kHz sampling the ADC's noise will be spread *uniformly* from dc to 48kHz. Digital post-filtering then rejects noise outside of the 20kHz or 22kHz bandwidth, resulting in improved signal-to-noise and dynamic range. For a white noise spectrum, a 2X reduction in bandwidth yields a 3dB improvement in dynamic range.

Due to its on-chip self-calibration scheme, the CS5126's dynamic range is limited only by *white* broadband noise rather than signal-dependent DNL errors. Therefore, the CS5126 picks up a full 3dB improvement in dynamic range to 95dB when implemented in 2X oversampling schemes.

Oversampling and digital filtering also enhance the ADC's distortion performance. Consider for example a full-scale 15kHz input signal to the CS5126 sampling at 96kHz. Sampling distortion produces THD of approximately 0.005% (86dB) at the converter's output. Most of the distortion energy resides in the second and third harmonics at 30kHz and 45kHz. Meanwhile, digital filters such as the SM5805 shown in Figure 10 will roll-off rapidly from 22kHz to 28kHz and reject distortion energy in the second, third, and fourth harmonics. Clearly, oversampling results in superior system-level distortion.

Still, if the CS5126's distortion performance with high-frequency, high-amplitude signals must be enhanced in 2X oversampling schemes, the TRKL or TRKR outputs can be used. Either TRKL or TRKR will fall at the end of each conversion cycle depending on which channel is being acquired. The AINL and TRKL connections (or AINR and TRKR) can be used as shown in Figure 11 to control an external low-distortion sample/hold to create an effective dc input for the CS5126 and remove sampling distortion.

## Digital Circuit Connections

When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

The CS5126 has a power down mode, initiated by bringing **SLEEP** low. During power down, the A/D Converter's calibration information is retained. The CS5126 may be used for conversion immediately after **SLEEP** is brought high.

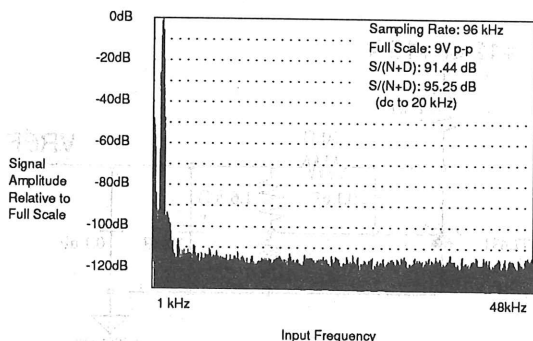


Figure 12. FFT Plot of CS5126 in Monaural 2X Oversampling Mode



## ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5126 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

### Reference Considerations

An application note titled "Voltage references for the CS501X/CSZ511X Series of A/D Converters" is available which describes the dynamic load conditions presented by the VREF input on Crystal's self-calibrating SAR A/D converters (including the CS5126). As the CS5126 sequences through bit decisions it switches portions of the capacitor array to the VREF pin in accordance with the successive-approximation algorithm. For proper operation, the source impedance at the VREF pin must remain low at frequencies up to 1MHz.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the frequencies of interest, so the reference voltage can simply be derived as shown in Figure 13a. Although very low cost, this reference has almost no power supply rejection from the VA+ line.

Alternatively, a more stable and precise reference can be generated using a TL431 shunt reference from T.I. or Motorola, as shown in Figure 13b.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At the full-rated 24 MHz clock the reference must supply a maximum load current of 20μA peak-to-peak (2μA typical). An output impedance of 2Ω will therefore yield a maximum error of 40mV. With a 4.5V reference and LSB size of 138mV this would insure approximately 1/4 LSB accuracy. A 10μF capacitor exhibits an impedance of less than 2Ω at frequencies greater than 16kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

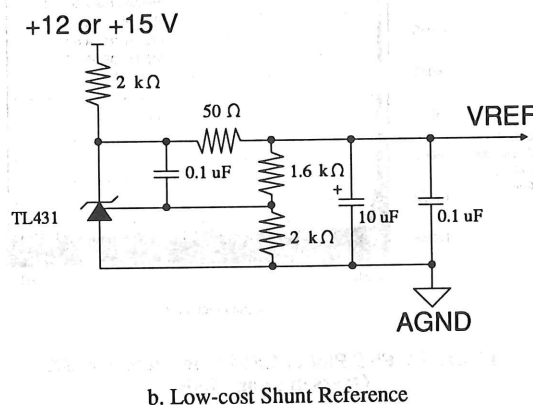
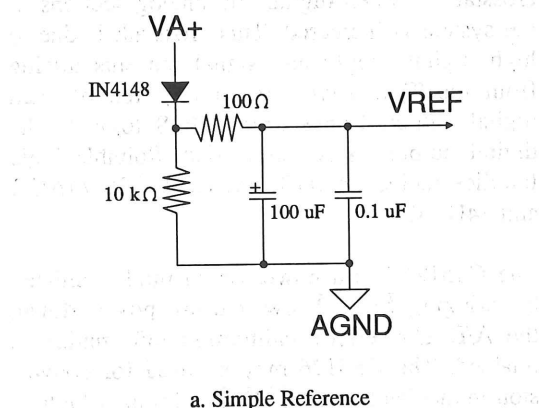


Figure 13. Suggested Voltage Reference Circuits

The CS5126 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5126 can actually accept reference voltages up to the positive analog supply. However, as the reference voltage approaches  $V_{A+}$  the external drive requirements may increase at  $V_{REF}$ .

An internal reference buffer is used to protect the external reference from current transients during conversion. This internal buffer enlists the aid of an external 0.1  $\mu$ F ceramic capacitor which must be tied between its output,  $REFBUF$ , and the negative analog supply,  $V_{A-}$ .

### Analog Input Connection

Each time the CS5126 finishes a conversion cycle it switches the internal capacitor array to the appropriate analog input pin,  $A_{INL}$  or  $A_{INR}$ . This creates a minor dynamic load at the sampling frequency. All throughput specifications apply for maximum analog source impedances of 200  $\Omega$  at  $A_{INL}$  and  $A_{INR}$ . In addition, the comparator requires source impedances of less than 400  $\Omega$  around 2MHz for stability, which is met by practically all bipolar op amps. For more information, see our Application Note: "Input Buffers for the CS501X/CSZ511X Series of A/D Converters"

### Analog Input Range/Coding Format

The CS5126 features a bipolar input range with the reference voltage applied to  $V_{REF}$  defining both positive and negative full-scale. The coding format is set by the state of the  $CODE$  input. If high, coding is 2's complement; if low, the CS5126's output is in offset-binary format.

### Grounding and Power Supply Decoupling

The CS5126 uses the analog ground connection,  $AGND$ , only as a reference voltage.

*No dc power or signal currents flow through the  $AGND$  connection, thus minimizing the potential for interchannel crosstalk. Also,  $AGND$  is completely independent of  $DGND$ . However, any noise riding on the  $AGND$  input relative to the system's analog ground will induce conversion errors. Therefore, both analog inputs and the reference voltage should be referred to the  $AGND$  pin, which should be used as the entire system's analog ground. The digital and analog supplies are isolated within the CS5126 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1  $\mu$ F ceramic capacitors. If significant low frequency noise is present on the supplies, 1  $\mu$ F tantalum capacitors are recommended in parallel with the 0.1  $\mu$ F capacitors.*

*The positive digital power supply of the CS5126 must never exceed the positive analog supply by more than a diode drop or the CS5126 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagrams in figures 2 and 9 show a decoupling scheme which allows the CS5126 to be powered from a single set of  $\pm 5V$  rails. The positive digital supply is derived from the analog supply through a 10  $\Omega$  resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10  $\Omega$  resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.*

As with any high-precision A/D converter, the CS5126 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5126. The CDB5126 evaluation board is available for the CS5126, which avoids

the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5126, and can be quickly reconfigured to simulate any combination of sampling and master clock conditions.

### Power Supply Rejection

The CS5126 features a fully differential comparator design, resulting in superior power supply rejection. Rejection is further enhanced by the on-chip self-calibration and "auto-zero" process. Figure 14 shows worst-case rejection for all combinations of conversion rates and input conditions.

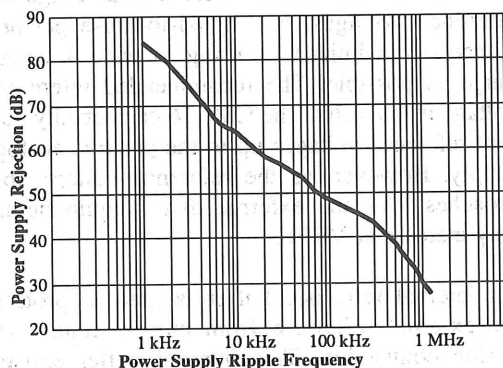
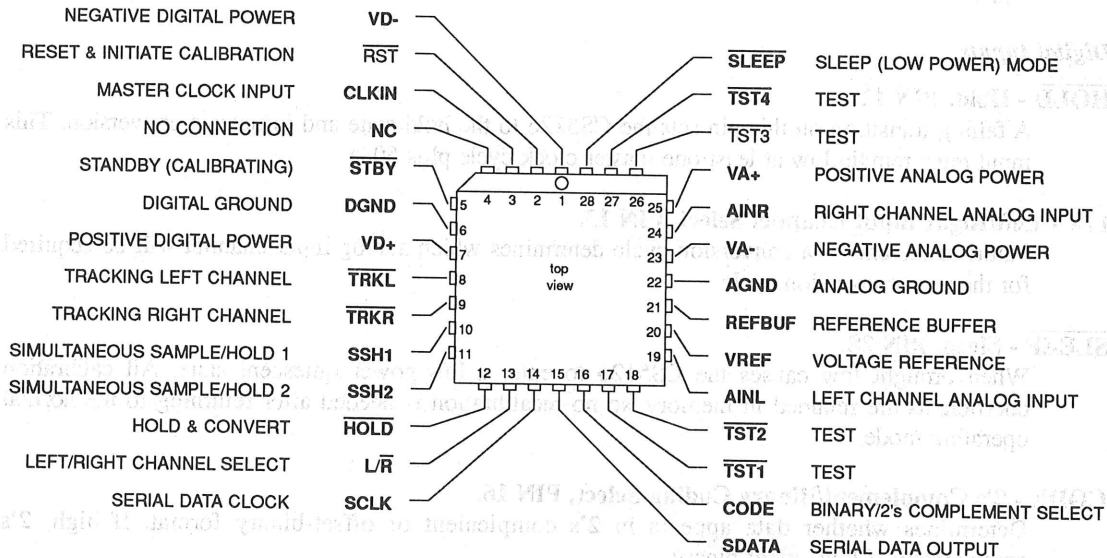


Figure 14. Power Supply Rejection

## PIN DESCRIPTIONS

2

NEGATIVE DIGITAL POWER	VD-	1	28	SLEEP	SLEEP (LOW POWER) MODE
RESET & INITIATE CALIBRATION	RST	2	27	TST4	TEST
MASTER CLOCK INPUT	CLKIN	3	26	TST3	TEST
NO CONNECTION	NC	4	25	VA+	POSITIVE ANALOG POWER
STANDBY (CALIBRATING)	STBY	5	24	AINR	RIGHT CHANNEL ANALOG INPUT
DIGITAL GROUND	DGND	6	23	VA-	NEGATIVE ANALOG POWER
POSITIVE DIGITAL POWER	VD+	7	22	AGND	ANALOG GROUND
TRACKING LEFT CHANNEL	TRKL	8	21	REFBUF	REFERENCE BUFFER
TRACKING RIGHT CHANNEL	TRKR	9	20	VREF	VOLTAGE REFERENCE
SIMULTANEOUS SAMPLE/HOLD 1	SSH1	10	19	AINL	LEFT CHANNEL ANALOG INPUT
SIMULTANEOUS SAMPLE/HOLD 2	SSH2	11	18	TST2	TEST
HOLD & CONVERT	HOLD	12	17	TST1	TEST
LEFT/RIGHT CHANNEL SELECT	L/R	13	16	CODE	BINARY/2's COMPLEMENT SELECT
SERIAL DATA CLOCK	SCLK	14	15	SDATA	SERIAL DATA OUTPUT



**Power Supply Connections****VD+ - Positive Digital Power, PIN 7.**

Positive digital power supply. Nominally +5 volts.

**VD- - Negative Digital Power, PIN 1.**

Negative digital power supply. Nominally -5 volts.

**DGND - Digital Ground, PIN 6.**

Digital ground reference.

**VA+ - Positive Analog Power, PIN 25.**

Positive analog power supply. Nominally +5 volts.

**VA- - Negative Analog Power, PIN 23.**

Negative analog power supply. Nominally -5 volts.

**AGND - Analog Ground, PIN 22.**

Analog ground reference.

Oscillator

**CLKIN - Clock Input, PIN 3.**

All conversions and calibrations are timed from a master clock which must be externally supplied.

**Digital Inputs****HOLD - Hold, PIN 12.**

A falling transition on this pin sets the CS5126 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

**L/R - Left/Right Input Channel Select, PIN 13.**

Status at the end of a conversion cycle determines which analog input channel will be acquired for the next conversion cycle.

**SLEEP - Sleep, PIN 28.**

When brought low causes the CS5126 to enter a low-power quiescent state. All calibration coefficients are retained in memory, so no recalibration is needed after returning to the normal operating mode.

**CODE - 2's Complement/Binary Coding Select, PIN 16.**

Determines whether data appears in 2's complement or offset-binary format. If high, 2's complement; if low, offset-binary.

**SCLK - Serial Clock, PIN 14.**

Serial data changes status on a falling edge of this input, and is valid on a rising edge.

**RST - Reset, PIN 32.**

When taken low, all internal digital logic is reset. Upon returning high, a full calibration sequence is initiated which takes 34,584,480 master clock cycles to complete.

***Analog Inputs*****AINL, AINR - Left and Right Channel Analog Inputs, PINS 19 and 24.**

Analog input connections for the left and right input channels.

**VREF - Voltage Reference, PIN 20.**

The analog reference voltage which sets the analog input range. Its magnitude sets both positive and negative full-scale.

***Digital Outputs*****STBY - Standby (Calibrating), PIN 5.**

Indicates calibration status after reset. Remains low throughout the calibration sequence and returns high upon completion.

**SDATA - Serial Output, PIN 15.**

Presents each output data bit on a falling edge of the SCLK input. Data is valid to be latched on the rising edge of SCLK.

**SSH1, SSH2 - Simultaneous Sample/Hold 1 and 2, PINS 10 and 11.**

Used to control external sample/hold amplifier(s) to achieve simultaneous stereo sampling.

**TRKL, TRKR - Tracking Left, Tracking Right, PINS 8 and 9.**

Indicate the end of a conversion cycle. Either TRKL or TRKR falls at the end of a conversion cycle depending on the status of L/R and which channel is to be tracked.

***Analog Outputs*****REFBUF - Reference Buffer Output, PIN 21.**

Reference buffer output. A 0.1μF ceramic capacitor must be tied between this pin and VA-.

***Miscellaneous*****NC - No Connection, PIN 4.**

Must be left floating for proper operation.

**TST1, TST2, TST3, TST4 - Test, PINS 17, 18, 26, 27.**

Allow access to the CS5126's test functions which are reserved for factory use. Must be tied to VD+.



## PARAMETER DEFINITIONS

**Total Harmonic Distortion** - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

**Signal-to-Noise plus Distortion Ratio** - The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

**Dynamic Range** - Full-scale Signal-to-Noise plus Distortion with the input signal 60dB below full-scale. Units in decibels.

**Interchannel Isolation** - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

**Full Scale Error** - The deviation of the last code transition from the ideal ( $V_{REF}/2$  LSB's) after all offsets have been externally compensated. Units in decibels relative to full scale.

**Bipolar Offset** - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal ( $1/2$  LSB below AGND). Units in microvolts.

**Interchannel Mismatch** - The difference in output codes between the left and right channels with the same analog input applied. Units expressed in decibels relative to full scale. Tested at full scale input.

**Aperture Time** - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

**Aperture Jitter** - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

## Evaluation Board for CS5101, CS5102 & CS5126

### Features

- Serial to Parallel Conversion
- All Timing Signals Provided
- Adjustable Voltage Reference
- $\pm 5$  V Regulators
- Digital and Analog Patch Areas

### General Description

The CDB5101/5102/5126 Evaluation Board allows fast evaluation of the CS5101, CS5102 and/or CS5126 2-Channel, 16-bit Analog-to-Digital Converters.

Analog inputs are via BNC connectors. Digital outputs are available both directly from the ADC in serial form, and in 16 bit parallel form.

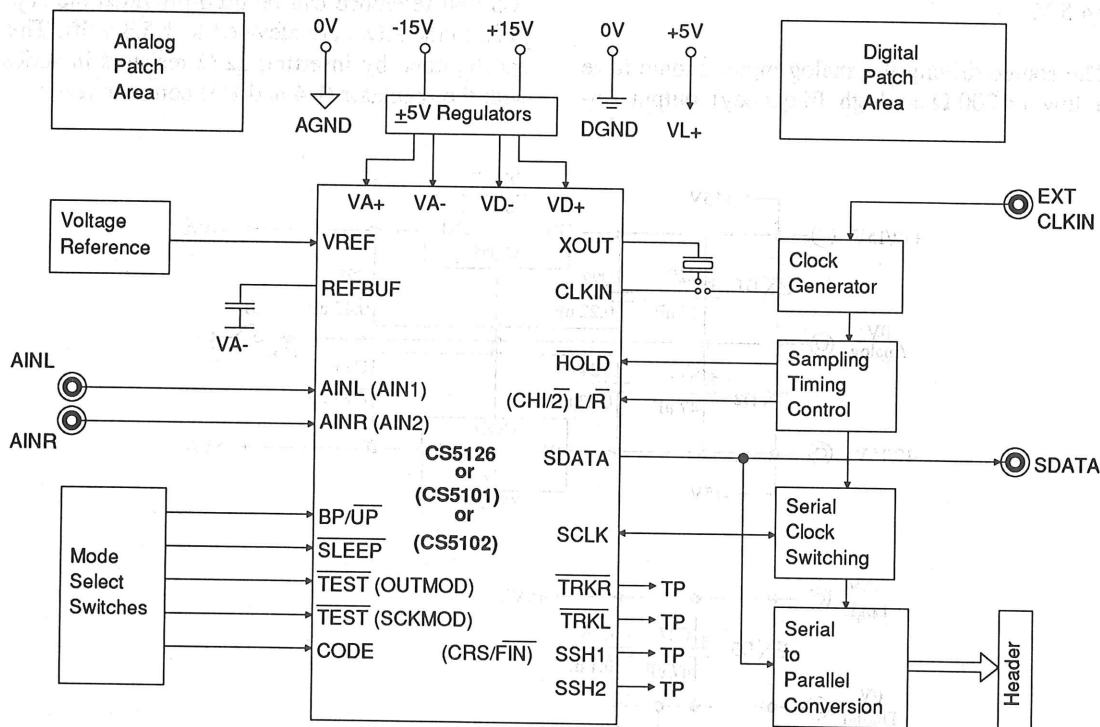
An adjustable monolithic voltage reference is included.

### Ordering Information

CDB5126  
CDB5101  
CDB5102

2

### Block Diagram



## Power Supplies

Figure 1 shows the power supply arrangements. The analog section of the board is powered by  $\pm 12/15$  volts, which is regulated down to  $\pm 5$  V for the ADC. A separate +5 V digital supply is required to power the discrete logic. Be sure to switch on the  $\pm 12/15$  V at the same time as, or before, the +5 V logic supply. This will make sure that the CLK and other logic signal are not driving the part before it is powered.

## Analog Input

The analog input range is either  $\pm V_{ref}$  in the bipolar mode or 0 V to  $+V_{ref}$  in the unipolar mode. The voltage reference is factory set to the recommended value of +4.5 volts, so the typical input signal ranges become  $\pm 4.5$  volts or 0 V to +4.5 V.

The source driving the analog inputs should have a low ( $< 200 \Omega$  at high frequency) output im-

pedance. Be careful not to overdrive the inputs outside the power supplies of the ADC ( $\pm 5$  V). Figure 2 shows the buffer circuit used at the Crystal factory to drive the ADC when performing FFT testing. See the CS5126 data sheet for example FFT test results.

## Voltage Reference

As shown in Figure 3, an LT1019-5 voltage reference provides a stable 4.5 V reference for the ADC. An optional OP27 buffer filters out excess reference noise and provides a very low output impedance. To try the unbuffered LT1019-5 directly, solder in J2 and cut the VREF trace. Alternatively the shunt reference based reference schematic given in the CS5126 data sheet can be evaluated by adding it to the analog patch area.

A 5 volt reference can be used provided the supplies to the ADC are elevated to  $\pm 5.3$  volts. This can be done by inserting  $22 \Omega$  resistors in series with the regulator (U4 and U5) common leads.

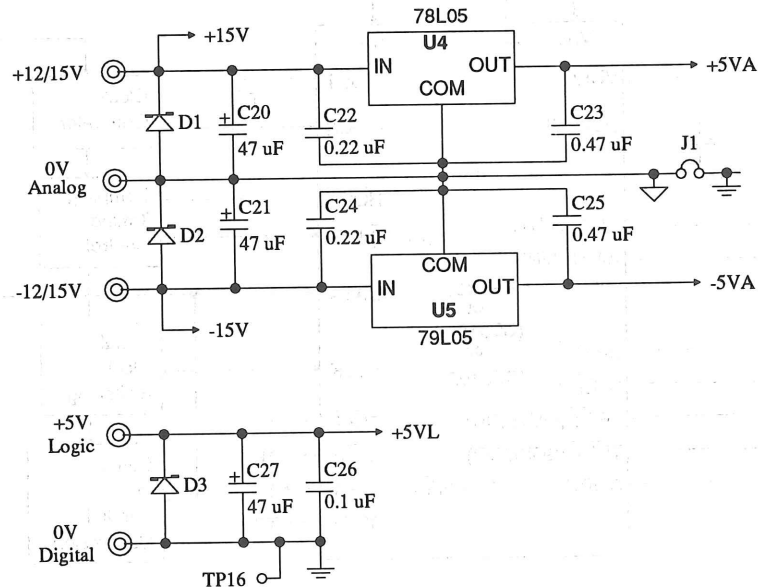


Figure 1. Power Supplies

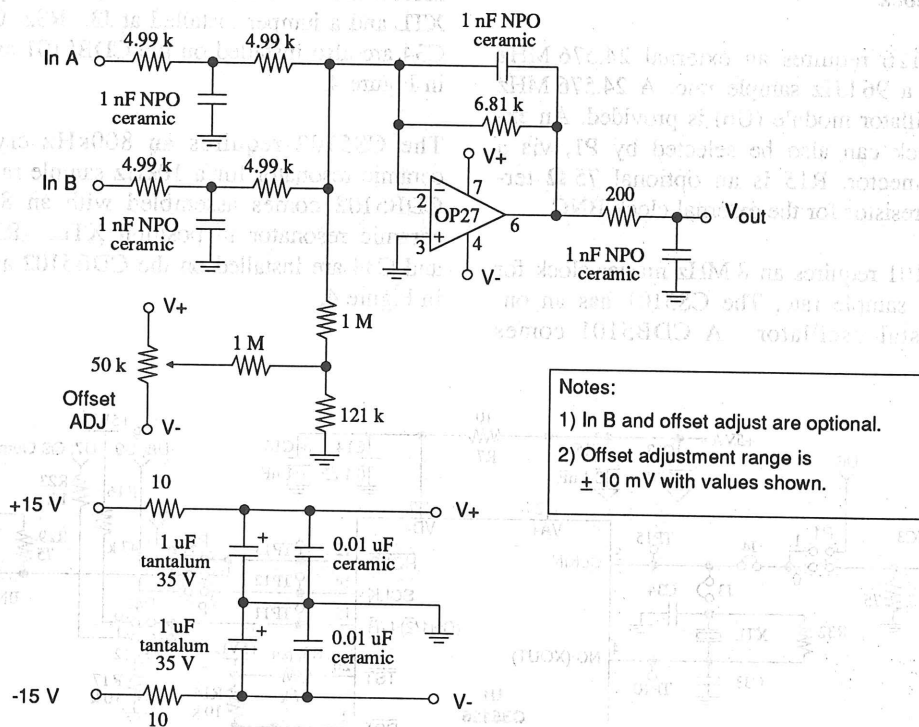


Figure 2. Example Input Buffer Circuit (not provided on the CDB5126/5101 evaluation board)

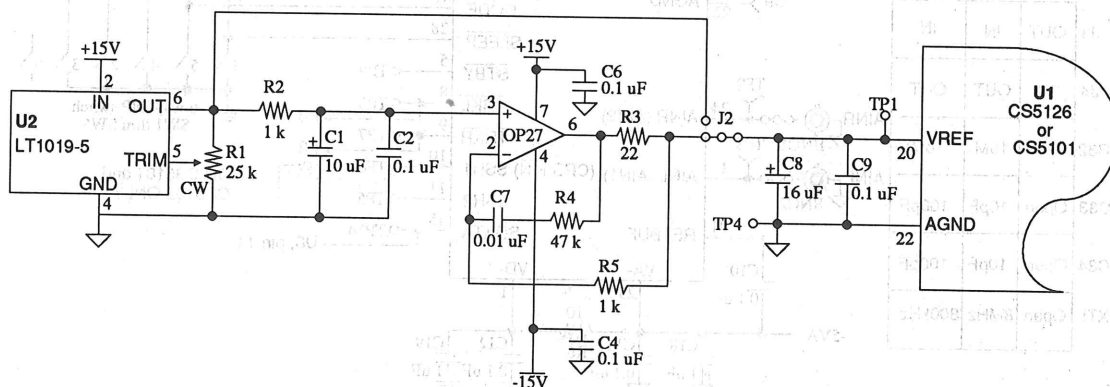


Figure 3. Voltage Reference

### Master Clock

The CS5126 requires an external 24.576 MHz clock for a 96 kHz sample rate. A 24.576 MHz clock oscillator module (U6) is provided. An external clock can also be selected by P1, via a BNC connector. R15 is an optional 75  $\Omega$  terminating resistor for the external clock BNC.

The CS5101 requires an 8 MHz master clock for a 96 kHz sample rate. The CS5101 has an on-chip crystal oscillator. A CDB5101 comes

assembled with an 8 MHz crystal in position XTL and a jumper installed at J3. R32, C33 and C34 are also installed on the CDB5101 as shown in Figure 4.

The CS5102 requires an 800kHz crystal or ceramic resonator for a 10kHz sample rate. The CDB5102 comes assembled with an 800 kHz ceramic resonator in position XTL. R32, C33 and C34 are installed on the CDB5102 as shown in Figure 4.

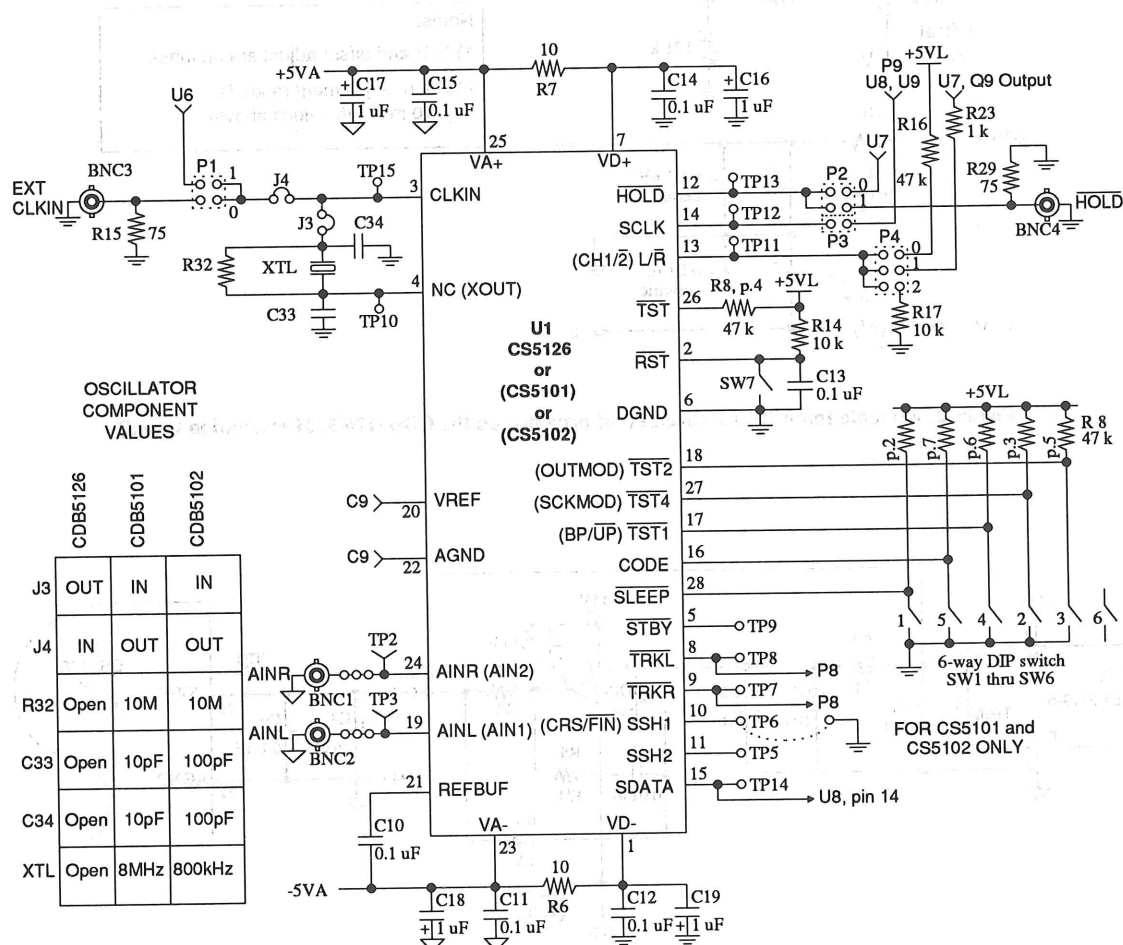


Figure 4. ADC Connections

### Sampling Clock Generation Logic

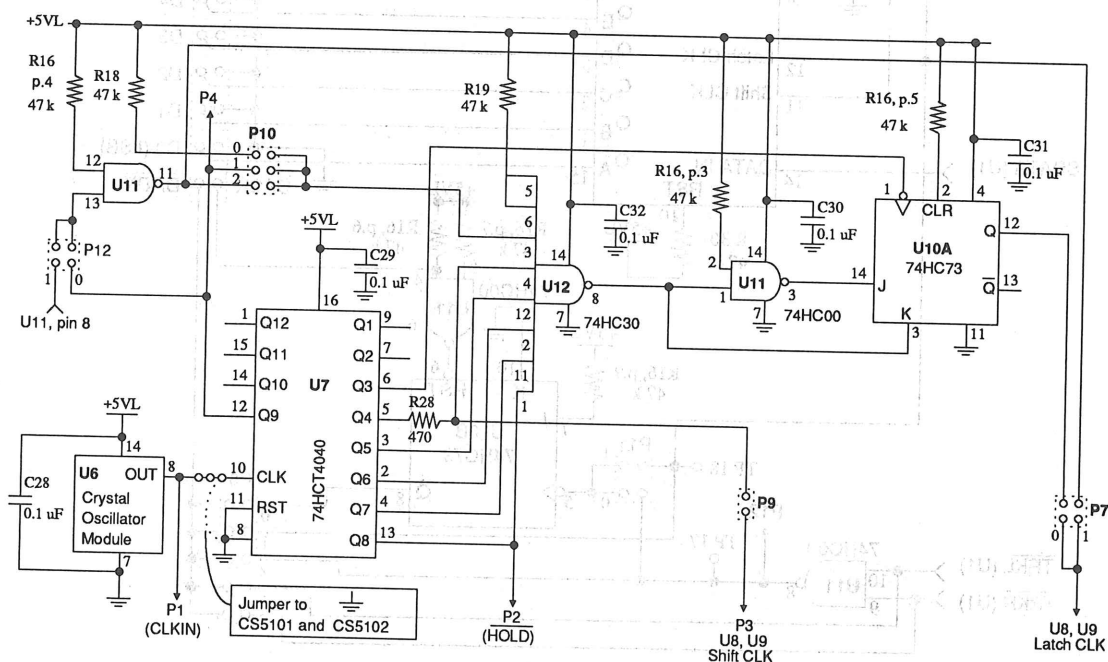
The CS5126, and the CS5101 or CS5102 in PDT mode, requires an external serial clock to clock out the data. The CDB5126/5101/5102 board has the logic necessary to generate the master clock, HOLD, L/R, and SCLK to allow fast evaluation of the ADC. In most systems, these timing signals will be available from the main timing section, typically generated by a logic array of some variety. HOLD may be brought in externally via a BNC, optionally terminated by R29. SCLK and L/R select may be brought in externally via test points and removing jumpers.

Figure 5 shows the on-board clock generation circuitry. U7 (74HC4040) produces binary divided ratios of the 24.576 MHz master clock. Q4 generates a 1.5 MHz clock, which is used for SCLK. Q8 generates a 96 kHz clock, used for  $\overline{\text{HOLD}}$ , and Q9 generates a 48 kHz clock, optionally used to toggle  $\text{L}/\overline{\text{R}}$  select. This set of clocks

causes the CS5126 to continuously convert, generating a continuous stream of serial data bits. To correctly identify the last bit of each word, U12 produces a pulse only when Q4, Q5, Q6, Q7, Q8, and optionally Q9 are all high. This state is latched by U10A to prevent any glitches, and the resulting signal (attached to TP18) is used to latch the U8-U9 shift registers.

## Serial to Parallel Conversion

Figure 6 shows the serial to parallel conversion circuit. Two 74HC595 shift register/latches connected in series with SDATA assemble 16-bit, parallel words, clocked by SCLK. As discussed above, the outputs are latched inside the 74HC595 at the end of each 16-bit word. The outputs are brought out to a 40-way header (P5). Only low capacitance, twisted pair, ribbon cable should be used.



### Figure 5. Timing Generator



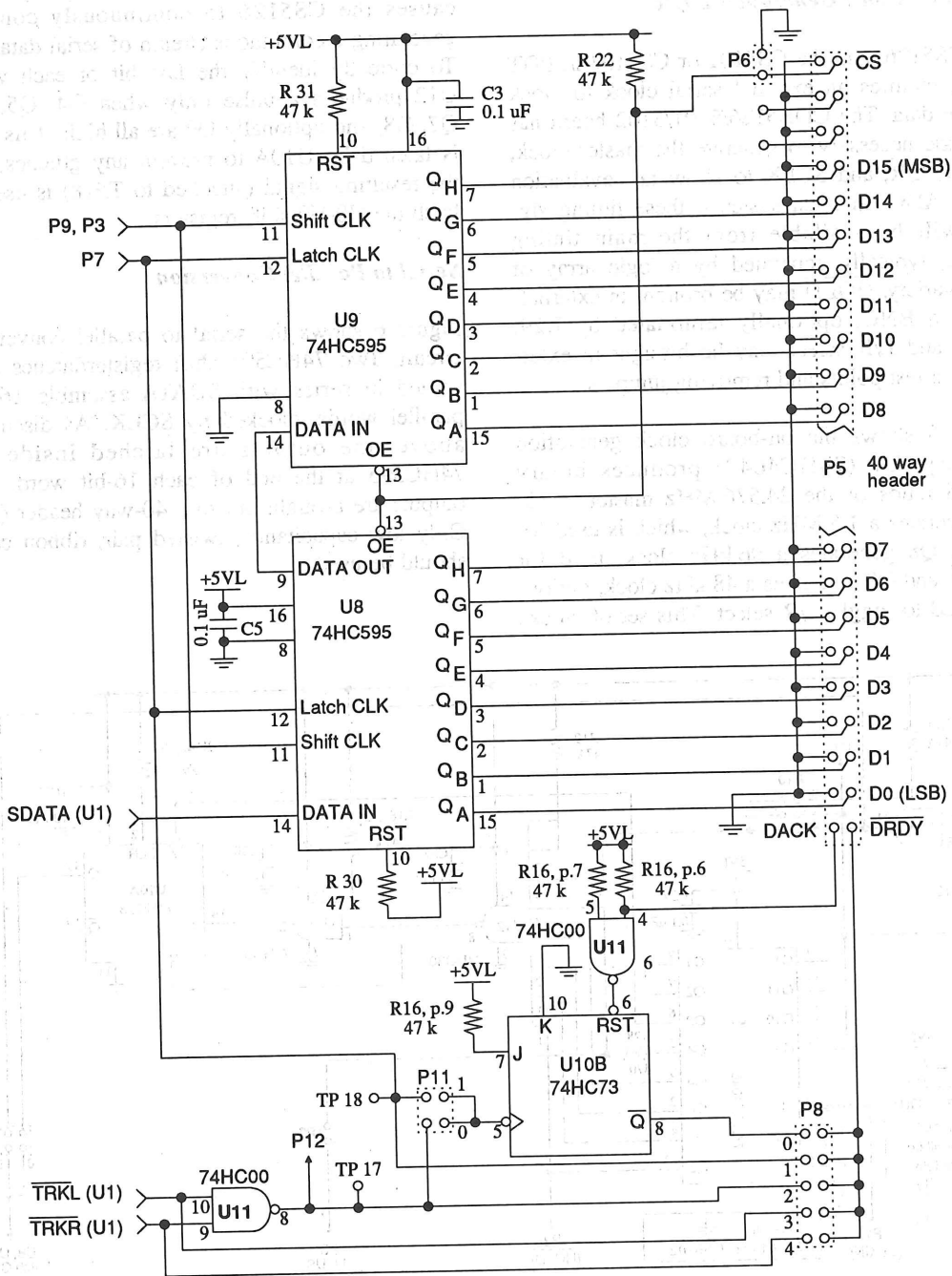


Figure 6. Serial to Parallel Converter

J1	-	Joins analog ground to digital ground on the board.
J2	-	Joins LT1019-5 reference directly to the VREF pin on the ADC. Before doing this, break the connection between R3 and the ADC VREF pin by using a twist drill to remove the central feedthrough. This option allows evaluation of different reference configurations.
J3	-	Connects the crystal to CLKIN on the ADC. Only used for CS5101.
J4	-	Connects an external clock to CLKIN on the ADC. Cut if using a crystal.

**Table 1. Solder Link Options**

P1	†	0	-	Select external clock via BNC connector
	*	1	-	Select on-board clock generated by U6.
P2	*	0	-	Select on-board generated $\overline{\text{HOLD}}$ .
	†	1	-	Select external $\overline{\text{HOLD}}$ via BNC connector.
P3	*†			Connect SCLK to on-board shift registers.
P4	*†	0	-	Pull $\overline{\text{L/R}}$ select pin high, selecting the left channel only.
		1	-	Drive $\overline{\text{L/R}}$ select at 48 kHz from the on-board timing generator.
		2	-	Pull $\overline{\text{L/R}}$ select pin low, selecting the right channel only.
P6	*†			Connect the $\overline{\text{OE}}$ pins of the shift registers to ground. Permanently enables the 3-state output buffers.
P7	*	0	-	Connects the on-board Data Ready signal to the shift registers.
	†	1	-	Connects the NAND gate outputs (U11, pin 11) to the shift registers. Used in CS5101/CS5102 FRN mode.
P8	*†	0	-	Connects the latched on-board Data Ready signal to P5.
		1	-	Connects the un-latched on-board Data Ready signal to P5.
		2	-	Connects $\overline{\text{TRKL}}$ and $\overline{\text{TRKR ANDED}}$ together to P5. This signal can be used as an "End of Convert" indicator.
		3	-	Connects $\overline{\text{TRKL}}$ to P5.
		4	-	Connects $\overline{\text{TRKR}}$ to P5.
P9	*			Connects the on-board generated SCLK to the rest of the on-board circuitry. Not present in the CS5101/5102 FRN mode.
P10	*†	0	-	Causes the on-board Data Ready generating circuit to flag data ready every conversion.
		1	-	Causes the on-board Data Ready generating circuit to flag data ready every left conversion. P4 must be in position 1 for this to work.
		2	-	Causes the on-board Data Ready generating circuit to flag data ready every right conversion. P4 must be in position 1 for this to work.
P11	†	0	-	Connects $\overline{\text{TRKL}}$ & $\overline{\text{TRKR}}$ to U10B, the handshake flip-flop. Used in CS5101/CS5102 FRN mode.
	*	1	-	Connects the on-board data ready signal to U10B. Used for the CS5126.
P12	*	0	-	Allows selection of the $\overline{\text{DRDY}}$ signals for alternate channels.
	†	1	-	Connects the $\overline{\text{TRKL}}$ & $\overline{\text{TRKR}}$ to U11, pin 13. Used in the CS5101/CS5102 FRN mode.
* Factory default state for CS5126				

**Table 2. Shorting Plug Selectable Options**

U10B (74HC73) is used as a handshake flip-flop with the computer system attached to the evaluation board. The board brings  $\overline{\text{DRDY}}$  low. The computer reads the data and then sets DACK momentarily high. This resets U10B for the next word. This handshake can be disabled by setting P8 jumper to position 1.

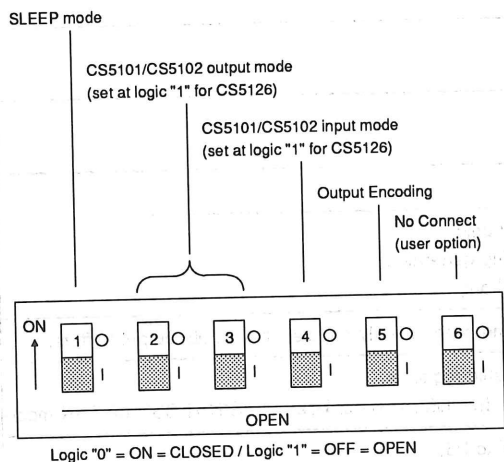


Figure 7. DIP switch configuration

Switch	Logic	Mode
1	0	SLEEP mode
	1	Normal mode
2, 3		CS5101/CS5102 output mode, set to "1" for CS5126
4	0	CS5101/CS5102 Unipolar input
	1	CS5101/CS5102 Bipolar input / CS5126 normal
5	0	Offset binary output code
	1	2's complement output code
6		Unconnected. Available for user's application

Table 3. DIP Switch Selection Options

Sw. 2	Sw. 3	CS5101/CS5102 Output Mode
1	1	(PDT) Pipelined Data Transmission
1	0	(RBT) Registered Burst Transmission
0	1	(SSC) Synchronous Self-Clocking
0	0	(FRN) Free Run

Table 4. CS5101/CS5102 Output Mode Options

### DIP Switches

Figure 7 and Tables 3 and 4 show the DIP switch selectable options.

	CS5126	CS5101
TP1	VREF	VREF
TP2	AINR	AIN2
TP3	AINL	AIN1
TP4	AGND	AGND
TP5	SSH2	SSH
TP6	SSH1	CRS/ $\overline{\text{FIN}}$
TP7	$\overline{\text{TRKR}}$	$\overline{\text{TRK2}}$
TP8	$\overline{\text{TRKL}}$	$\overline{\text{TRK1}}$
TP9	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$
TP10	NC	XOUT
TP11	L/ $\overline{\text{R}}$	CH/ $\overline{2}$
TP12	SCLK	SCLK
TP13	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$
TP14	SDATA	SDATA
TP15	CLKIN	CLKIN
TP16	DGND	DGND
TP17	$\overline{\text{TRKL}} + \overline{\text{TRKR}}$	
TP18	Latch Clock for the 74HC595 shift registers	

Table 5. CDB5126/5101/5102 Test Points

### Test Points

Above is a list of the test points provided on the CDB5126/5101/5102 Evaluation Board.

## Miscellaneous Hints on Using the Evaluation Board

Always hit the reset button after powering-up the board. The CS5126, CS5101 and CS5102 are self calibrating and require the reset signal to initiate the calibration procedure.

P4 controls the ADC input mux. This is used to set the mux to be continuously connected to one channel, or to be toggling between two channels. This is very useful for evaluating oversampled vs. regular sampling digital audio.

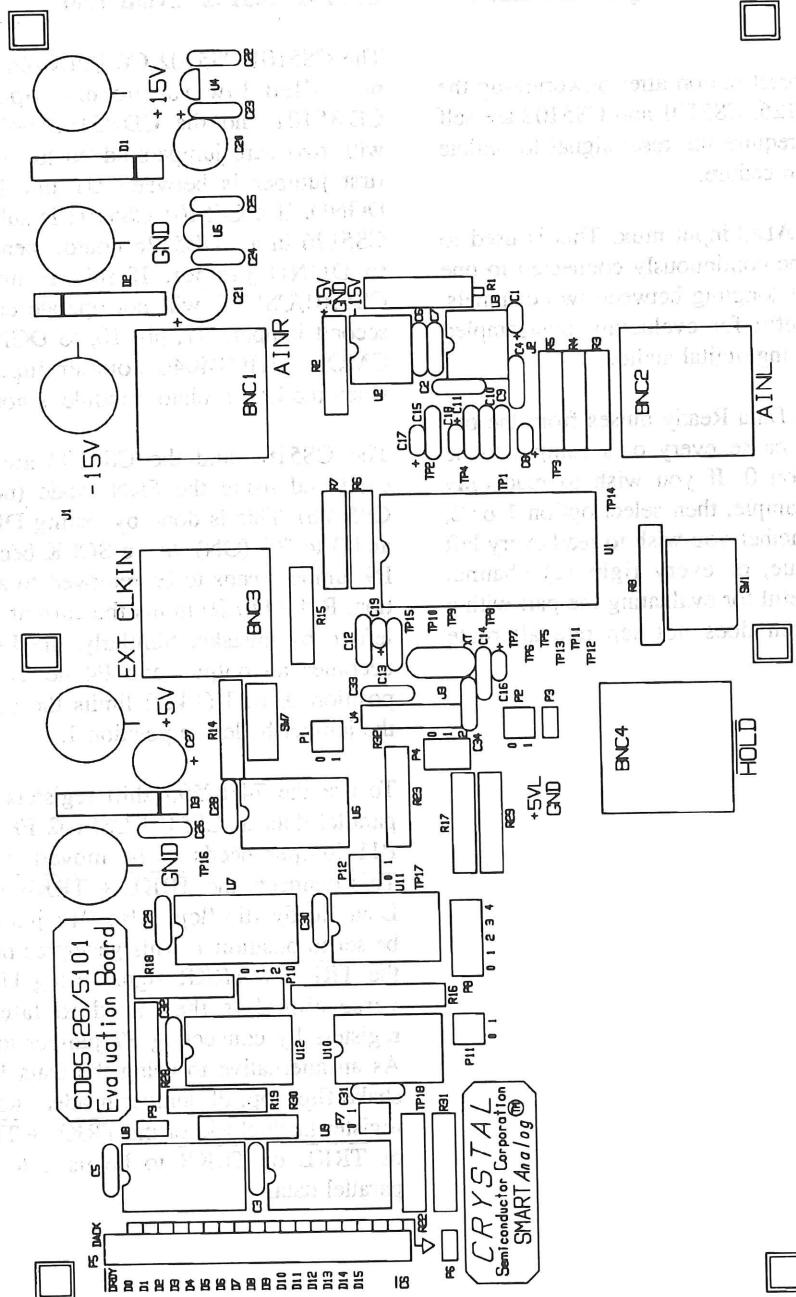
P10 controls the Data Ready pulses from the on-board logic. To cause every data sample to be read, select option 0. If you wish to read only every alternate sample, then select option 1 or 2, depending on whether you wish to read every left (1) channel value, or every right (2) channel value. This is useful for evaluating the part with a test system which does not separate alternate values.

## CS5101/CS5102 Evaluation

The CS5101/CS5102 CRS/ $\overline{\text{FIN}}$  pin (pin 10) must be pulled low for normal operation. The CDB5101 and the CDB5102 will be shipped with two wire jumpers added to the board. The first jumper is between U1 pin 10 (TP6) and DGND. If a CS5101/CS5102 is substituted for a CS5126 in a CDB5126 board, then add the TP6 to DGND jumper. If this is not done, the CS5101/CS5102 will not operate correctly. The second jumper, U7, pin 10, to DGND shorts the CMOS 74HCT4040 counter input to ground when the U6 oscillator module is not used.

The CS5101 and the CS5102 are most easily evaluated using the FRN mode (not present in CS5126). This is done by setting DIP switches 2 and 3 to "0" (ON). Since SCLK becomes output, P9 jumper needs to be removed to avoid contention. R28 (470  $\Omega$ ) limits the current should P9 be left in by mistake. Similarly, the  $\text{L}/\overline{\text{R}}$  select pin becomes an output, and P4 needs to be set to position 0. R23 (1 k $\Omega$ ) limits the current should the jumper be left in position 1.

To use the 74HC595 shift registers to assemble parallel data in CS5101/CS5102 FRN mode, the P11 jumper needs to be moved to position 0. This connects the  $\overline{\text{TRKL}}$  +  $\overline{\text{TRKR}}$  signal to the Data Ready flip-flop. Also P12 jumper needs to be set to position 1. This generates the inverse of the  $\overline{\text{TRKL}}$  +  $\overline{\text{TRKR}}$  signal using U11. This inverse signal is then used to latch the shift registers by connecting P7 jumper to position 1. As an alternative to using the Data Ready handshake flip-flop, P8 jumper header allows the shift register latch clock, or the  $\overline{\text{TRKL}}$  +  $\overline{\text{TRKR}}$  signal, or  $\overline{\text{TRKL}}$  or  $\overline{\text{TRKR}}$  to be used to qualify the parallel data.



**Figure 8. CDB5126/5101/5102 Component Layout**

# 16 & 18-Bit, Stereo A/D Converters for Digital Audio

## Features

- Complete CMOS Stereo A/D System  
Delta-Sigma A/D Converters  
Digital Anti-Alias Filtering  
S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates  
30 kHz to 50 kHz
- Low Noise and Distortion  
95 dB dynamic range, 16-Bit  
97 dB dynamic range, 18-Bit  
100 dB dynamic range, 19-Bit Mono  
0.0015% THD
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering  
0.001dB Passband Ripple  
86dB Stopband Rejection
- Low Power Dissipation: 450 mW  
Power-Down Mode for Portable Applications

## General Description

The CS5326, CS5327, CS5328 & CS5329 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16 or 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

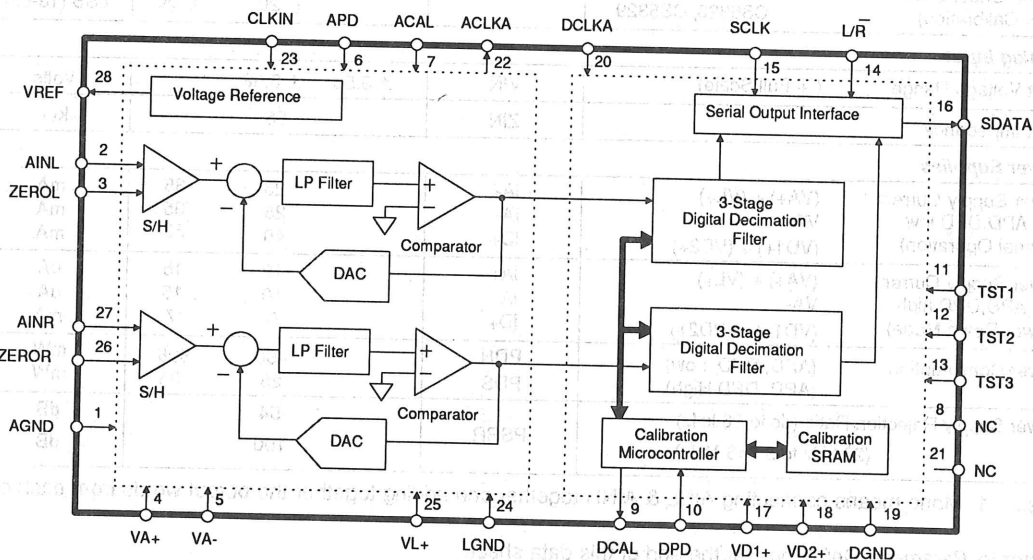
The ADCs use delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5326 & CS5327 are 16-bit ADCs, achieving 95 dB dynamic range. The CS5328 & CS5329 are 18-bit ADCs with 97 dB dynamic range in stereo mode and 100 dB dynamic range in mono mode.

The CS5326 & CS5328 have digital filters which are compatible with CD requirements. The CS5327 & CS5329 have filters which guarantee no aliasing. The filters have linear phase, 0.001 dB passband ripple, and >86 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP.

**ORDERING INFORMATION:** Page 2-143





**ANALOG CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ;  $V_{A+}, V_{L+}, V_{D1+}, V_{D2+} = 5\text{V}$ ;  $V_{A-} = -5\text{V}$ ; Full-Scale Input Sinewave, 4kHz; CLKIN = 6.144MHz; SCLK = 3.072 MHz; Source Impedance =  $50\Omega$  with 10 nF to AGND; Measurement Bandwidth is 10 Hz to 20 kHz; Digital Inputs: Logic 1 = VD+, Logic 0 = DGND; unless otherwise specified.)

unless otherwise specified.)

Parameter*		Symbol	Specification min                      typ                      max		Units
Resolution	CS5326, CS5327 CS5328, CS5329		16		Bits
			18		Bits
<b>Dynamic Performance</b>					
Dynamic Range  (Note 1)	CS5326, CS5327		92.7	95.7	dB
	CS5328, CS5329		94.7	97.1	dB
	Mono CS5328, CS5329			100.1	dB
Signal-to- (Noise + Distortion) (Note 1)	CS5326, CS5327	S/(N+D)	90.7	92.7	dB
	CS5328, CS5329		92.5	94.5	dB
	Mono CS5328, CS5329			97	dB
Total Harmonic Distortion Vin = ± FS Vin = -20 dB		THD	0.003	0.0015 0.001	% %
Interchannel Phase Deviation				0.0001	Degrees
Interchannel Isolation (dc to 20 kHz)			100	106	dB
<b>dc Accuracy</b>					
Interchannel Gain Mismatch				0.01                      0.05	dB
Gain Error				± 1                      ± 5	%
Gain Drift				50	ppm/ ° C
Bipolar Offset Error (After Calibration)	CS5326, CS5327		± 5	± 15	LSB (16-bit)
	CS5328, CS5329		± 20	± 60	LSB (18-bit)
<b>Analog Input</b>					
Input Voltage Range	( ± Full Scale)	VIN	± 3.50	± 3.68	Volts
Input Impedance		ZIN		65	kΩ
<b>Power Supplies</b>					
Power Supply Current with APD,DPD low (Normal Operation)	(VA+) + (VL+)	IA+	25	35	mA
	VA-	IA-	25	35	mA
	(VD1+) + (VD2+)	ID+	40	55	mA
Power Supply Current with APD,DPD high (Power-Down Mode)	(VA+) + (VL+)	IA+	10	15	uA
	VA-	IA-	10	15	uA
	(VD1+) + (VD2+)	ID+	5	7	mA
Power Consumption	(APD, DPD Low)	PDN	450	625	mW
	(APD, DPD High)	PDS	25	35	mW
Power Supply Rejection Ratio (dc to 26 kHz) (26 kHz to 3.046 MHz)		PSRR	54		dB
			100		dB

Notes: 1. Mono means connecting AINL & AINR together and adding together the output words from each channel

\* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

### DIGITAL FILTER CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ ;  $V_{A+}$ ,  $V_{L+}$ ,  $VD1+$ ,  $VD2+ = 5V \pm 5\%$ ;  $V_{A-} = -5V \pm 5\%$ ;  $CLKIN = 6.144\text{MHz}$ )

Parameter	Symbol	Min	Typ	Max	Units
Passband (-3 dB)	CS5326, CS5328	0		23.5	kHz
Passband (-3 dB)	CS5327, CS5329	0		21.6	kHz
Passband (-0.001 dB)	CS5326, CS5328	0		21.8	kHz
Passband (-0.001 dB)	CS5327, CS5329	0		20.0	kHz
Passband Ripple				0.001	dB
Stopband	CS5326, CS5328	26		3046	kHz
Stopband	CS5327, CS5329	24		3052	kHz
Stopband Attenuation (Note 2)		86			dB
Group Delay	$t_{gd}$		4274/CLKIN		s
Group Delay Variation vs. Frequency	$\Delta t_{gd}$			0.0	us

Notes: 2. The analog modulator samples the input at 3.072MHz for a CLKIN of 6.144MHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for  $n \times 3.072\text{MHz} \pm 21.8\text{kHz}$  for the CS5326 & CS5328, or  $n \times 3.072\text{MHz} \pm 20.0\text{kHz}$  for the CS5327 & CS5329, where  $n = 0, 1, 2, 3, \dots$ ).

### DIGITAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ ;  $V_{A+}$ ,  $V_{L+}$ ,  $VD1+$ ,  $VD2+ = 5V \pm 5\%$ ;  $V_{A-} = -5V \pm 5\%$ )

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (CLKIN)	$V_{IH}$	$(VD+) - 1.0$	-	-	V
Low-Level Input Voltage (CLKIN)	$V_{IL}$	-	-	1.0	V
High-Level Input Voltage (except CLKIN)	$V_{IH}$	70%VD+	-	-	V
Low-Level Input Voltage (except CLKIN)	$V_{IL}$	-	-	30% VD+	V
High-Level Output Voltage at $I_O = -20\mu\text{A}$	$V_{OH}$	4.4	-	-	V
Low-Level Output Voltage at $I_O = 20\mu\text{A}$	$V_{OL}$	-	-	0.1	V
Input Leakage Current	$I_{in}$	-	1.0	-	$\mu\text{A}$

### RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:					
Positive Digital	$VD1+, VD2+$	4.75	5.0	5.25	V
Positive Logic	$V_{L+}$	4.75	5.0	$V_{A+}$	V
Positive Analog	$V_{A+}$	4.75	5.0	5.25	V
Negative Analog	$V_{A-}$	-4.75	-5.0	-5.25	V
Analog Input Voltage (Note 3)	$V_{AIN}$	-3.68	-	3.68	V
CLKIN Frequency	$f_{CLK}$	3.84	-	6.4	MHz
SCLK Frequency	$f_{SCLK}$	$f_{CLK} / 2$	-	$f_{CLK}$	Hz
L/R Frequency	$f_{L/R}$	$f_{CLK} / 128$	-	$f_{CLK} / 128$	Hz

Notes: 3. The ADCs accept input voltages up to the analog supplies ( $V_{A+}$ ,  $V_{A-}$ ). They will produce a positive full-scale output for inputs above 3.68 V and negative full-scale output for inputs below -3.68 V. These values are subject to the gain error tolerance specification.

## SWITCHING CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ ;  $V_{A+}$ ,  $V_{L+}$ ,  $V_{D1+}$ ,  $V_{D2+} = 5V \pm 5\%$ ;  $V_{A-} = -5V \pm 5\%$ ; Inputs: Logic 0 = 0V, Logic 1 =  $V_{D+}$ ;  
 $C_L = 20\text{ pF}$ )

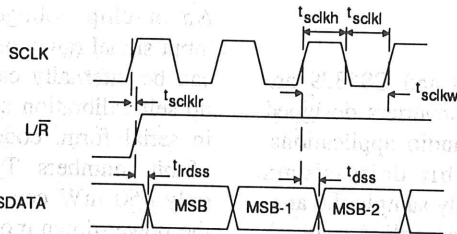
Parameter	Symbol	Min	Typ	Max	Units
CLKIN Period	$t_{clkw}$	155	-	260	ns
CLKIN Low	$t_{ckl}$	50	-	-	ns
CLKIN High	$t_{cklh}$	50	-	-	ns
CLKIN Rising to ACLKA edge (Note 4)	$t_{clka}$	40	-	100	ns
ACLKA Falling to $L/\bar{R}$ Edge (Note 4)	$t_{aclr}$	-140	-	140	ns
CLKIN Rising to $L/\bar{R}$ Edge (Note 4)	$t_{clr}$	-10	-	170	ns
ACLKA to CLKIN phase correct		-10	-	30	
ACLKA to CLKIN phase unknown					
SCLK Pulse Width Low	$t_{sckl}$	60	-	-	ns
SCLK Pulse Width High	$t_{sckh}$	60	-	-	ns
SCLK Period	$t_{sckw}$	155	-	-	ns
SCLK Rising to SDATA Valid	$t_{dss}$	-	-	45	ns
$L/\bar{R}$ edge to MSB Valid	$t_{lrdss}$	-	-	50	ns
SCLK Rising to $L/\bar{R}$ edge	$t_{scklr}$	-40	-	40	ns
DPD, APD pulse width	$t_{pd}$	150	-	-	ns
CLKIN Falling to APD Falling	$t_{apdclk}$	-30	-	30	ns

Notes: 4. It is recommended that  $L/\bar{R}$  be generated by dividing ACLKA by 64. If CLKIN is used to generate  $L/\bar{R}$ , a longer CLKIN to  $L/\bar{R}$  delay may be tolerated if the phase of ACLKA is determined through the use of the APD pin. When high, the APD pin resets the divide-by-two circuit that generates ACLKA from CLKIN (that is, ACLKA is reset to "0"). APD should be brought low on a falling edge of CLKIN. This falling edge should be chosen such that  $L/\bar{R}$  edges nominally occur at ACLKA falling edges.

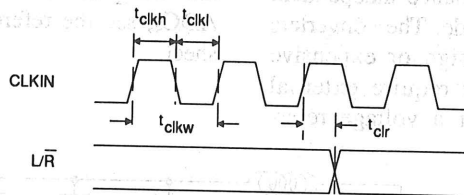
## ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	+6.0	V
	Negative Analog	VA-	+0.3	-6.0	V
	Positive Logic	VL+	-0.3	(VA+) + 0.3	V
	Positive Digital	VD1+,VD2+	-0.3	+6.0	V
Input Current, Any Pin Except Supplies		I <sub>in</sub>	-	± 10	mA
Analog Input Voltage (AIN and ZERO pins)		V <sub>INA</sub>	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V <sub>IND</sub>	-0.3	(VD+) + 0.3	V
Ambient Temperature (power applied)		T <sub>A</sub>	-55	+125	°C
Storage Temperature		T <sub>stg</sub>	-65	+150	°C

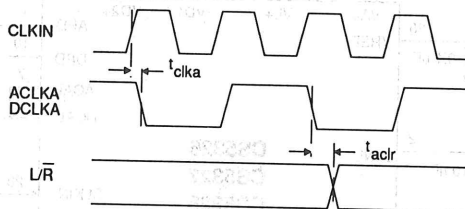
WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
 Normal operation is not guaranteed at these extremes.



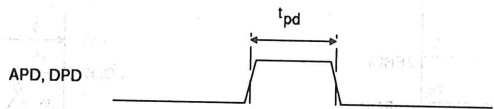
### Serial Data Timing



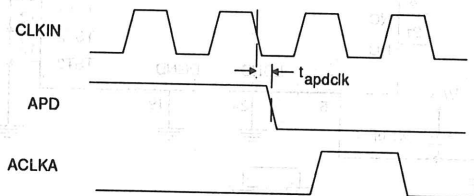
### Channel Selection Timing Using L/R Derived From CLKIN/128



### Channel Selection Timing Using L/R Derived from ACLKA/64



### Power Down Timing



### ACLKA Phase Determination using APD

### GENERAL DESCRIPTION

The CS5326, CS5327, CS5328 and CS5329 are 16 & 18-bit, 2-channel A/D converters designed specifically for stereo digital audio applications. The devices use two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a  $64\times$  sampling rate. A three-stage digital filter then constructs pairs of 16-bit or 18-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for an input signal range of  $\pm 3.68$  volts. Any zero offset can be internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16 or 18-bit numbers. Typical power consumption of only 450 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside these ADCs, see the references at the end of this data sheet.

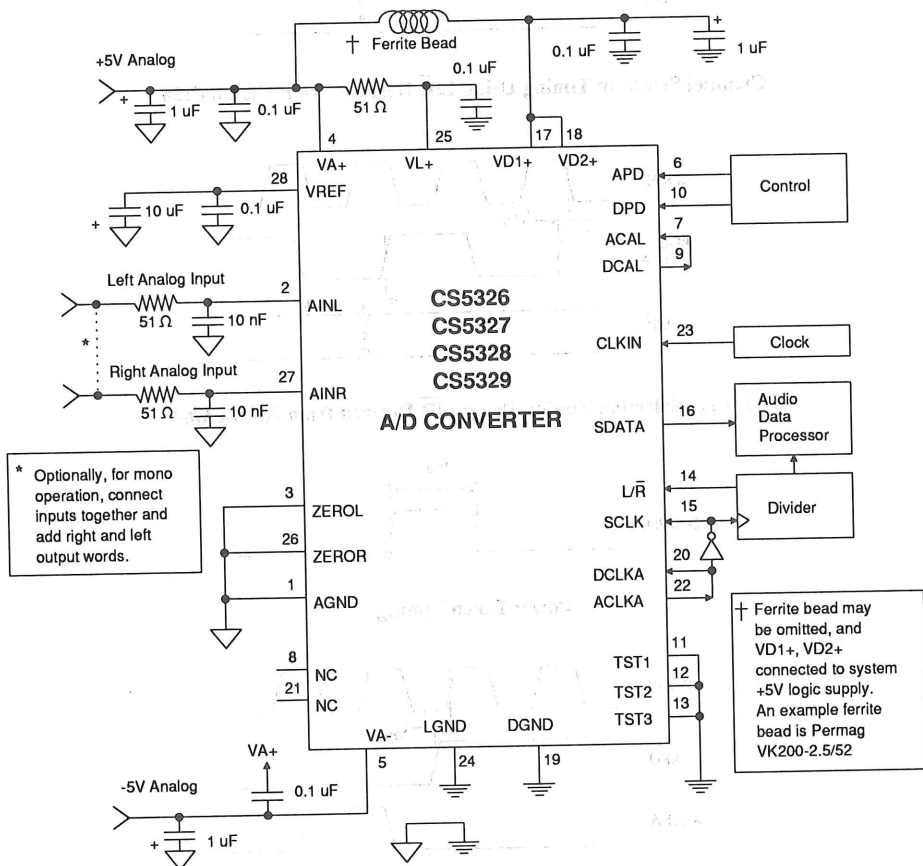


Figure 1. Typical Connection Diagram

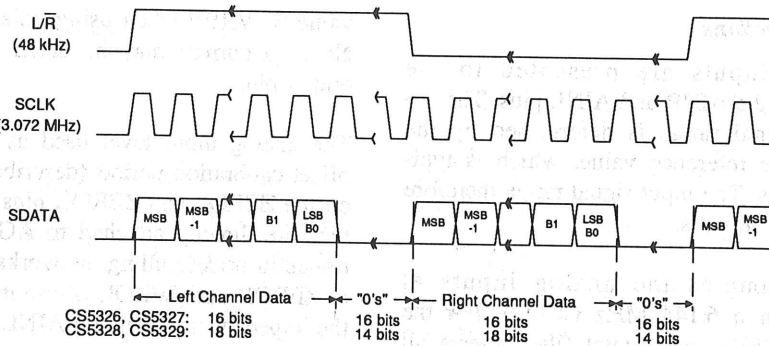


Figure 2. Data Output Timing

### SYSTEM DESIGN WITH THE CS5326/7/8/9

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required.

#### Clocks and Data Output Format

All timing and control inputs to the ADC can be easily generated from a master system clock. This clock, connected to the CLKIN pin on the device, must be exactly equal to 128 times the desired output word rate. Standard digital audio rates are 32 kHz, 44.1 kHz and 48 kHz, requiring master clock rates of 4.096 MHz, 5.6448 MHz and 6.144 MHz, respectively.

The CLKIN signal should be greater than 4 volts for a logic one and less than 1 volt for a logic zero. This is to minimize any clock related jitter in the sampling process, which can smear high frequency signals. Indeed, a low jitter (such as a crystal-based) clock is recommended.

Data bits are clocked out via the SDATA pin using the SCLK and L/R inputs. The rising edge of SCLK causes the part to output each bit, except the MSB, which is clocked out by the L/R edge. Even so, a rising SCLK edge must occur

coincident (within the timing tolerance) with the L/R edge for internal housekeeping purposes.

It is recommended to connect SCLK to ACLKA, as shown in Figure 1. Fourteen or sixteen trailing zero's will be clocked out on SDATA as part of each data word, as shown in Figure 2. ACLKA's frequency is the analog modulator sampling rate, and if a lower frequency is used for SCLK, slight degradation of the ADC dynamic range can occur due to interference effects.

Selection of left channel or right channel data is accomplished using the L/R input pin. The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/R cycle represent simultaneously sampled inputs.

Rising edges of L/R are used to synchronize the digital filter; therefore L/R's frequency must be CLKIN/128. It is preferable to generate L/R by dividing ACLKA by 64. If CLKIN is used to generate L/R, it is best to determine the phase of ACLKA through the use of the APD pin. (When high, the APD pin resets the internal divide-by-two circuit that generates ACLKA. See Figure 4 for an example circuit.) If ACLKA phase is left indeterminate, then the CLKIN to L/R delay must be shorter than the smaller delay shown in the Switching Characteristics table (see Note 4.).



### Analog Connections

The analog inputs are presented to the modulators via the AINR and AINL pins. The analog input signal range is determined by the internal voltage reference value, which is typically -3.68 volts. The input signal range therefore is typically  $\pm 3.68$  volts.

The ADC samples the analog inputs at 3.072 MHz for a 6.144 MHz CLKIN. For the CS5326 & CS5328 the digital filter rejects all noise between 26 kHz and (3.072 MHz-26 kHz). For the CS5327 & CS5329 the digital filter rejects all noise between 24 kHz and (3.072 MHz-24 kHz). However, the filter will not reject frequencies right around 3.072 MHz. Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a  $51\ \Omega$  resistor in series with the analog input, and a 10 nF NPO or COG capacitor to ground will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins.

The on-chip voltage reference output is brought out to the VREF pin. A 10  $\mu$ F electrolytic capacitor in parallel with a 0.1  $\mu$ F ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Note the negative

value of VREF when using polarized capacitors. No load current may be taken from the VREF output pin.

The analog input level used as zero during the offset calibration period (described later) is input on the ZEROL and ZEROR pins. Typically, these pins are directly attached to AGND. For the ultimate in offset nulling, networks can be attached to ZEROR and ZEROL whose impedances match the impedances present on AINL and AINR.

### Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 20 mW. In addition, exiting the power-down state initiates the offset calibration procedure. This can be important for digital audio applications since any initial offset manifests itself as an audible power-on click.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle, whereas APD going low sets the phase of the ACLKA signal. If not using the power down feature and if not using APD to set the phase of ACLKA, APD should be tied to ground. When using the power down feature, DPD and APD may be tied together if the capacitor on VREF is not greater than 10  $\mu$ F, as stated in the "Power-Up Considerations" section.

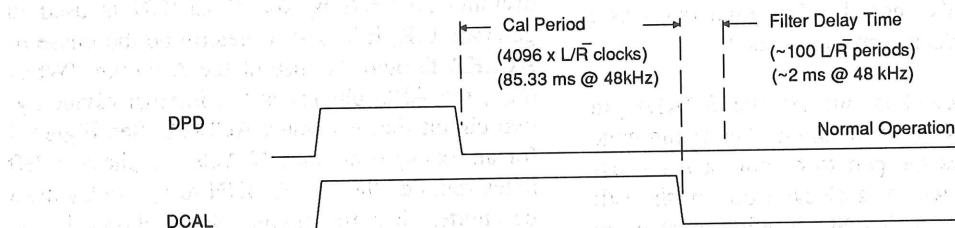


Figure 3. Initial Calibration Cycle Timing

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AINL and AINR) or the zero pins (ZEROL and ZEROR) depending on the state of the ACAL pin. With ACAL low, the analog input pin voltages are measured, and with ACAL high, the zero pin voltages are measured.

As shown in Figure 3, the DCAL output is high during calibration, which takes 4096  $L/\bar{R}$  clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage on ZEROR and ZEROL. These should be connected directly to ground or through a network matched to that present on the analog input pins. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to ground the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present on the front end.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any power-on click that might otherwise be experienced. A short delay of approximately 100 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals. The transition is simply the natural filter response and is, of course, graceful.

### ***Power-up Considerations***

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace

potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference, however, can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/ $\mu$ F. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10  $\mu$ F. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

### ***Grounding and Power Supply Decoupling***

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows powering the part from single  $\pm 5$  volt supplies. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. The VREF decoupling capacitors, particularly the 0.1  $\mu$ F, must be positioned to minimize the electrical path from VREF to Pin 1 AGND and to minimize the path between VREF and the capacitors.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

### Multiple ADC's

In systems where multiple ADC's are used, care must be taken to ensure that the ACLKA phases are synchronized if simultaneous sampling is desired. In the absence of this synchronization, the sampling difference could be one CLKIN cycle (typically 162 ns). If this difference is unacceptable, the parts may be synchronized to within several nanoseconds by using the circuit shown in Figure 4. This circuit ensures that when the ADC's come out of power-down mode, ACLKA will have the same phase between all ADC's. The APD signal is used to reset the internal divide-by-two flip-flop which generates ACLKA. The circuit also ensures that  $L/\overline{R}$  and SCLK occur at the correct time.

## PERFORMANCE

### FFT Tests

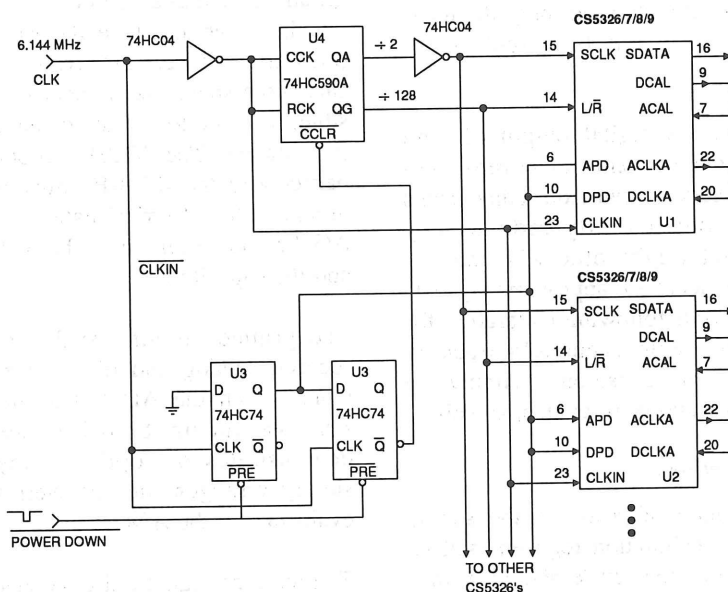
For FFT based tests, a very pure sine wave is presented to the ADC, and an FFT analysis is

performed on the output data. The resulting spectrum is a measure of the performance of the ADC.

Figure 5 shows the spectral purity of the CS5326 with a 1 kHz, -10 dB input. Notice the low noise floor, the absence of any harmonic distortion, and the Dynamic Range value of 94.63 dB.

Figure 6 shows the CS5326 high frequency performance. The input signal is a -10 dB, 9 kHz sine wave. Notice the small 2nd harmonic at -112 dB.

Figure 7 shows the low-level performance of the CS5326. Notice the lack of any distortion components. Traditional R-2R ladder based ADC's can have problems with this test, since differential non-linearities around the zero point become very significant. Figure 8 shows the same very low input amplitude performance, but at 9kHz input frequency.



**Figure 4. Connections for Synchronization of Multiple CS5326/7/8/9 ADC's.**

Figure 9 shows the CS5327 FFT plot with an input signal of 1 kHz at -10 dB. This is very similar to the CS5326 plot, but notice the reduction in the noise floor between 22 kHz and

24 kHz. This is caused by the digital filter attenuating the noise in its transition band.

Figure 10 shows a plot of Signal to (Noise + Distortion) versus input amplitude relative to full

2

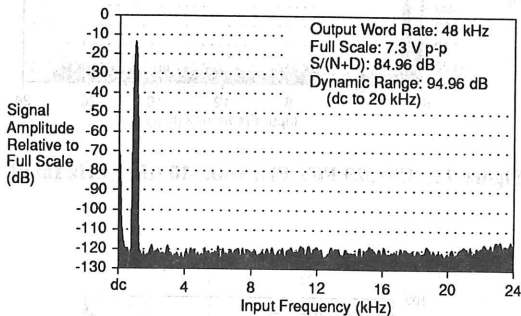


Figure 5. CS5326 FFT Plot with -10 dB, 1 kHz Input

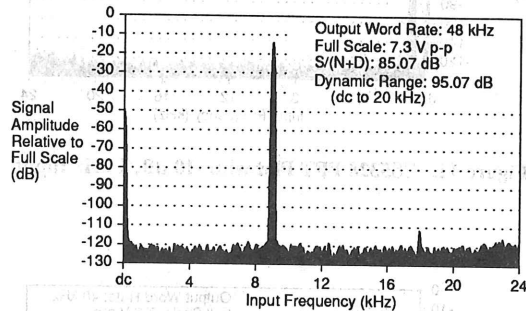


Figure 6. CS5326 FFT Plot with -10 dB, 9 kHz Input

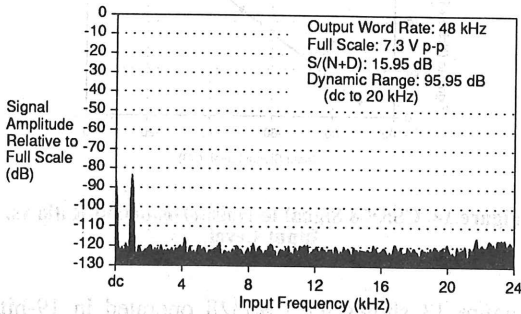


Figure 7. CS5326 FFT Plot with -80 dB, 1 kHz Input

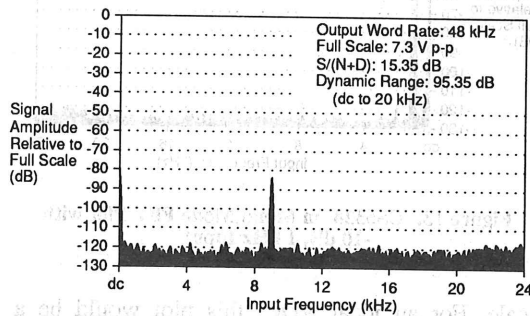


Figure 8. CS5326 FFT Plot with -80 dB, 9 kHz Input

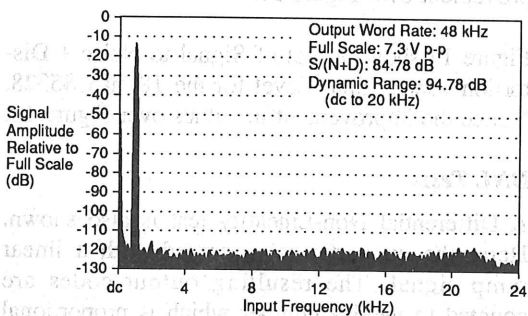


Figure 9. CS5327 FFT Plot with -10 dB, 1 kHz Input

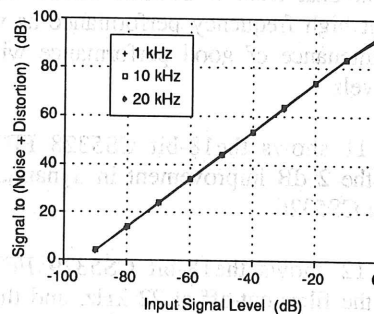


Figure 10. CS5326, CS5327 Signal to Noise+Distortion Ratio vs. Input Level

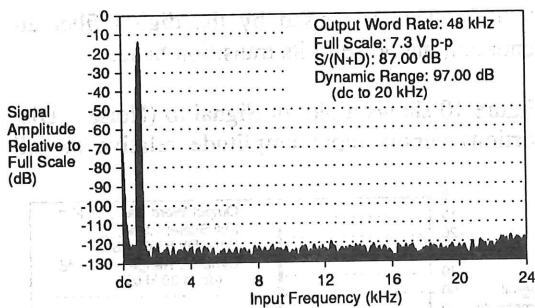


Figure 11. CS5328 FFT Plot with -10 dB, 1 kHz Input

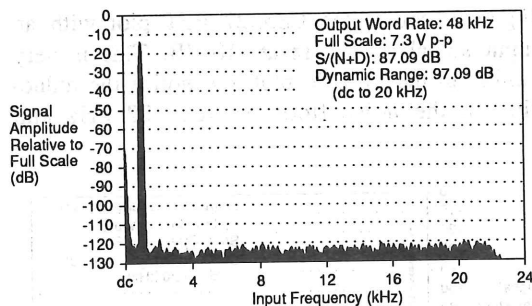


Figure 12. CS5329 FFT Plot with -10 dB, 1 kHz Input

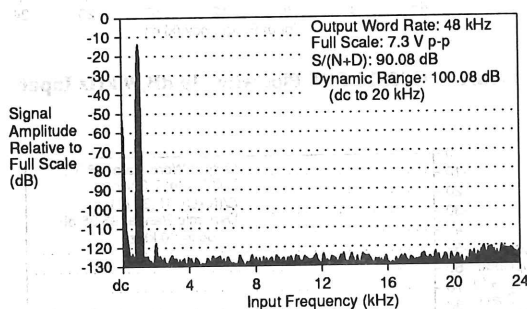


Figure 13. CS5328 in Mono Mode FFT Plot with -10 dB, 1 kHz Input

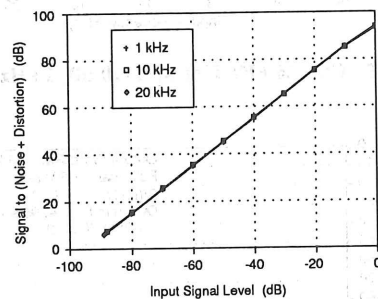


Figure 14. CS5328 Signal to Noise+Distortion Ratio vs. Input Level

scale. For an ideal ADC, this plot would be a straight line at 45° for all input frequencies between dc and half the output word rate. The measured data from a CS5326 shows both the excellent high frequency performance as well as the maintenance of good performance with low input levels.

Figure 11 shows the 18-bit CS5328 FFT plot. Notice the 2 dB improvement in dynamic range over the CS5326.

Figure 12 shows the 18-bit CS5329 FFT plot. Notice the filter cut-off at 22 kHz, and the 2 dB improvement in dynamic range over the CS5327.

Figure 13 shows the CS5328 operated in 19-bit mono mode, with the two inputs joined together, and the output words added. Notice the 3 dB improvement over Figure 11.

Figure 14 shows a plot of Signal to Noise + Distortion versus Input Level for the 18-bit CS5328. Notice the improvement in values over Figure 10.

### DNL Tests

A Differential Non-Linearity test is also shown. Here, the converter is presented with a linear ramp signal. The resulting output codes are counted to yield a number which is proportional to the codewidth. A plot of codewidth versus code graphically illustrates the uniformity of the

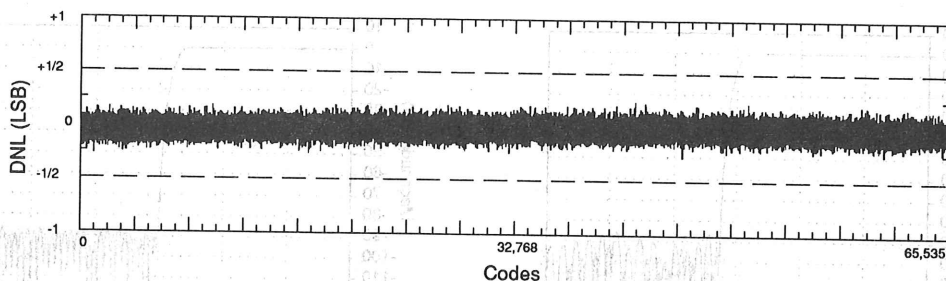


Figure 15. CS5326 Differential Non-Linearity Plot

codewidths. Figure 15 shows the excellent Differential Non-Linearity of the CS5326. This plot displays the worst case positive and negative errors in each of 512 groups of 128 codes. Codewidths typically are within  $\pm 0.2$  LSB's of ideal. A delta-sigma modulator based ADC has no inherent mechanism for generating DNL errors. The residual small deviations shown in Figure 10 are a result of noise. Nevertheless, the performance shown is extremely good, and is superior to typical R-2R ladder based designs.

### Digital Filter

Figures 16 through 21 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz, with a CLKIN frequency of 6.144 MHz. The filter frequency response will scale precisely with changes in CLKIN frequency. The passband ripple is flat to  $\pm 0.001$  dB maximum. Stopband rejection is greater than 86 dB.

Figures 16,18 & 20 show the CS5326 and CS5328 filter characteristics. Figure 20 is an expanded view of the transition band.

Figures 17,19 & 21 show the CS5327 and CS5329 filter characteristics. Figure 21 is an expanded view of the transition band. Notice how the filter enters the stopband at exactly 24 kHz, which is half the output word rate, thereby guaranteeing no aliasing.

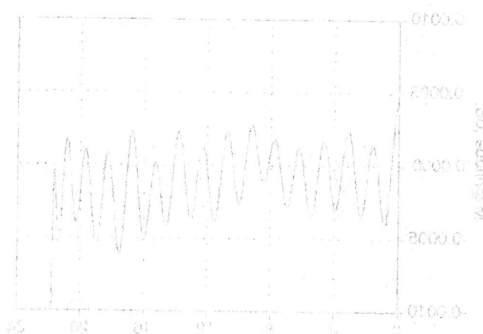


Figure 16. CS5326 Filter Frequency Response

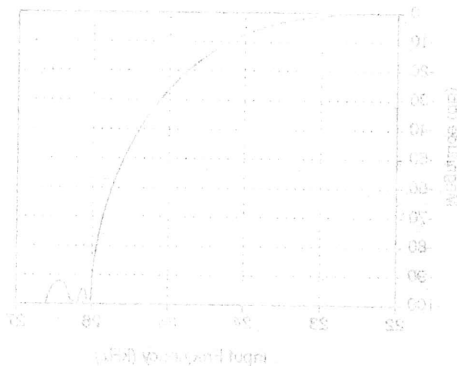
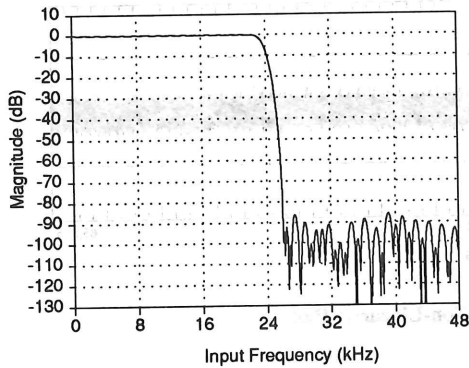
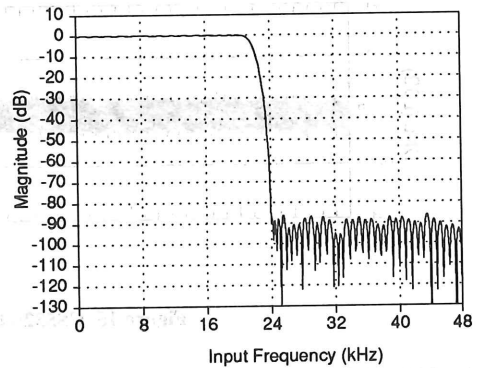


Figure 17. CS5327 Filter Frequency Response

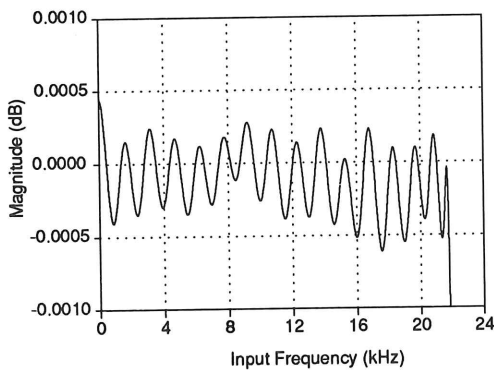




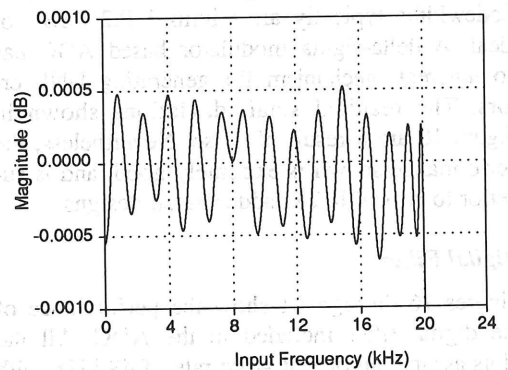
**Figure 16. CS5326 /8 Digital Filter Stopband Rejection**



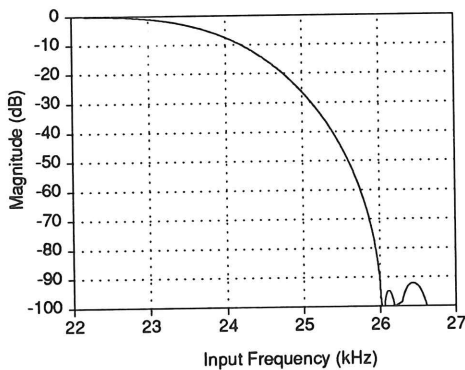
**Figure 17. CS5327/9 Digital Filter Stopband Rejection**



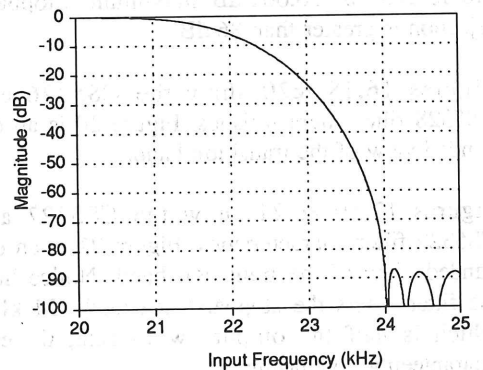
**Figure 18. CS5326/8 Digital Filter Passband Ripple**



**Figure 19. CS5327/9 Digital Filter Passband Ripple**



**Figure 20. CS5326/8 Digital Filter Transition Band**



**Figure 21. CS5327/9 Digital Filter Transition Band**

### PIN DESCRIPTIONS

ANALOG GROUND	AGND	1	28	VREF	VOLTAGE REFERENCE OUTPUT
LEFT CHANNEL ANALOG INPUT	AINL	2	27	AINR	RIGHT CHANNEL ANALOG INPUT
LEFT CHANNEL ZERO INPUT	ZEROL	3	26	ZEROR	RIGHT CHANNEL ZERO INPUT
POSITIVE ANALOG POWER	VA+	4	25	VL+	ANALOG SECTION LOGIC POWER
NEGATIVE ANALOG POWER	VA-	5	24	LGND	ANALOG SECTION LOGIC GROUND
ANALOG POWER DOWN INPUT	APD	6	23	CLKIN	MASTER CLOCK INPUT
ANALOG CALIBRATE INPUT	ACAL	7	22	ACLKA	ANALOG SECTION CLOCK OUTPUT
NO CONNECT	NC	8	21	NC	NO CONNECT
DIGITAL CALIBRATE OUTPUT	DCAL	9	20	DCLKA	DIGITAL SECTION CLOCK INPUT
DIGITAL POWER DOWN INPUT	DPD	10	19	DGND	DIGITAL GROUND
TEST	TST1	11	18	VD2+	DIGITAL SECTION POSITIVE POWER
TEST	TST2	12	17	VD1+	DIGITAL SECTION POSITIVE POWER
TEST	TST3	13	16	SDATA	SERIAL DATA OUTPUT
LEFT/RIGHT SELECT INPUT	L/R	14	15	SCLK	SERIAL DATA CLOCK INPUT

2

### Power Supply Connections

#### VA+ - Positive Analog Power, PIN 4.

Positive analog supply. Nominally +5 volts.

#### VL+ - Positive Logic Power, PIN 25.

Positive logic supply for the analog section. Nominally +5 volts.

#### VA- - Negative Analog Power, PIN 5.

Negative analog supply. Nominally -5 volts.

#### AGND - Analog Ground, PIN 1.

Analog ground reference.

#### LGND - Logic Ground, PIN 24

Ground for the logic portions of the analog section.

#### VD1+, VD2+ - Positive Digital Power, PINS 17, 18.

Positive supply for the digital section. Nominally +5 volts.

#### DGND - Digital Ground, PIN 19.

Digital ground for the digital section.

### Analog Inputs

#### AINL, AINR - Left and Right Channel Analog Inputs, PINS 2, 27

Analog input connections for the left and right input channels. Nominally  $\pm 3.68$  volts full scale.

**ZEROL, ZEROR - Zero Level Inputs for Left and Right Channels, PINS 3, 26.**

Analog zero level inputs for the left and right channels. The levels present on these pins can be used as zero during the offset calibration cycle. Normally connected to AGND, optionally through networks matched to the analog input networks..

**Analog Outputs****VREF - Voltage Reference Output, PIN 28.**

Nominally -3.68 volts. Normally connected to a 0.1 $\mu$ F ceramic capacitor in parallel with a 10 $\mu$ F or larger electrolytic capacitor. Note the negative output polarity.

**Digital Inputs****CLKIN - Master Input Clock, PIN 23.**

This clock is internally divided by 2 to set the modulators sample rate. Sampling rates, output rates, and digital filter characteristics scale to CLKIN frequency. CLKIN frequency of 6.144 MHz corresponds to an output word rate of 48 kHz per channel.

**DCLKA - Digital Section Input Clock, PIN 20.**

This clock is used to clock the modulator output data into the digital section. Must be connected to ACLKA.

**SCLK - Serial Output Data Clock, PIN 15.**

Data bits are output on the rising edge of SCLK.

**L/R - Left/Right Select, PIN 14.**

Select the left or right channel for output on SDATA. The rising edge of L/R starts the MSB of the left channel data. Thereafter, CLKIN, SCLK and L/R should run synchronously. L/R must be equal to CLKIN/128. Although the outputs of each channel are transmitted at different times, the two words in a L/R cycle represent simultaneously sampled analog inputs.

**APD - Analog Power Down, PIN 6.**

Analog section power-down command. When high the analog circuitry is in power-down mode. It also causes the analog section to reset the clock output (ACLKA). APD is normally connected to DPD when using the power down feature.

**DPD - Digital Power Down, PIN 10**

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 L/R periods (85.33 ms with a 6.144 MHz clock). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD. A calibration cycle should always be initiated after applying power to the supply pins.

**ACAL - Analog Calibrate, PIN 7.**

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to ZEROL and ZEROR inputs respectively. May be connected to DCAL.

**Digital Outputs****ACLKA - Analog Section Output Clock, PIN 22.**

This clock is  $CLKIN/2$ . It is used by the digital section to clock in the modulator output data. ACLKA must be connected to DCLKA. The phase of ACLKA may be reset by using APD.

**SDATA - Serial Data Output, PIN 16.**

Data bits are presented MSB first, in 2's complement format.

**DCAL - Digital Calibrate Output, PIN 9.**

This pin rises immediately upon entering the power-down state (DPD brought high). It returns low 4096  $L/R$  periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 6.144 MHz CLKIN). May be connected to ACAL. (See Figure 3)

**Miscellaneous****NC - No Connection, PINS 8,21.**

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

**TST1, TST2, TST3 -Test Inputs, PINS 11, 12, 13.**

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

**PARAMETER DEFINITIONS**

**Resolution** - The total number of possible output codes is equal to  $2^N$ , where N = the number of bits in the output word for each channel.

**Signal-to-Noise plus Distortion Ratio** - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

**Total Harmonic Distortion** - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

**Dynamic Range** - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

**Interchannel Phase Deviation** - The difference between the left and right channel sampling times.

**Interchannel Isolation** - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

**Interchannel Gain Mismatch** - The gain difference between left and right channels. Units in decibels.

**Gain Error** - The deviation of the gain value from the typical number given in the analog specifications table.

**Gain Drift** - The change in gain value with temperature. Units in ppm/°C.

**Bipolar Offset Error** - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

**Differential Non-Linearity** - The deviation of a code's width from the ideal width. Units in LSB's.

### REFERENCES (All reprinted in the back of this data book)

- 1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.
- 2) "The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.
- 3) "An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

2

### Ordering Guide

Model	Resolution	Filter Enters Stopband	Temperature	Package
CS5326-KP	16-bits	26 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5327-KP	16-bits	24 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5328-KP	18-bits	26 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5329-KP	18-bits	24 kHz	0°C to 70 °C	28-pin Plastic DIP
CDB5326	CS5326 Evaluation Board			
CDB5327	CS5327 Evaluation Board			
CDB5328	CS5328 Evaluation Board			
CDB5329	CS5329 Evaluation Board			



## Evaluation Board for CS5326, CS5327, CS5328 and CS5329

### Features

- Demonstrates recommended layout and grounding arrangements
- CS8402 Generates AES/EBU, S/PDIF & CP-340 Compatible Digital Audio
- Buffered Serial Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

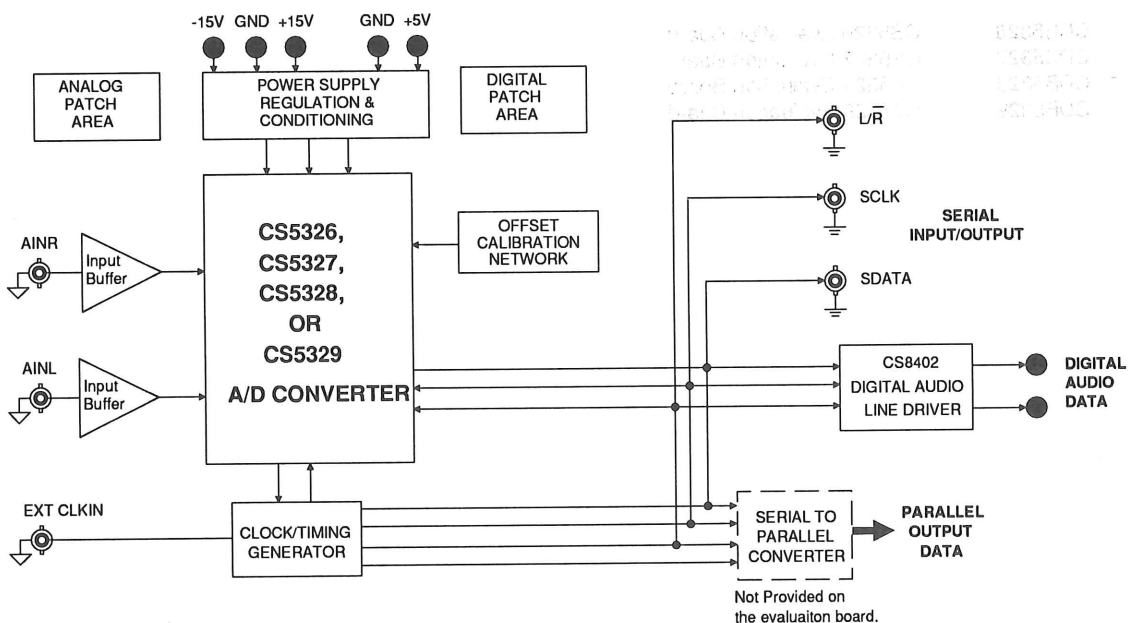
### General Description

The CDB5326 and CDB5327 evaluation boards allow fast evaluation of the CS5326 and CS5327 16-bit, stereo A/D converters. The CDB5328 and CDB5329 evaluation boards allow fast evaluation of the CS5328 and CS5329 18-bit, stereo A/D converters. The boards generate all converter timing signals and provide a serial output interface. Evaluation requires a digital signal processor, a low-distortion signal source, and a power supply.

The evaluation boards may also be configured to accept external timing signals for operation in a user application during system development.

### ORDERING INFORMATION:

CDB5326, CDB5327, CDB5328, CDB5329



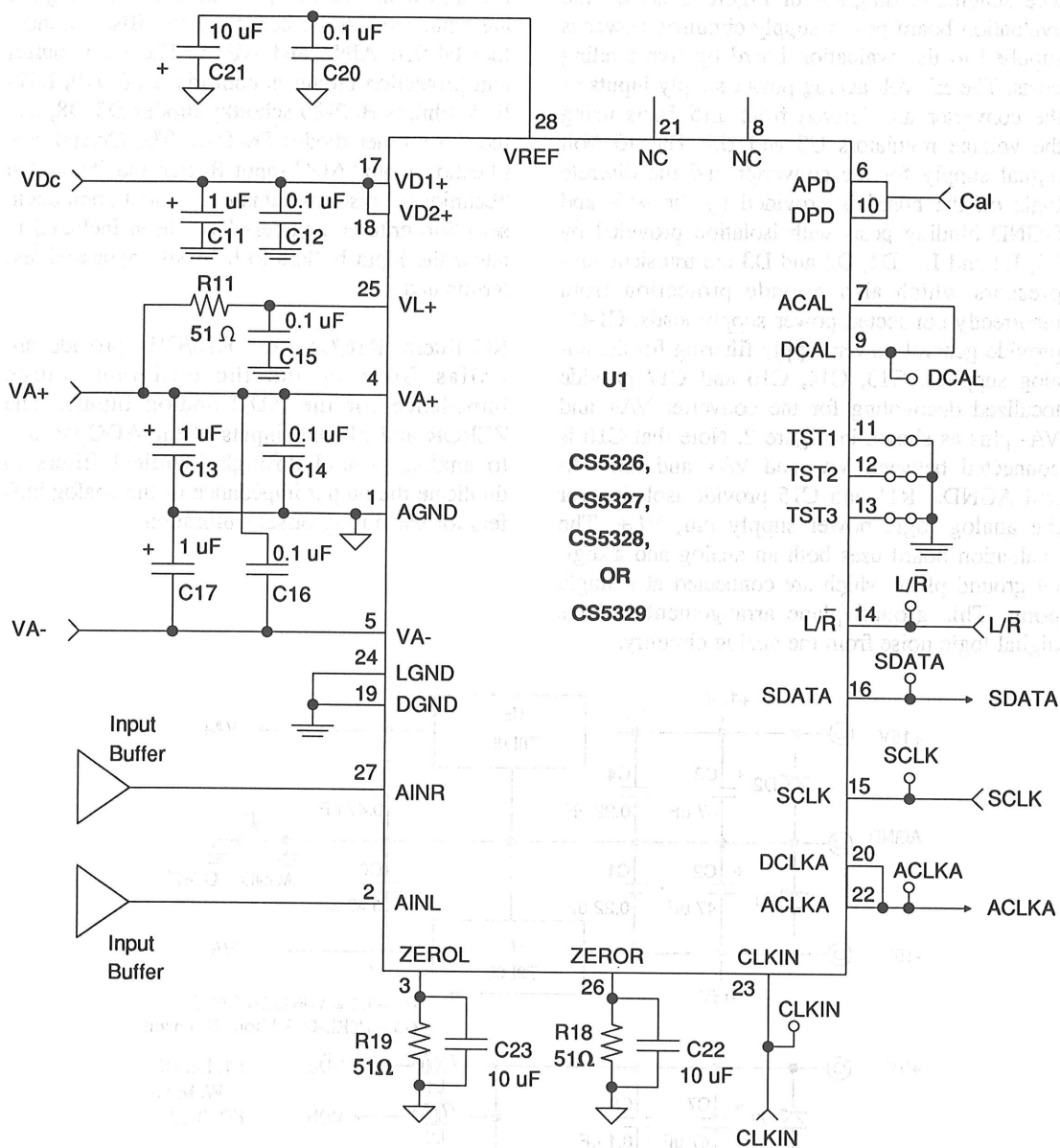


Figure 1. ADC Connections

## Power Supply Circuitry

The schematic diagram in Figure 2 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by five binding posts. The  $\pm 15$  Volt analog power supply inputs of the converter are derived from  $\pm 15$  Volts using the voltage regulators U3 and U5. The +5 Volt digital supply for the converter and the discrete logic on the board is provided by the +5V and DGND binding posts with isolation provided by L1, L2 and L3. D1, D2 and D3 are transient suppressors which also provide protection from incorrectly connected power supply leads. C1-C6 provide general power supply filtering for the analog supplies. C13, C14, C16 and C17 provide localized decoupling for the converter VA+ and VA- pins as shown in Figure 2. Note that C16 is connected between VA- and VA+ and not VA- and AGND. R11 and C15 provide isolation for the analog logic power supply pin, VL+. The evaluation board uses both an analog and a digital ground plane which are connected at a single point. This ground plane arrangement isolates digital logic noise from the analog circuitry.

## Analog Input Buffer and Protection Circuitry

As shown in Figure 2, the analog input signals are connected to the board via the BNC connectors labeled AINL and AINR. The input buffer and protection circuit is comprised of U10, R12-R15, Philips BAT-85 schottky diodes D5-D8, and the 5.6V zener diodes D9-D10. The Crystal Application Note "ADC Input Buffer and Protection Techniques" discusses this circuit and component selection criteria. Jumpers have been included to allow the input buffers to be easily bypassed and terminated.

RC filters, R16/C18 and R18/C19, provide antialias filtering and the optimum source impedance for the ADC analog inputs. The ZEROR and ZEROL inputs of the ADC are tied to analog ground through identical filters to duplicate the output impedance of the analog buffers for use during offset calibration.

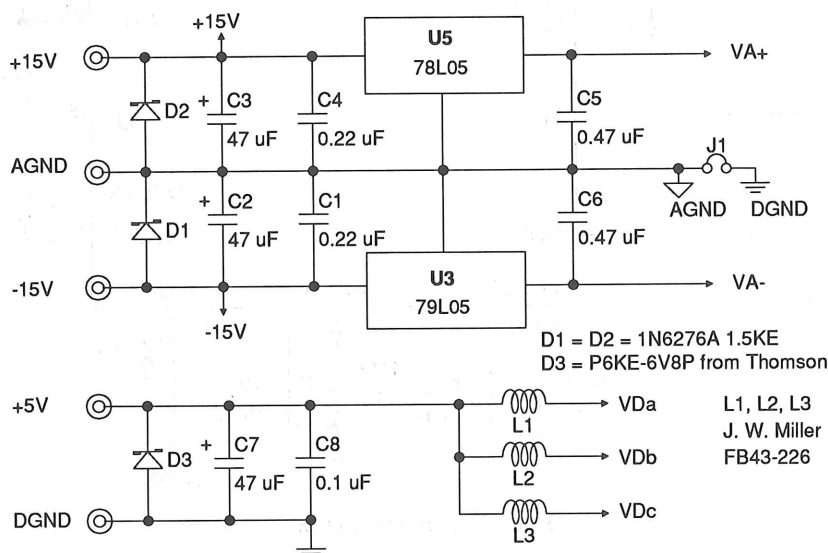


Figure 2. Power Supply Circuitry

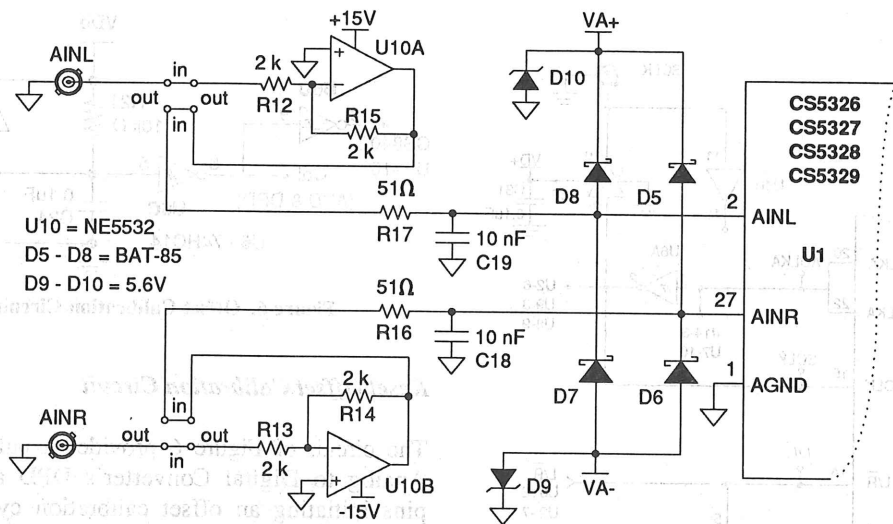


Figure 3. ADC Input Buffer and Protection Circuitry

### CLOCK/TIMING GENERATOR

A 12.288 MHz clock signal is provided by the onboard oscillator X1. U9B performs a divide by 2 of the clock signal to supply a 6.144 MHz clock to the ADC and the Digital Audio Line Driver to support a 48kHz sample rate. An external master clock may be connected to the EXTCLKIN BNC connector if the onboard oscillator is removed.

As recommended in the converter's data sheet, ACLKA is inverted and connected to SCLK to clock data out of the converter at half the CLKIN frequency as shown in Figure 5. To generate the L/R signal, ACLKA is divided by 64 with the counter U7 shown in Figure 9. Since U7 is an asynchronous counter that advances on falling edges of ACLKA, U8A insures that L/R meets the  $t_{clr}$ ,  $t_{aclr}$ , and  $t_{scklr}$  timing requirements specified in the converter's data sheet. The divide by 32 output of U7 is also used to generate the LCLK signal for use with an external parallel output interface.

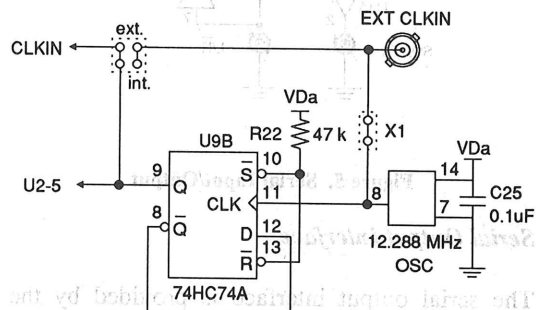


Figure 4. Clock Generator

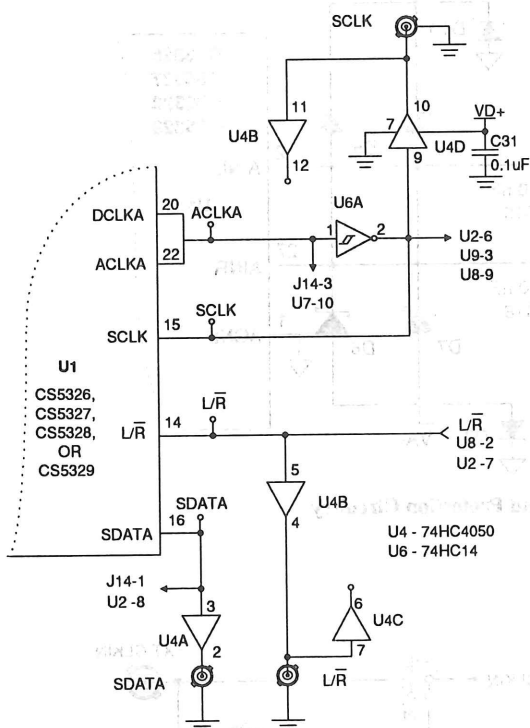


Figure 5. Serial Input/Output

## Serial Output Interface

The serial output interface is provided by the SDATA, SCLK, and  $\overline{L/R}$  BNC connectors on the evaluation board. These outputs are buffered, as shown in Figure 5, in order to isolate the converter from the digital signal processor. Serial data is clocked out of the converter by the SCLK signal at half of the master clock frequency. Note that in this configuration the serial output data is clocked out during the first part of each  $\overline{L/R}$  cycle. After the data for the selected channel has been clocked out, zeros are clocked out during the remaining SCLK cycles before  $\overline{L/R}$  changes state.

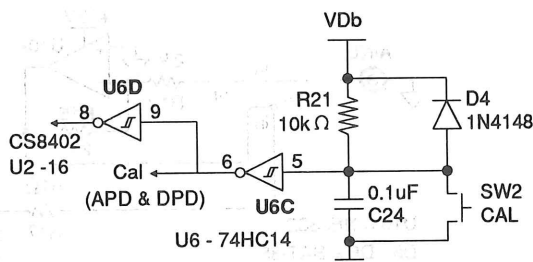


Figure 6. Offset Calibration Circuit

## Reset/Offset Calibration Circuit

The circuit of Figure 6 provides a pulse to the Analog to Digital Converter's DPD and APD pins initiating an offset calibration cycle. This pulse will also reset U2, the Digital Audio Line Driver. The circuit is activated on power-up and when SW2 is closed.

## Configuring the Board for External Timing

An external master clock may be supplied to the board directly via the EXTCLKIN input if the on board oscillator, X1 is removed. The board's SCLK and  $\overline{L/R}$  connectors may also be configured to accept input signals. This is accomplished with a simple modification. Holes in the SCLK and  $\overline{L/R}$  traces have been added to accomodate installing jumper wires and to facilitate breaking traces. Drilling through the surface pad of one of these holes with a small twist drill effectively breaks the trace and allows it to be driven by another source attached at an adjacent hole. This technique can be used to connect the converter to externally generated SCLK and  $\overline{L/R}$  signals during system development. Note that the SCLK trace must be broken at U6A pin 2 and U4D pin 9 before it may be configured as an input. Similarly, the  $\overline{L/R}$  trace must be broken at U4B pin 4 and U8 pin 2 before the BNC connector may be configured as an input.

# Digital Audio Standard Interface

Included on the evaluation board is a CS8402 Digital Audio Line Driver. This device can implement AES/EBU, S/PDIF and EIAJ CP-340 interface standards. Figure 7 shows the schematic for the CS8402. The C, U and V bits can be driven from external logic using the CBL output for block synchronization. SW1 provides 8 DIP switches to select various modes and bits for the CS8402. Table 3 lists the settings for the professional mode which is the default setting for the evaluation board from the factory. The third switch selects between professional and consumer modes; however, the CS8402 output to the transformer must be modified, as shown in Figure 8, to be compatible with the consumer interface.

Table 5 lists the switch settings for consumer mode. If the C input is used, the input bits are logically OR'ed with the appropriate DIP switch bits. In Tables 3 and 5, the 'C' bits listed in the comment section are taken from the Digital Audio Interface specifications. As an example, switch 6 in the professional mode (Table 3) controls  $\overline{C9}$  which is the inverse of channel status bit 9 (also listed as byte 1, bit 1 in the CS8402 data sheet). Channel status bit 9 is one of four bits indicating channel mode. Therefore, using DIP switch 6, only two of the available channel modes may be selected. The C input port may be used to select other channel modes. See the CS8401 & CS8402 data sheet for more information on the operation of the CS8402.

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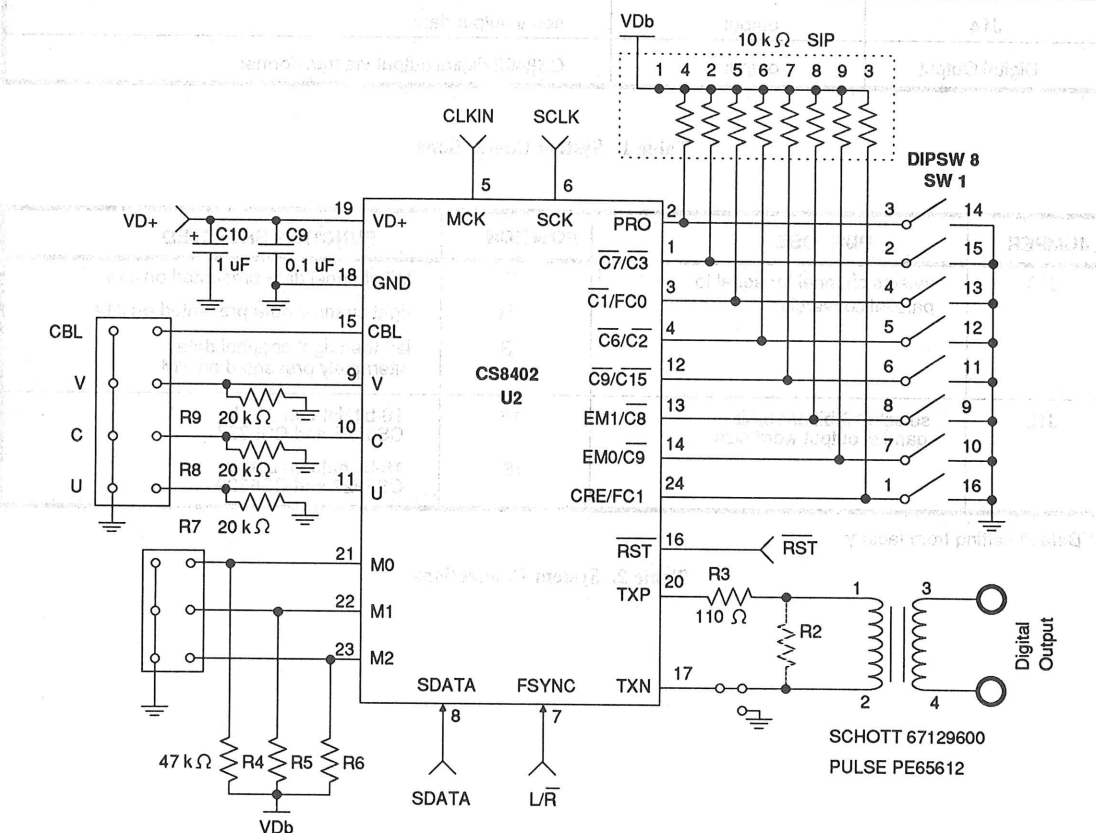


Figure 7. Digital Audio Line Connections



CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+15	input	+15 Volts from power supply
-15	input	-15 Volts from power supply
AGND	input	analog ground connection from power supply
+5	input	+5V for ADC VD1+ / VD2+ and discrete logic
DGND	input	digital ground connection from power supply
AINL	input	left channel analog input
AINR	input	right channel analog input
EXTCLKIN	input	external master clock input
L/R	output	left /right channel signal
SDATA	output	serial output data
SCLK	output	serial output clock
J14	output	serial output data
Digital Output	output	CS8402 digital output via transformer

**Table 1. System Connections**

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
J13	selects channel for serial to parallel conversion	*L	left channel data presented on J14
		R	right channel data presented on J14
		B	left then right channel data alternately presented on J14
J12	selects 16-bit or 18-bit parallel output word size	16	16-bit data on J14 for CS5326 and CS5327
		18	18-bit data on J14 for CS5327 and CS5329

\* Default setting from factory

**Table 2. System Connections**

Switch#	0=Closed, 1=Open	Comment
3	PRO=0	Professional Mode, C0=1 (default)
1	CRE	Local Sample Address Counter & Reliability Flags
default	0 1	Disabled Internally Generated (channel status bytes 14-17 and byte 22)
5, 2	C6, C7	C6, C7 - Sample Frequency
default	1 1 1 0 0 1 0 0	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
4	C1	C1 - Audio
default	1 0	0 - Normal Audio 1 - Non-Audio
6	C9	C8, C9, C10, C11 - Channel Mode (1 of 4 bits)
default	1 0	0000 - Not indicated - Default to 2-channel 0100 - Stereophonic
8, 7	EM1, EM0	C2, C3, C4 - Emphasis
default	1 1 1 0 0 1 0 0	000 - Not Indicated - default to none 100 - No emphasis 110 - 50/15 $\mu$ s 111 - CCITT J.17

Table 3. CS8402 Switch Definitions - Professional Mode

M2	M1	M0	Format
0	0	0	0 - FSYNC & SCK Output
0	0	1	1 - Left/Right, 16-24 Bits
0	1	0	2 - Word Sync, 16-24 Bits
0	1	1	3 - Reserved
1	0	0	4 - Left/Right, I <sup>2</sup> S Compatible
1	0	1	5 - LSB Justified, 16 Bits
1	1	0	6 - LSB Justified, 18 Bits
1	1	1	7 - MSB Last, 16-24 Bits

Table 4. CS8402A Audio Port Modes

\* Default setting for CDB5326/7/8/9.

Switch#	0=Closed, 1=Open	Comment
3	$\overline{\text{PRO}}=1$	Consumer Mode, C0=0 (Note 1)
1, 4	FC1, FC0	C24,C25,C26,C27 - Sample Frequency (encoded 2 of 4 bits)
	0 0	0000 - 44.1 kHz
	0 1	0100 - 48 kHz
	1 0	1100 - 32 kHz
	1 1	0000 - 44.1 kHz, CD Mode
2	$\overline{\text{C3}}$	C3,C4,C5 - Emphasis (1 of 3 bits)
	1	000 - None
	0	100 - 50/15 $\mu$ s
5	$\overline{\text{C2}}$	C2 - Copy/Copyright
	1	0 - Copy Inhibited/Copyright Asserted
	0	1 - Copy Permitted/Copyright Not Asserted
6	$\overline{\text{C15}}$	C15 - Generation Status
	1	0 - Definition is based on category code.
	0	1 - See CS8402 Data Sheet, Appendix A
8, 7	$\overline{\text{C8}}, \overline{\text{C9}}$	C8-C14 - Category Code (2 of 7 bits)
	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - Compact Disk - CD
	0 0	1100000 - Digital Audio Tape - DAT

Note: 1. The evaluation board is shipped from the factory in the Professional mode. Changing switch 3 to open places the CS8402 in Consumer mode; however, the hardware is not set up for consumer mode. To modify the hardware for Consumer mode, change R3 to 374 $\Omega$ , add R2 at 90.9 $\Omega$ , cut the trace connecting TXN to the transformer, and connect the transformer side to the ground hole provided (see Figure 8). For a full explanation of the consumer hardware interface, see the CS8402 data sheet, Appendix B.

Table 5. CS8402 Switch Definitions - Consumer Mode

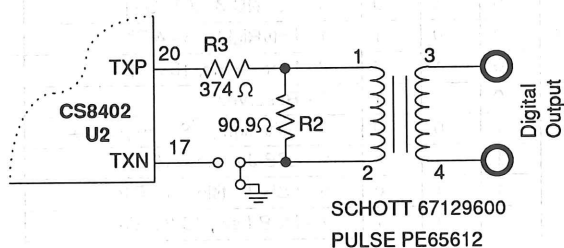


Figure 8. Hardware Connections for Consumer Mode

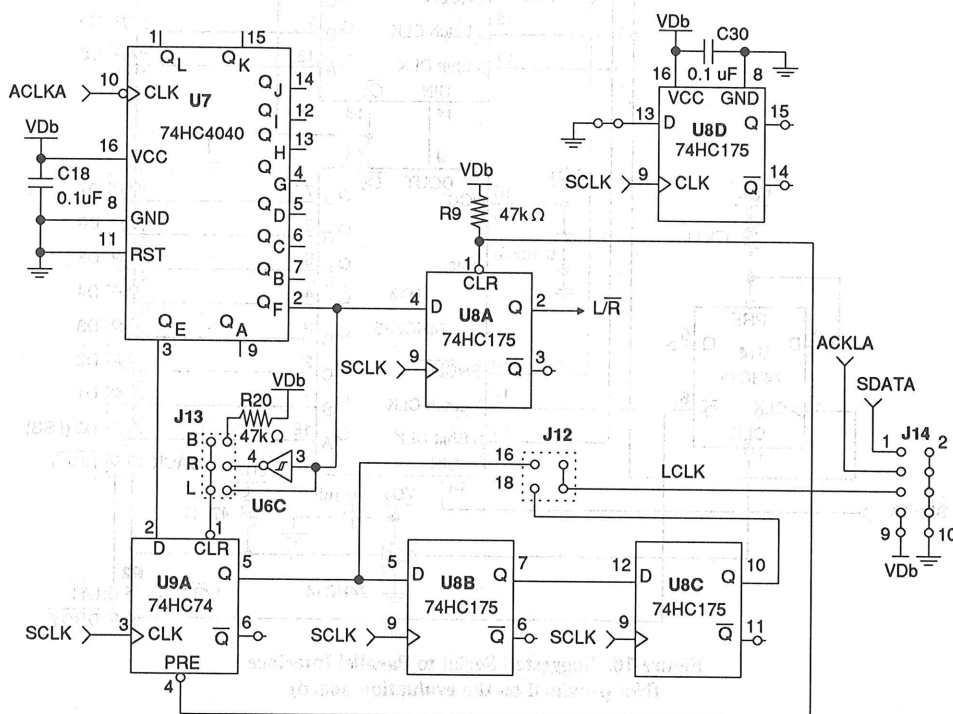
### External Parallel Output Interface

Figure 10 is a suggested circuit which assembles 16-bit or 18-bit words from the serial data output on J14. J12, Figure 9, on the evaluation board selects the word size which should be set to "16" for use with the CS5326 and CS5327 and "18" for use with the CS5328 and CS5329. Each bit of serial data is clocked out of the converter on the rising edge of SCLK and shifted into the 24-bit shift register formed by U11, U12 and U13 on SCLK's falling edge. After all data bits for the selected channel have been shifted into U11, U12 and U13 the data is latched onto P3 by the rising edge of LCLK.

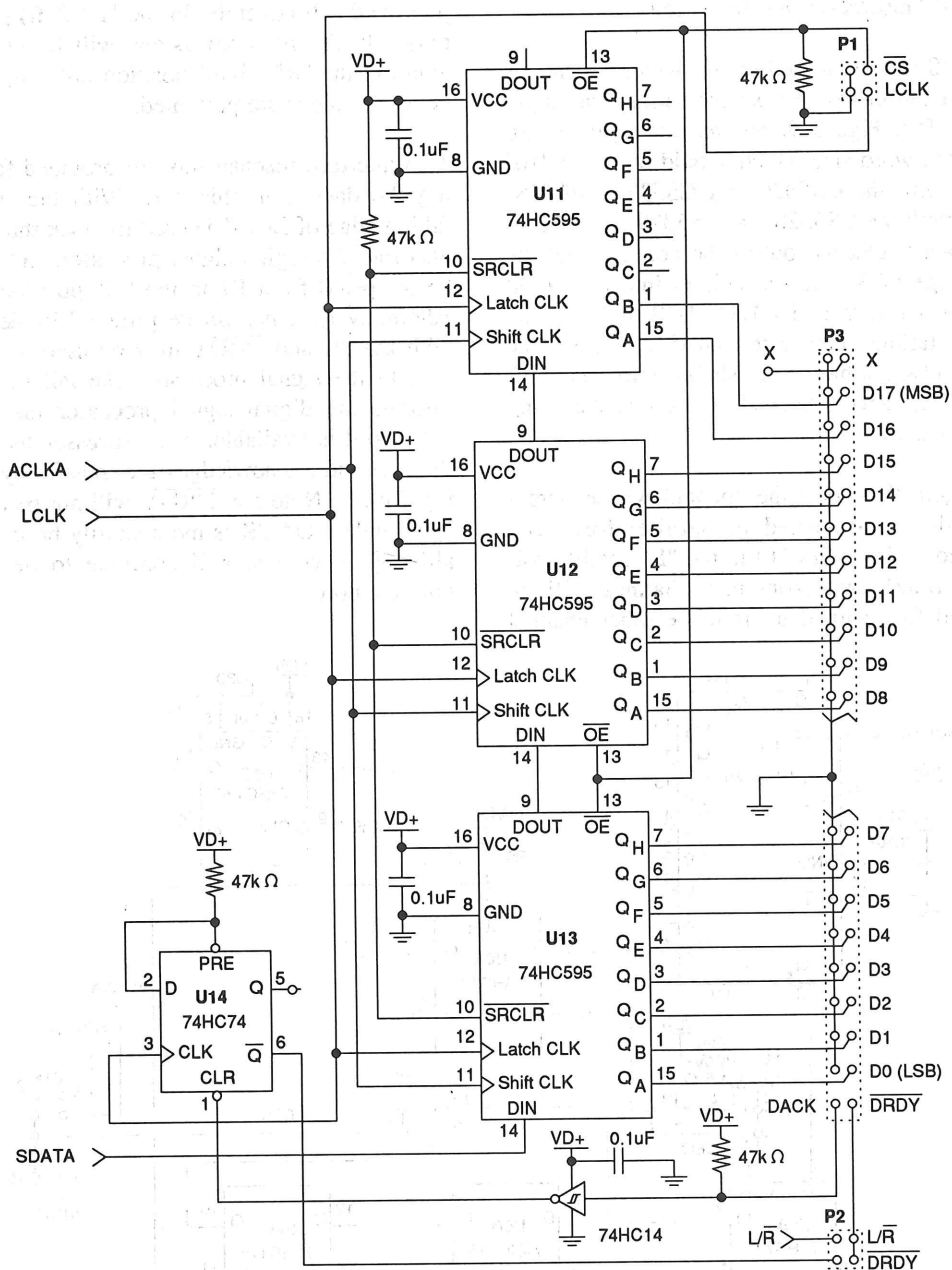
J13, Figure 9, selects the channel whose output data will be converted to parallel form and presented on P3. With J13 in the "B" (both) position, parallel data from one channel will be presented first with data from the other channel

presented subsequently. In the "L" (left) position, only left channel conversions will be presented, while in the "R" (right) position only right channel conversions are presented.

Two interface mechanisms are provided for reading the data from this port. With the first, the falling edge of LCLK is used to clock the parallel data into the digital signal processor. LCLK may be jumpered from P1 to the "X" position of P3. Alternatively, a handshake protocol implemented with DACK and  $\overline{\text{DRDY}}$  may be used to transfer data to the signal processor. The fall of  $\overline{\text{DRDY}}$  informs the digital signal processor that a new data word is available. The processor then reads the port and acknowledges the transfer by asserting DACK. Note that  $\overline{\text{DRDY}}$  will not be asserted again unless DACK is momentarily brought high although new data will continue to be latched onto the port.



### Figure 9. Timing Generator



**Figure 10. Suggested Serial to Parallel Interface**  
(Not provided on the evaluation board)



**Figure 11. CDB5326/7/8/9 Rev. E. Layout**



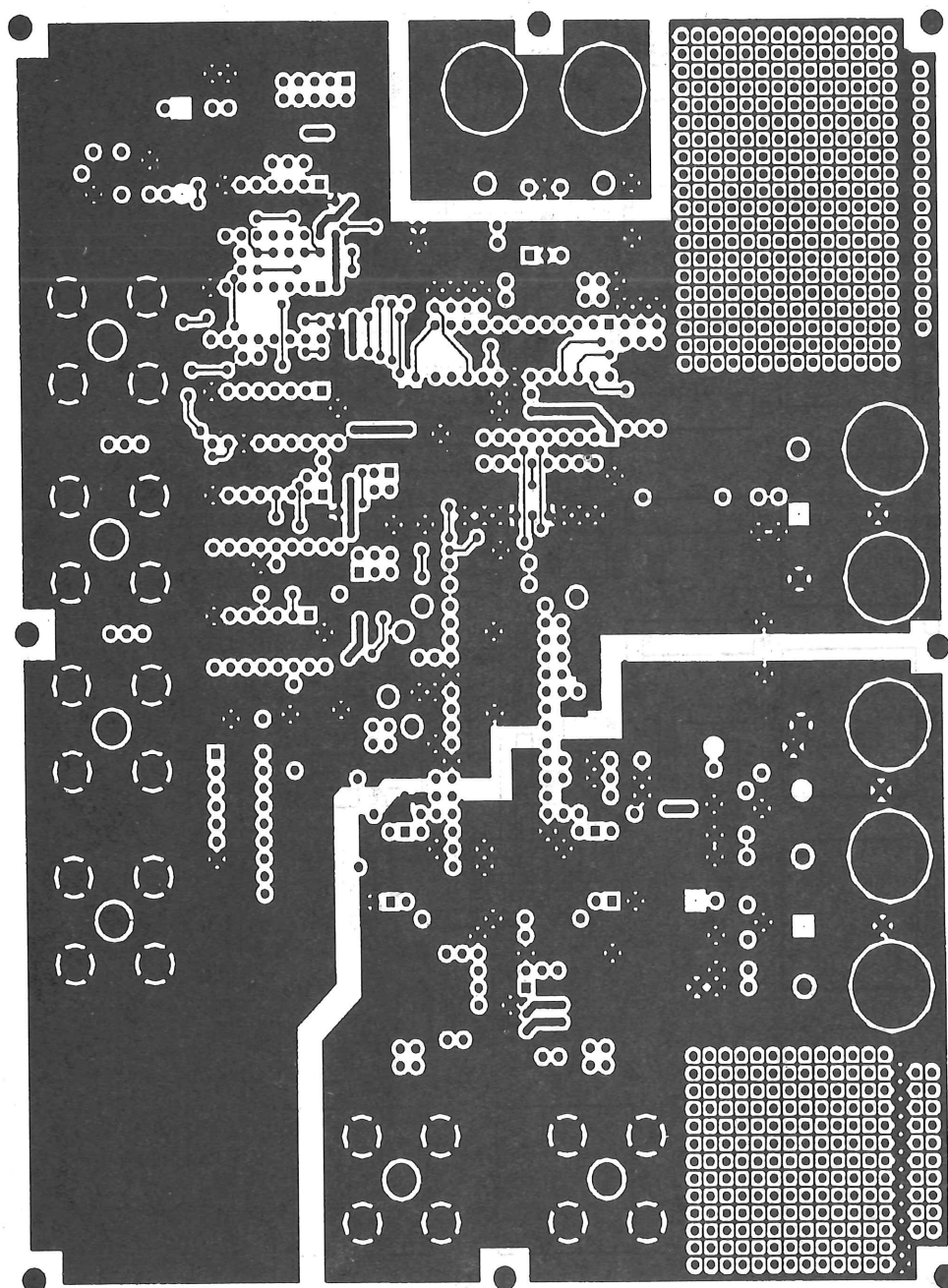


Figure 12. CDB5326/7/8/9 Rev. E. Component Side

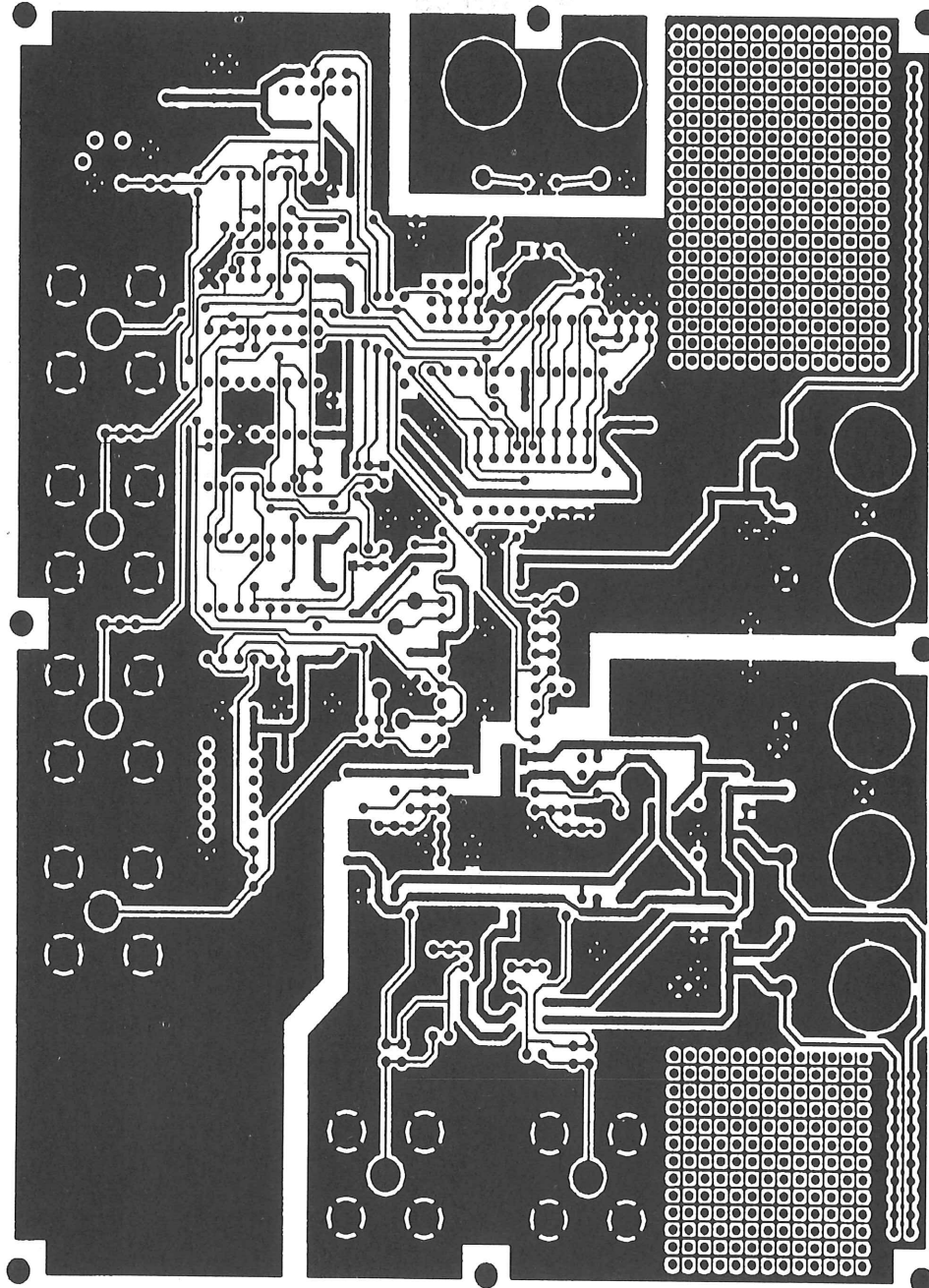


Figure 13. CDB5326/7/8/9 Rev. E. Solder Side

**• Notes •**

## 16-Bit, Stereo A/D Converters for Digital Audio

### Features

- Complete CMOS Stereo A/D System  
Delta-Sigma A/D Converters  
Digital Anti-Alias Filtering  
S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates  
including 32kHz, 44.1 kHz & 48kHz
- Low Noise and Distortion  
>90 dB S/(N+D)
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering  
0.01dB Passband Ripple  
80dB Stopband Rejection
- Low Power Dissipation: 400 mW  
Power-Down Mode for Portable  
Applications
- Evaluation Board Available

### General Description

The CS5336, CS5338 & CS5339 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The ADCs use delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

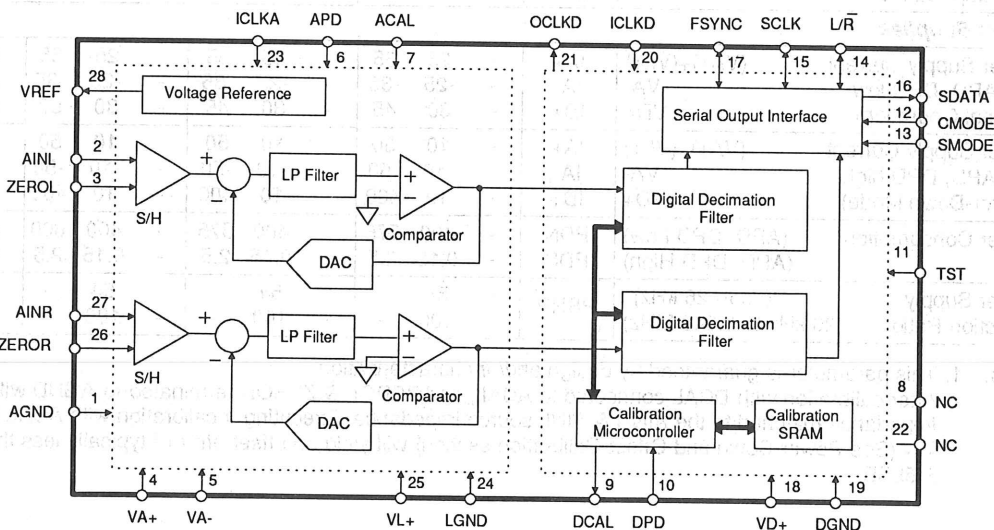
The CS5336 & CS5338 have an SCLK which clocks out data on rising edges. The CS5339 has an SCLK which clocks out data on falling edges.

The CS5336 has a filter passband of dc to 22kHz. The CS5338 & CS5339 have a filter passband of dc to 24 kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package. Extended temperature range versions of the CS5336 are also available.

**ORDERING INFORMATION:** See Page 2-179

2



**ANALOG CHARACTERISTICS** (Logic 0 = GND; Logic 1 = VD+; K grade: T<sub>A</sub> = 25°C; B and T grades: T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>; VA+, VL+, VD+ = 5V; VA- = -5V; Full-Scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 50Ω with 10 nF to AGND; Measurement Bandwidth is 10 Hz to 20 kHz; unless otherwise specified.)

Parameter	Symbol	CS5336,8,9-K			CS5336-B			CS5336-T			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range	T <sub>A</sub>	0	to	70	-40	to	+85	-55	to	+125	°C
Resolution		16	-	-	16	-	-	16	-	-	Bits
<b>Dynamic Performance</b>											
Dynamic Range		92.7	95.7	-	90	93.5	-	84	92	-	dB
Signal-to-(Noise + Distortion); THD+N	S/(N+D)	90.7	92.7	-	85	89	-	82	86	-	dB
Signal to Peak Noise		-	96	-	-	95	-	-	94	-	dB
Total Harmonic Distortion	THD	.0025	.001	-	.005	.001	-	.013	.005	-	%
Interchannel Phase Deviation		-	.0001	-	-	.0001	-	-	.0001	-	°
Interchannel Isolation (dc to 20 kHz)		100	106	-	90	106	-	83	96	-	dB
<b>dc Accuracy</b>											
Interchannel Gain Mismatch		-	0.01	0.05	-	.01	.05	-	.01	0.1	dB
Gain Error (includes V <sub>ref</sub> tolerance)		-	±1	±5	-	±2	±5	-	±3	±6	%
Gain Drift (includes V <sub>ref</sub> drift, Note 1)		-	25	-	-	70	-	-	70	-	ppm/°C
Bipolar Offset Error (Note 2)		-	±5	±15	-	±10	±30	-	±16	±65	LSB
Offset Drift (Note1)		-	15	-	-	20	-	-	20	-	ppm/°C
<b>Analog Input</b>											
Input Voltage Range (±Full Scale)	V <sub>IN</sub>	±3.5	±3.68	-	±3.5	±3.68	-	±3.5	±3.68	-	V
Input Impedance	Z <sub>IN</sub>	-	65	-	-	65	-	-	65	-	kΩ
<b>Power Supplies</b>											
Power Supply Current (VA+)+(VL+) with APD, DPD low (Normal Operation)	IA+	-	25	35	-	25	35	-	25	35	mA
	IA-	-	-25	-35	-	-25	-35	-	-25	-35	mA
	ID+	-	30	45	-	30	45	-	30	50	mA
Power Supply Current (VA+)+(VL+) with APD, DPD high (Power-Down Mode)	IA+	-	10	50	-	10	50	-	10	50	μA
	IA-	-	-10	-50	-	-10	-50	-	-10	-50	μA
	ID+	-	10	400	-	10	400	-	10	400	μA
Power Consumption (APD, DPD Low) (APD, DPD High)	P <sub>DN</sub>	-	400	575	-	400	575	-	400	600	mW
	P <sub>DS</sub>	-	0.15	2.5	-	0.15	2.5	-	0.15	2.5	mW
Power Supply Rejection Ratio (dc to 26 kHz) (26 kHz to 3.046 MHz)	PSRR	-	54	-	-	54	-	-	54	-	dB
		-	100	-	-	100	-	-	100	-	dB

- Notes: 1. This parameter is guaranteed by design and/or characterization.  
2. After calibration with DCAL connected to ACAL, and ZEROL & ZEROR terminated to AGND with an impedance matched to the AINR & AINL source impedance. Executing a calibration with ACAL tied low (See Power Down and Offset Calibration section) will yield an offset error of typically less than ± 5LSB.

Specifications are subject to change without notice.

## DIGITAL FILTER CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ ;  $V_{A+}$ ,  $V_{L+}$ ,  $V_{D+} = 5\text{V} \pm 5\%$ ;  $V_{A-} = -5\text{V} \pm 5\%$ ; Output word rate of 48 kHz)

Parameter	Symbol	Min	Typ	Max	Units
Passband (-3 dB) CS5336		0	to	22	kHz
(-3 dB) CS5338, CS5339		0	to	24	kHz
(-0.01 dB) CS5336		0	to	20	kHz
(-0.01 dB) CS5338, CS5339		0	to	22	kHz
Passband Ripple		-	-	$\pm 0.01$	dB
Stopband CS5336		26	to	3046	kHz
CS5338, CS5339		28	to	3044	kHz
Stopband Attenuation (Note 3)		80	-	-	dB
Group Delay (OWR = Output Word Rate)	$t_{gd}$	-	18/OWR	-	s
Group Delay Variation vs. Frequency	$\Delta t_{gd}$	-	-	0.0	us

Notes: 3. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for  $n \times 3.072\text{MHz} \pm 22\text{kHz}$  for the CS5338 & CS5339, or  $n \times 3.072\text{MHz} \pm 20.0\text{kHz}$  for the CS5336, where  $n = 0, 1, 2, 3, \dots$ ).

## DIGITAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ ;  $V_{A+}$ ,  $V_{L+}$ ,  $V_{D+} = 5\text{V} \pm 5\%$ ;  $V_{A-} = -5\text{V} \pm 5\%$ )

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	$V_{IH}$	$70\%V_{D+}$	-	-	V
Low-Level Input Voltage	$V_{IL}$	-	-	$30\%V_{D+}$	V
High-Level Output Voltage at $I_o = -20\mu\text{A}$	$V_{OH}$	4.4	-	-	V
Low-Level Output Voltage at $I_o = 20\mu\text{A}$	$V_{OL}$	-	-	0.1	V
Input Leakage Current	$I_{in}$	-	1.0	-	$\mu\text{A}$

## ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to GND)

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive Analog	$V_{A+}$	-0.3	+6.0	V
Negative Analog	$V_{A-}$	+0.3	-6.0	V
Positive Logic	$V_{L+}$	-0.3	$(V_{A+}) + 0.3$	V
Positive Digital	$V_{D+}$	-0.3	+6.0	V
Input Current, Any Pin Except Supplies	$I_{in}$	-	$\pm 10$	mA
Analog Input Voltage (AIN and ZERO pins)	$V_{INA}$	$(V_{A-}) - 0.3$	$(V_{A+}) + 0.3$	V
Digital Input Voltage	$V_{IND}$	-0.3	$(V_{D+}) + 0.3$	V
Ambient Temperature (power applied)	$T_A$	-55	+125	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65	+150	$^\circ\text{C}$

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.



## SWITCHING CHARACTERISTICS

(T<sub>A</sub> = 25 °C; V<sub>A+</sub>, V<sub>L+</sub>, V<sub>D+</sub> = 5V ± 5%; V<sub>A-</sub> = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = V<sub>D+</sub>; C<sub>L</sub> = 20 pF)

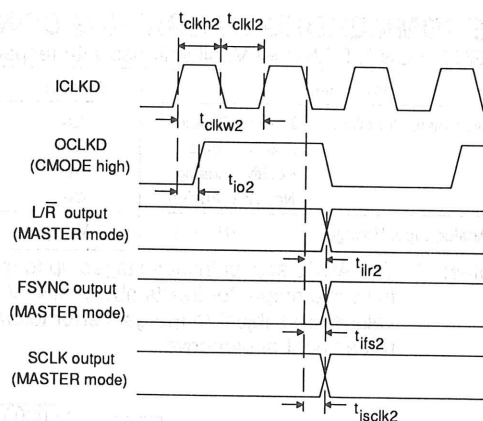
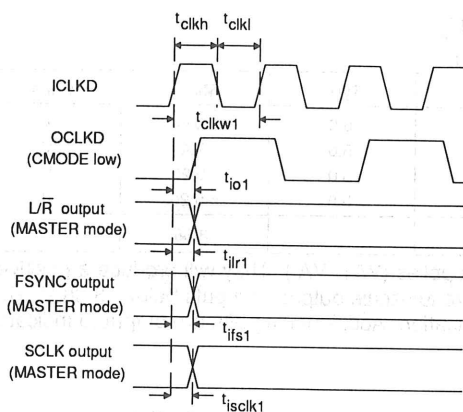
Parameter	Symbol	Min	Typ	Max	Unit
ICLKD Period (CMODE low) (Note 6)	t <sub>clkw1</sub>	78	-	3906	ns
ICLKD Low (CMODE low)	t <sub>clk1</sub>	31	-	-	ns
ICLKD High (CMODE low)	t <sub>clkh1</sub>	31	-	-	ns
ICLKD rising to OCLKD rising (CMODE low)	t <sub>io1</sub>	5	-	40	ns
ICLKD Period (CMODE high)	t <sub>clkw2</sub>	52	-	2604	ns
ICLKD Low (CMODE high)	t <sub>clk2</sub>	20	-	-	ns
ICLKD High (CMODE high)	t <sub>clkh2</sub>	20	-	-	ns
ICLKD rising or falling to OCLKD rising (CMODE high, Note 4)	t <sub>io2</sub>	5	-	45	ns
ICLKD rising to L/R edge (CMODE low, MASTER mode)	t <sub>ilr1</sub>	5	-	50	ns
ICLKD rising to FSYNC edge (CMODE low, MASTER mode)	t <sub>ifs1</sub>	5	-	50	ns
ICLKD rising to SCLK edge (CMODE low, MASTER mode)	t <sub>isclk1</sub>	5	-	50	ns
ICLKD falling to L/R edge (CMODE high, MASTER mode)	t <sub>ilr2</sub>	5	-	50	ns
ICLKD falling to FSYNC edge (CMODE high, MASTER mode)	t <sub>ifs2</sub>	5	-	50	ns
ICLKD falling to SCLK edge (CMODE high, MASTER mode)	t <sub>isclk2</sub>	5	-	50	ns
SCLK rising to SDATA valid (MASTER mode, Note 5)	t <sub>sdo</sub>	0	-	50	ns
SCLK duty cycle (MASTER mode)		40	50	60	%
SCLK rising to L/R (MASTER mode, Note 5)	t <sub>mslr</sub>	-20	-	20	ns
SCLK rising to FSYNC (MASTER mode, Note 5)	t <sub>msfs</sub>	-20	-	20	ns
SCLK Period (SLAVE mode)	t <sub>sclkw</sub>	155	-	-	ns
SCLK Pulse Width Low (SLAVE mode)	t <sub>sclkl</sub>	60	-	-	ns
SCLK Pulse Width High (SLAVE mode)	t <sub>sclkh</sub>	60	-	-	ns
SCLK rising to SDATA valid (SLAVE mode, Note 5)	t <sub>dss</sub>	-	-	50	ns
L/R edge to MSB valid (SLAVE mode)	t <sub>lrdss</sub>	-	-	50	ns
Falling SCLK to L/R edge delay (SLAVE mode, Note 5)	t <sub>slr1</sub>	30	-	-	ns
L/R edge to falling SCLK setup time (SLAVE mode, Note 5)	t <sub>slr2</sub>	30	-	-	ns
Falling SCLK to rising FSYNC delay (SLAVE mode, Note 5)	t <sub>sfs1</sub>	30	-	-	ns
Rising FSYNC to falling SCLK setup time (SLAVE mode, Note 5)	t <sub>sfs2</sub>	30	-	-	ns
DPD pulse width	t <sub>pdw</sub>	2 x t <sub>clkw</sub>	-	-	ns
DPD rising to DCAL rising	t <sub>pcr</sub>	-	-	50	ns
DPD falling to DCAL falling (OWR = Output Word Rate)	t <sub>pcf</sub>	-	4096	-	1/OWR

Notes: 4. ICLKD rising or falling depends on DPD to L/R timing (see Figure 2).

5. SCLK is shown for CS5336, CS5338. SCLK is inverted for CS5339.

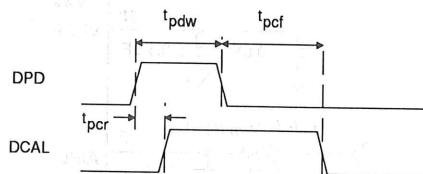
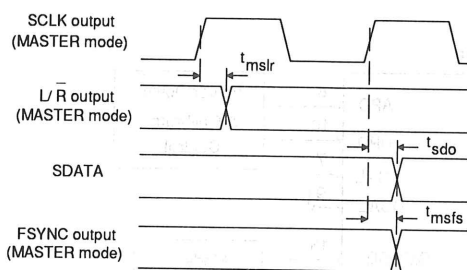
6. Specifies minimum output word rate (OWR) of 1 kHz.





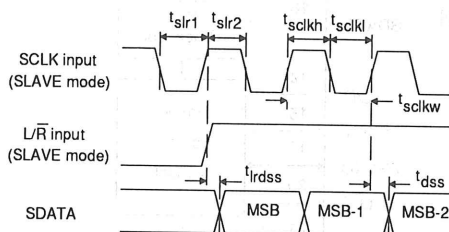
**ICLKD to Outputs Propagation Delays (CMODE low)**

**ICLKD to Outputs Propagation Delays (CMODE high)**

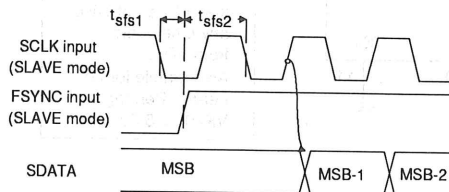


**SCLK to SDATA, L/R & FSYNC - MASTER Mode**

**Power Down & Calibration Timing**



**SCLK to L/R & SDATA - SLAVE mode, FSYNC high**



**FSYNC to SCLK - SLAVE Mode, FSYNC Controlled.**

### RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	VA+
	Positive Logic	VL+	4.75	5.0	VA+
	Positive Analog	VA+	4.75	5.0	5.25
	Negative Analog	VA-	-4.75	-5.0	-5.25
Analog Input Voltage	(Note 7)	V <sub>AIN</sub>	-3.68	-	3.68
					V

Notes: 7. The ADCs accept input voltages up to the analog supplies (VA+, VA-). They will produce a positive full-scale output for inputs above 3.68 V and negative full-scale output for inputs below -3.68 V. These values are subject to the gain error tolerance specification. Additional tag bits are output to indicate the amount of overdrive.

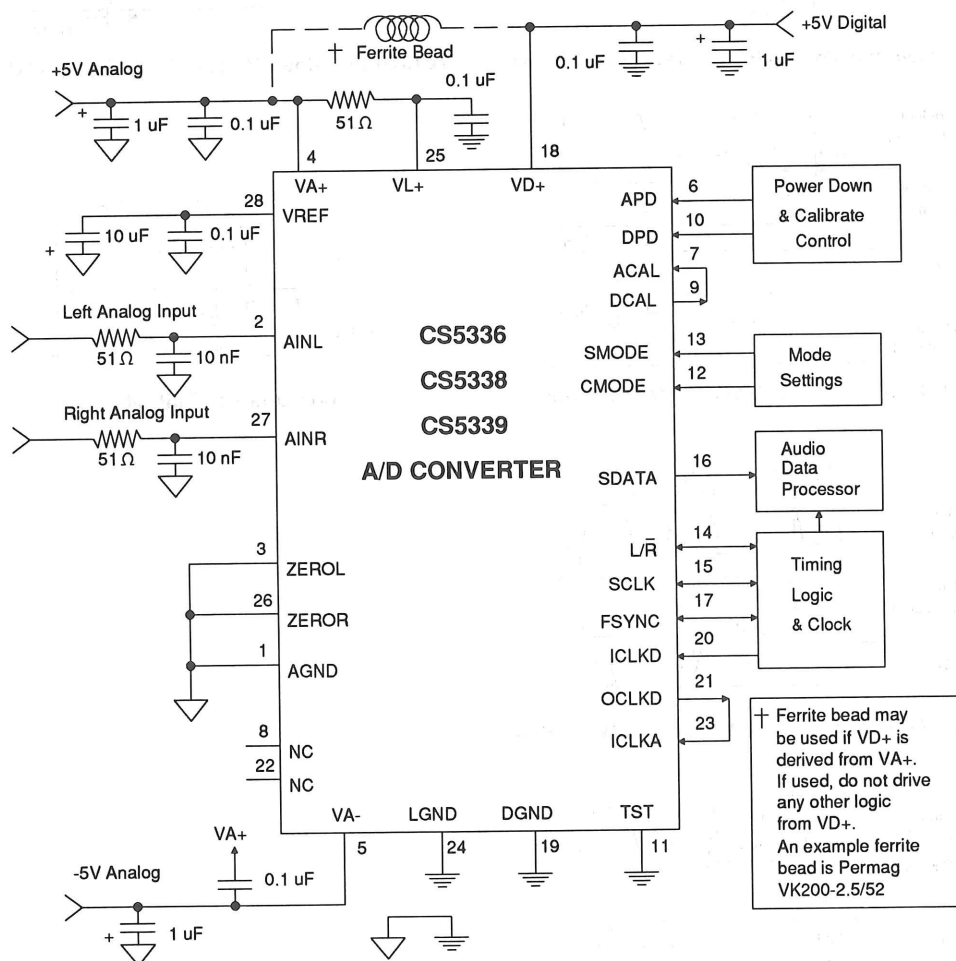


Figure 1. Typical Connection Diagram

## GENERAL DESCRIPTION

The CS5336, CS5338, and CS5339 are 16-bit, 2-channel A/D converters designed specifically for stereo digital audio applications. The devices use two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 16-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for an input signal range of  $\pm 3.68$  volts. Any zero offset is internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16-bit numbers. Typical power consumption of only 400 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside these ADCs, see the references at the end of this data sheet.

L/R (kHz)	CMODE	ICLKD (MHz)	OCLKD/ ICLKA (MHz)	SCLK (MHz)
32	low	8.192	4.096	2.048
32	high	12.288	4.096	2.048
44.1	low	11.2896	5.6448	2.8224
44.1	high	16.9344	5.6448	2.8224
48	low	12.288	6.144	3.072
48	high	18.432	6.144	3.072

Table 1. Common Clock Frequencies

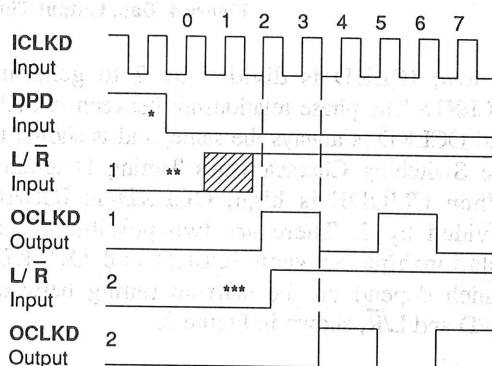
## SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

### Master Clock Input

The master input clock (ICLKD) into the ADC runs the digital filter, and is used to generate the modulator sampling clock. ICLKD frequency is determined by the desired Output Word Rate (OWR) and the setting of the CMODE pin. CMODE high will set the required ICLKD frequency to 384 X OWR, while CMODE low will set the required ICLKD frequency to 256 X OWR. Table 1 shows some common clock frequencies. The digital output clock (OCLKD) is always equal to 128 X OWR, which is always 2 X the input sample rate. OCLKD should be connected to ICLKA, which controls the input sample rate.

The phase alignment between ICLKD and OCLKD is determined as follows: when CMODE



\* DPD low is recognized on the next ICLKD rising edge (#0)

\*\* L/R rising before ICLKD rising #2 causes OCLKD -1

\*\*\* L/R rising after ICLKD rising #2 causes OCLKD -2

Figure 2. ICLKD to OCLKD Timing with CMODE high (384 X OWR)

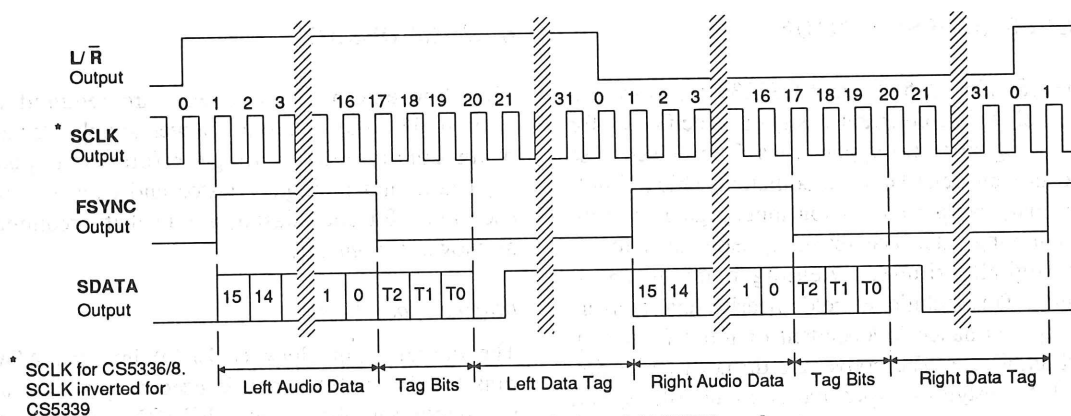


Figure 3. Data Output Timing - MASTER mode

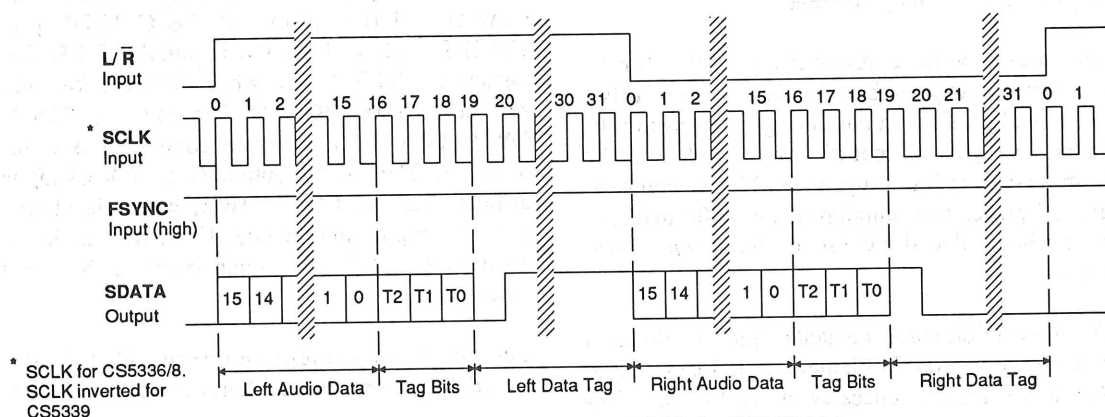


Figure 4. Data Output Timing - SLAVE Mode, FSYNC high

is low, ICLKD is divided by 2 to generate OCLKD. The phase relationship between ICLKD and OCLKD is always the same, and is shown in the Switching Characteristics Timing Diagrams. When CMODE is high, OCLKD is ICLKD divided by 3. There are two possible phase relationships between ICLKD and OCLKD, which depend on the start-up timing between DPD and  $L/\bar{R}$ , shown in Figure 2.

### Serial Data Interface

The serial data output interface has 3 possible modes of operation: MASTER mode, SLAVE mode with FSYNC high, and SLAVE mode with FSYNC controlled. In MASTER mode, the A/D

converter is driven from a master clock (ICLKD) and outputs all other clocks, derived from ICLKD (see Figure 3). Notice the one SCLK cycle delay between  $L/\bar{R}$  edges and FSYNC rising edges. FSYNC brackets the 16 data bits for each channel.

In SLAVE mode,  $L/\bar{R}$  and SCLK are inputs.  $L/\bar{R}$  must be externally derived from ICLKD, and should be equal to the Output Word Rate. SCLK should be equal to the input sample rate, which is equal to OCLKD/2. Other SCLK frequencies are possible, but may degrade dynamic range because of interference effects. Data bits are clocked out via the SDATA pin using the SCLK and  $L/\bar{R}$  inputs. The rising edge of SCLK causes the ADC to

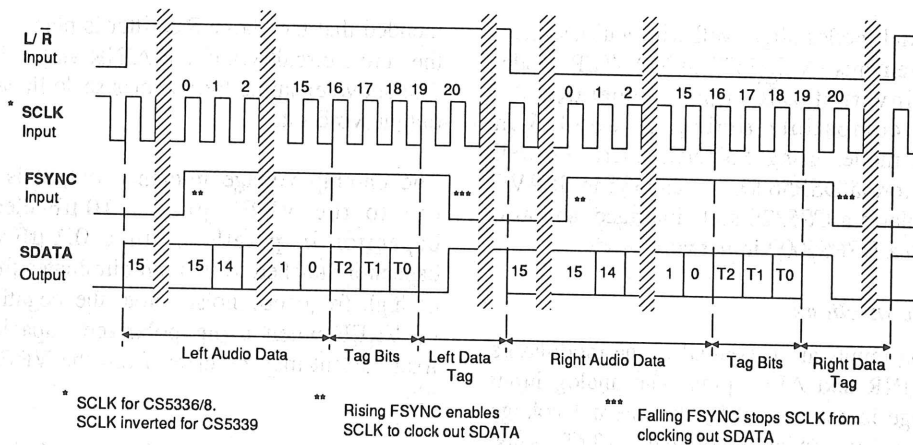


Figure 5. Data Output Timing - SLAVE Mode, FSYNC controlled

output each bit, except the MSB, which is clocked out by the  $L/\bar{R}$  edge. As shown in Figure 4, when FSYNC is high, serial data bits are clocked immediately following the  $L/\bar{R}$  edge.

In SLAVE mode with FSYNC controlled, as shown in Figure 5, when FSYNC is low, only the MSB is clocked out after the  $L/\bar{R}$  edge. With FSYNC low, SCLK is ignored. When it is desired to start clocking out data, bring FSYNC high which enables SCLK to start clocking out data. Bringing FSYNC low will stop the data being clocked out. This feature is particularly useful to

position in time the data bits onto a common serial bus.

The serial nature of the output data results in the left and right data words being read at different times. However, the words within an  $L/\bar{R}$  cycle represent simultaneously sampled analog inputs.

In all modes, additional bits are output after the data bits: 3 tag bits and a left/right indicator. The tag bits indicate a near-to-clipping input condition for the data word to which the tag bits are attached. Table 2 shows the relationship between input level and the tag bit values. The serial bit immediately following the tag bits is 0 for the left channel, and 1 for the right channel. The remaining bits before the next  $L/\bar{R}$  edge will be 1's for the left channel and 0's for the right channel. Normally, the tag bits are separated from the audio data by the digital signal processor. However, if the tag bits are interpreted as audio data, their position below the LSB would result as a very small dc offset.

Input Level	T2	T1	T0
1.375 x FS	1	1	1
1.250 x FS to 1.375 x FS	1	1	0
1.125 x FS to 1.250 x FS	1	0	1
1.000 x FS to 1.125 x FS	1	0	0
-1.006dB to 0.000dB	0	1	1
-3.060dB to -1.006dB	0	1	0
-6.000dB to -3.060dB	0	0	1
< -6.000dB	0	0	0

FS = Full Scale (0dB) Input

Table 2. Tag Bit Definition

In all modes, SCLK is shown for the CS5336 and CS5338, where data bits are clocked out on rising edges. SCLK is inverted for the CS5339.

Certain serial modes align well with various interface requirements. A CS5339 in MASTER mode, with an inverted L/R signal, generates I<sup>2</sup>S (Philips) compatible timing. A CS5336 in MASTER mode, using FSYNC, interfaces well with a Motorola DSP56000. A CS5336 in SLAVE mode emulates a CS5326 style interface, and also links up to a DSP56000 in network mode.

### Analog Connections

The analog inputs are presented to the modulators via the AINR and AINL pins. The analog input signal range is determined by the internal voltage reference value, which is typically -3.68 volts. The input signal range therefore is typically  $\pm 3.68$  volts.

The ADC samples the analog inputs at 3.072 MHz for a 12.288 MHz ICLKD (CMODE low). For the CS5336, the digital filter rejects all noise between 26 kHz and (3.072 MHz-26 kHz). For the CS5338 and CS5339, the digital filter rejects all noise between 28 kHz and (3.072 MHz-28 kHz). However, the filter will not reject frequencies right around 3.072 MHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 51  $\Omega$  resistor in series with the analog input, and a 10 nF NPO or COG capacitor to ground will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recom-

mended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

The on-chip voltage reference output is brought out to the VREF pin. A 10  $\mu$ F electrolytic capacitor in parallel with a 0.1  $\mu$ F ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Note the negative value of VREF when using polarized capacitors. No load current may be taken from the VREF output pin.

The analog input level used as zero during the offset calibration period (described later) is input on the ZEROL and ZEROR pins. Typically, these pins are directly attached to AGND. For the ultimate in offset nulling, networks can be attached to ZEROR and ZEROL whose impedances match the impedances present on AINL and AINR.

### Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 150  $\mu$ W. In addition, exiting the power-down state initiates an offset calibration procedure.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle. If not using the power down feature, APD should be tied to AGND. When using the power down feature, DPD and APD

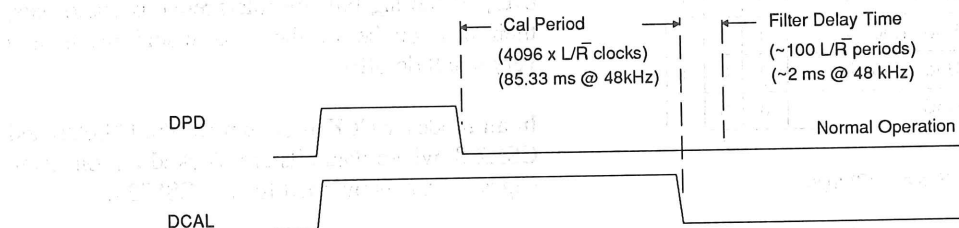


Figure 6. Initial Calibration Cycle Timing



may be tied together if the capacitor on VREF is not greater than 10  $\mu$ F, as stated in the "Power-Up Considerations" section.

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AINL and AINR) or the zero pins (ZEROL and ZEROR) depending on the state of the ACAL pin. With ACAL low, the analog input pin voltages are measured, and with ACAL high, the zero pin voltages are measured.

As shown in Figure 6, the DCAL output is high during calibration, which takes 4096  $L/\bar{R}$  clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage on ZEROR and ZEROL. These should be connected directly to ground or through a network matched to that present on the analog input pins. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to control a multiplexer which grounds the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present in the front end input circuitry.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any power-on click that might otherwise be experienced. A short delay of approximately 100 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals.

### *Power-up Considerations*

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/ $\mu$ F. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10  $\mu$ F. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

### *Grounding and Power Supply Decoupling*

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+, VA- and VL+ connected to a clean  $\pm 5$  V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy ( $< \pm 50$  mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground

planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. The VREF decoupling capacitors, particularly the 0.1  $\mu\text{F}$ , must be positioned to minimize the electrical path from VREF to Pin 1 AGND and to minimize the path between VREF and the capacitors. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

### ***Synchronization of Multiple CS5336/8/9***

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling. In the absence of this synchronization, the sampling difference could be one ICLKD period which is typically 81.4 nsec for a 48 kHz sample rate.

### ***SLAVE MODE***

Synchronous sampling in the slave mode is achieved by connecting all DPD and APD pins to a single control signal and supplying the same ICLKD and  $\overline{\text{L/R}}$  to all converters.

### ***MASTER MODE***

The internal counters of the CS5336/8/9 are reset during DPD/APD high and will start simultaneously by insuring that the release of DPD/APD for all converters is internally latched on the same rising edge of ICLKD. This can be achieved by connecting all DPD/APD pins to the same control signal and insuring that the DPD/APD falling edge occurs outside a  $\pm 30$  ns window either side of an ICLKD rising edge.

## **PERFORMANCE**

### ***FFT Tests***

For FFT based tests, a very pure sine wave is presented to the ADC, and an FFT analysis is performed on the output data. The resulting spectrum is a measure of the performance of the ADC.

Figure 7 shows the spectral purity of the CS5336 with a 1 kHz, -10 dB input. Notice the low noise floor, the absence of any harmonic distortion, and the Dynamic Range value of 95.41 dB.

Figure 8 shows the CS5336 high frequency performance. The input signal is a -10 dB, 9 kHz sine wave. Notice the small 2nd harmonic at 110 dB down.

Figure 9 shows the low-level performance of the CS5336. Notice the lack of any distortion components. Traditional R-2R ladder based ADC's can have problems with this test, since differential non-linearities around the zero point become very significant. Figure 10 shows the same very low input amplitude performance, but at 9kHz input frequency.

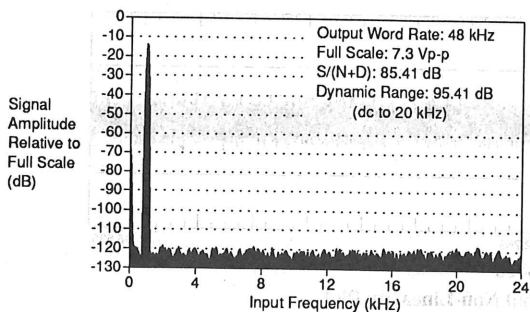


Figure 7. CS5336 FFT Plot with -10 dB, 1 kHz Input

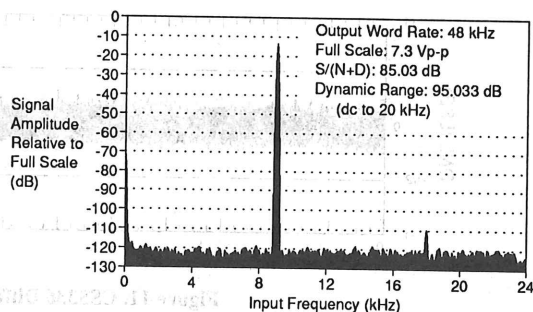


Figure 8. CS5336 FFT Plot with -10 dB, 9 kHz Input

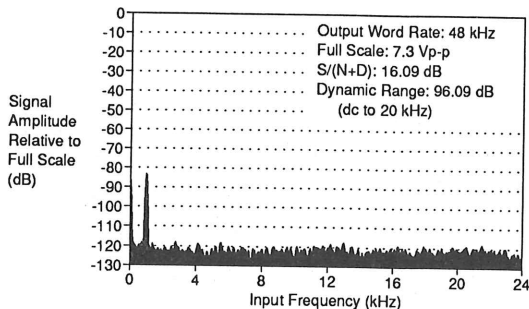


Figure 9. CS5336 FFT Plot with -80 dB, 1 kHz Input

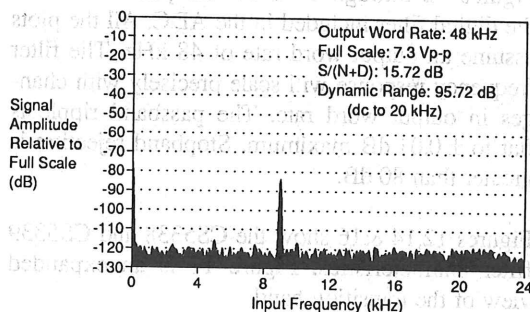
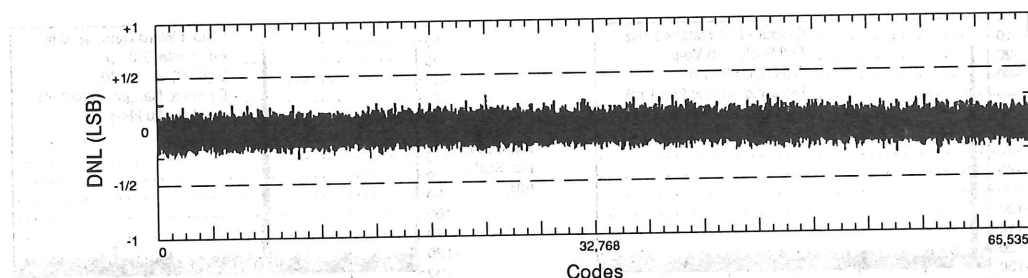


Figure 10. CS5336 FFT Plot with -80 dB, 9 kHz Input

### DNL Tests

A Differential Non-Linearity test is also shown. Here, the converter is presented with a linear ramp signal. The resulting output codes are counted to yield a number which is proportional to the codewidth. A plot of codewidth versus code graphically illustrates the uniformity of the codewidths. Figure 11 shows the excellent Differential Non-Linearity of the CS5336. This plot

displays the worst case positive and negative errors in each of 512 groups of 128 codes. Codewidths typically are within  $\pm 0.2$  LSB's of ideal. A delta-sigma modulator based ADC has no inherent mechanism for generating DNL errors. The residual small deviations shown in Figure 11 are a result of noise. Nevertheless, the performance shown is extremely good, and is superior to typical R-2R ladder based designs.



**Figure 11. CS5336 Differential Non-Linearity Plot**

### Digital Filter

Figures 12 through 17 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz. The filter frequency response will scale precisely with changes in output word rate. The passband ripple is flat to  $\pm 0.01$  dB maximum. Stopband rejection is greater than 80 dB.

Figures 12,14 &16 show the CS5338 and CS5339 filter characteristics. Figure 17 is an expanded view of the transition band.

Figures 13,15 & 17 show the CS5336 filter characteristics. Figure 17 is an expanded view of the transition band.

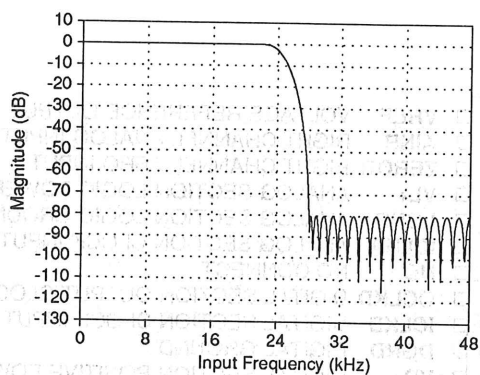


Figure 12. CS5338/9 Digital Filter Stopband Rejection

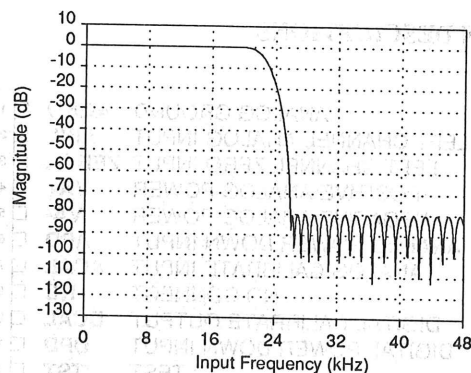


Figure 13. CS5336 Digital Filter Stopband Rejection

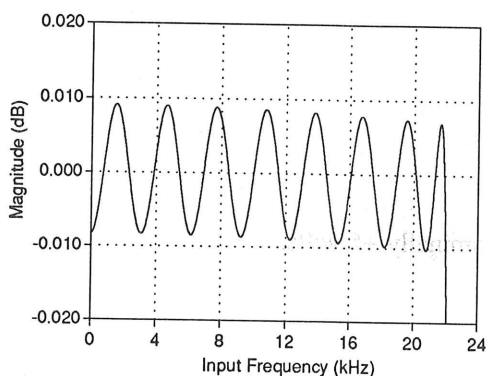


Figure 14. CS5338/9 Digital Filter Passband Ripple

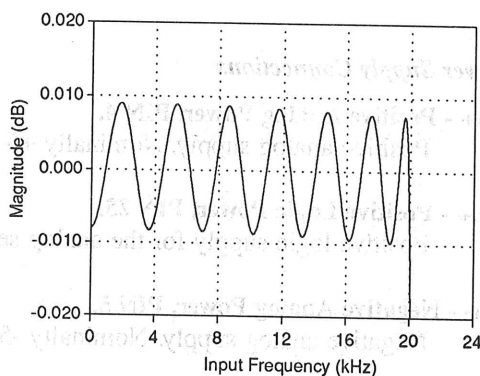


Figure 15. CS5336 Digital Filter Passband Ripple

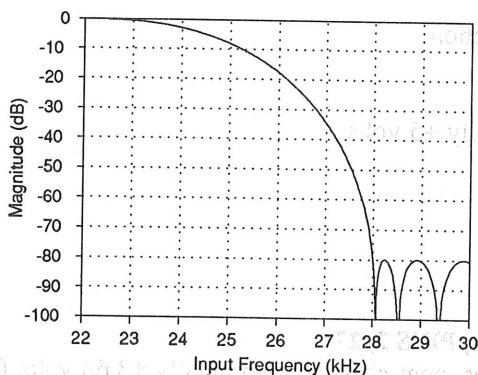


Figure 16. CS5338/9 Digital Filter Transition Band

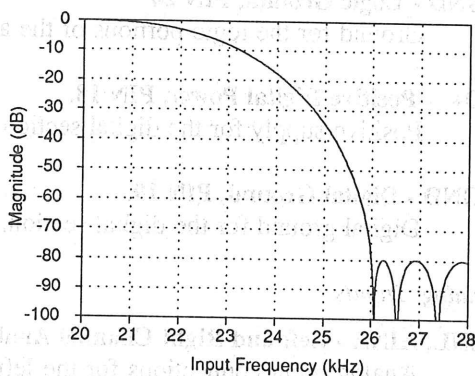


Figure 17. CS5336 Digital Filter Transition Band

## PIN DESCRIPTIONS

ANALOG GROUND	AGND	1	28	VREF	VOLTAGE REFERENCE OUTPUT
LEFT CHANNEL ANALOG INPUT	AINL	2	27	AINR	RIGHT CHANNEL ANALOG INPUT
LEFT CHANNEL ZERO INPUT	ZEROL	3	26	ZEROR	RIGHT CHANNEL ZERO INPUT
POSITIVE ANALOG POWER	VA+	4	25	VL+	ANALOG SECTION LOGIC POWER
NEGATIVE ANALOG POWER	VA-	5	24	LGND	ANALOG SECTION LOGIC GROUND
ANALOG POWER DOWN INPUT	APD	6	23	ICLKA	ANALOG SECTION CLOCK INPUT
ANALOG CALIBRATE INPUT	ACAL	7	22	NC	NO CONNECT
NO CONNECT	NC	8	21	OCLKD	DIGITAL SECTION OUTPUT CLOCK
DIGITAL CALIBRATE OUTPUT	DCAL	9	20	ICLKD	DIGITAL SECTION CLOCK INPUT
DIGITAL POWER DOWN INPUT	DPD	10	19	DGND	DIGITAL GROUND
TEST	TST	11	18	VD+	DIGITAL SECTION POSITIVE POWER
SELECT CLOCK MODE	CMODE	12	17	FSYNC	FRAME SYNC SIGNAL
SELECT SERIAL I/O MODE	SMODE	13	16	SDATA	SERIAL DATA OUTPUT
LEFT/RIGHT SELECT	L/R	14	15	SCLK	SERIAL DATA CLOCK

### Power Supply Connections

#### VA+ - Positive Analog Power, PIN 4.

Positive analog supply. Nominally +5 volts.

#### VL+ - Positive Logic Power, PIN 25.

Positive logic supply for the analog section. Nominally +5 volts.

#### VA- - Negative Analog Power, PIN 5.

Negative analog supply. Nominally -5 volts.

#### AGND - Analog Ground, PIN 1.

Analog ground reference.

#### LGND - Logic Ground, PIN 24

Ground for the logic portions of the analog section.

#### VD+ - Positive Digital Power, PIN 18.

Positive supply for the digital section. Nominally +5 volts.

#### DGND - Digital Ground, PIN 19.

Digital ground for the digital section.

### Analog Inputs

#### AINL, AINR - Left and Right Channel Analog Inputs, PINS 2, 27

Analog input connections for the left and right input channels. Nominally  $\pm 3.68$  volts full scale.

**ZEROL, ZEROR - Zero Level Inputs for Left and Right Channels, PINS 3, 26.**

Analog zero level inputs for the left and right channels. The levels present on these pins can be used as zero during the offset calibration cycle. Normally connected to AGND, optionally through networks matched to the analog input networks.

**Analog Outputs****VREF - Voltage Reference Output, PIN 28.**

Nominally -3.68 volts. Normally connected to a 0.1 $\mu$ F ceramic capacitor in parallel with a 10 $\mu$ F or larger electrolytic capacitor. Note the negative output polarity.

**Digital Inputs****ICLKA - Analog Section Input Clock, PIN 23.**

This clock is internally divided by 2 to set the modulators' sample rate. Sampling rates, output rates, and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is 128 X the output word rate. For example, 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD.

**ICLKD - Digital Section Input Clock, PIN 20.**

This is the clock which runs the digital filter. ICLKD frequency is determined by the required output word rate and by the CMODE pin. If CMODE is low, ICLKD frequency should be 256 X the desired output word rate. If CMODE is high, ICLKD should be 384 X the desired output word rate. For example, with CMODE low, ICLKD should be 12.288 MHz for an output word rate of 48 kHz. This clock also generates OCLKD, which is always 128 X the output word rate.

**APD - Analog Power Down, PIN 6.**

Analog section power-down command. When high, the analog circuitry is in power-down mode. APD is normally connected to DPD when using the power down feature. If power down is not used, then connect APD to AGND.

**DPD - Digital Power Down, PIN 10**

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 L/R periods (85.33 ms with a 12.288 MHz ICLKD). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD when using the power down feature. A calibration cycle should always be initiated after applying power to the supply pins.

**ACAL - Analog Calibrate, PIN 7.**

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to ZEROL and ZEROR inputs respectively. May be connected to DCAL.



**CMODE - Clock Mode Select, PIN 12.**

CMODE should be tied low to select an ICLKD frequency of 256 X the output word rate.  
CMODE should be tied high to select an ICLKD frequency of 384 X the output word rate.

**SMODE - Serial Interface Mode Select, PIN 13.**

SMODE should be tied high to select serial interface master mode, where SCLK, FSYNC and  $L/\bar{R}$  are all outputs, generated by internal dividers operating from ICLKD. SMODE should be tied low to select serial interface slave mode, where SCLK, FSYNC and  $L/\bar{R}$  are all inputs. In slave mode,  $L/\bar{R}$ , FSYNC and SCLK need to be derived from ICLKD using external dividers.

**Digital Outputs****SDATA - Serial Data Output, PIN 16.**

Audio data bits are presented MSB first, in 2's complement format. Additional tag bits, which indicate input overload and left/right channel data, are output immediately following each audio data word.

**DCAL - Digital Calibrate Output, PIN 9.**

DCAL rises immediately upon entering the power-down state (DPD brought high). It returns low 4096  $L/\bar{R}$  periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 12.288 MHz ICLKD). May be connected to ACAL.

**OCLKD - Digital Section Output Clock, PIN 21.**

OCLKD is always 128 X the output word rate. Normally connected to ICLKA.

**Digital Inputs or Outputs****SCLK - Serial Data Clock, PIN 15.**

Data is clocked out on the rising edge of SCLK for the CS5336 and CS5338. Data is clocked out on the falling edge of SCLK for the CS5339.

In master mode (SMODE high), SCLK is a continuous output clock at 64 X the output word rate.

In slave mode (SMODE low), SCLK is an input, which requires a continuously supplied clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). When FSYNC is high, SCLK clocks out serial data, except for the MSB which appears on SDATA when  $L/\bar{R}$  changes.

**$L/\bar{R}$  - Left/Right Select, PIN 14.**

In master mode (SMODE high),  $L/\bar{R}$  is an output whose frequency is at the output word rate.  $L/\bar{R}$  edges occur 1 SCLK cycle before FSYNC rises. When  $L/\bar{R}$  is high, left channel data is on SDATA, except for the first SCLK cycle. When  $L/\bar{R}$  is low, right channel data is on SDATA, except for the first SCLK cycle. The MSB data bit appears on SDATA one SCLK cycle after  $L/\bar{R}$  changes.

In slave mode (SMODE low),  $L/\bar{R}$  is an input which selects the left or right channel for output on SDATA. The rising edge of  $L/\bar{R}$  starts the MSB of the left channel data.  $L/\bar{R}$  frequency must be equal to the output word rate.

Although the outputs of each channel are transmitted at different times, the two words in an  $L/\bar{R}$  cycle represent simultaneously sampled analog inputs.

**FSYNC - Frame Synchronization Signal, PIN 17.**

In master mode (SMODE high), FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB) and falls low immediately after the last SDATA audio data bit (LSB).

In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following  $L/\bar{R}$  transitions. If it is desired to delay the data bits from the  $L/\bar{R}$  edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the  $L/\bar{R}$  edge, independent of the state of FSYNC.

**Miscellaneous****NC - No Connection, PINS 8, 22.**

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

**TST -Test Input, PIN 11.**

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

## **PARAMETER DEFINITIONS**

**Resolution** - The total number of possible output codes is equal to  $2^N$ , where N = the number of bits in the output word for each channel.

**Dynamic Range** - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

**Signal-to-(Noise plus Distortion) Ratio** - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

**Total Harmonic Distortion** - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

**Interchannel Phase Deviation** - The difference between the left and right channel sampling times.

**Interchannel Isolation** - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

**Interchannel Gain Mismatch** - The gain difference between left and right channels. Units in decibels.

**Gain Error** - The deviation of the measured full scale amplitude from the ideal full scale amplitude value.

**Gain Drift** - The change in gain value with temperature. Units in ppm/°C.

**Bipolar Offset Error** - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

### REFERENCES

- 1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.
- 2) "The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.
- 3) "An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

2

### Ordering Guide

Model	Resolution	Passband	SCLK	Temperature	Package
CS5336-KP	16-bits	22 kHz	↑ active	0°C to 70 °C	28-pin Plastic DIP
CS5336-BP	16-bits	22 kHz	↑ active	-40 to +85 °C	28-pin Plastic DIP
CS5338-KP	16-bits	24 kHz	↑ active	0°C to 70 °C	28-pin Plastic DIP
CS5339-KP	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin Plastic DIP
CS5336-KS	16-bits	22 kHz	↑ active	0°C to 70 °C	28-pin SOIC
CS5336-BS	16-bits	22 kHz	↑ active	-40 to +85 °C	28-pin SOIC
CS5338-KS	16-bits	24 kHz	↑ active	0°C to 70 °C	28-pin SOIC
CS5339-KS	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin SOIC
CS5336-TC	16-bits	22 kHz	↑ active	-55 to +125 °C	28-pin Sidebraced Ceramic DIP
CDB5336	CS5336 Evaluation Board				
CDB5338	CS5338 Evaluation Board				
CDB5339	CS5339 Evaluation Board				

## Evaluation Board for CS5336, CS5338 & CS5339

### Features

- Demonstrates recommended layout and grounding arrangements
- CS8402 Generates AES/EBU, S/PDIF & CP-340 Compatible Digital Audio
- Buffered Serial Output Interface
- 16-Bit Parallel Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

### General Description

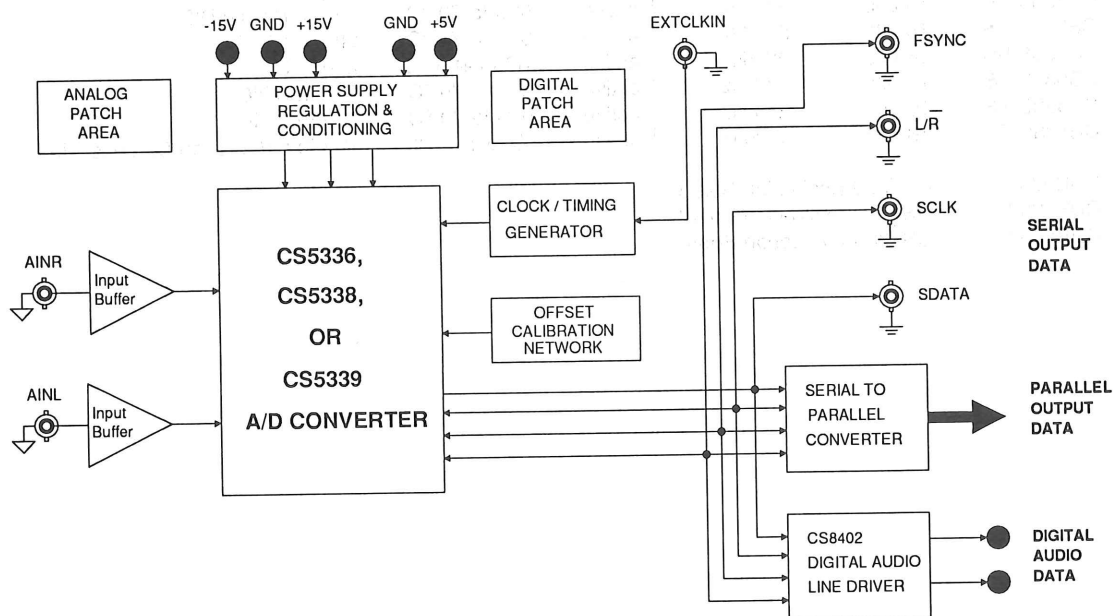
The CDB5336, CDB5338 & CDB5339 evaluation boards allow fast evaluation of the CS5336, CS5338 and CS5339 16-bit, stereo A/D converters. The boards generate all converter timing signals and provide both parallel and serial output interfaces. Evaluation requires a digital signal processor, a low-distortion signal source, and a power supply.

Also included is a CS8402 digital audio transmitter I.C., which can generate AES/EBU, S/PDIF & EIAJ CP-340 compatible audio data.

The evaluation boards may also be configured to accept external timing signals for operation in a user application during system development.

### ORDERING INFORMATION:

CDB5336, CDB5338, CDB5339



## Power Supply Circuitry

The schematic diagram in Figure 1 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by five binding posts. The  $\pm 5$  Volt analog power supply inputs of the converter are derived from  $\pm 15$  Volts using the voltage regulators U10 and U11. The +5 Volt digital supply for the converter and the discrete logic on the board is provided by the +5V and DGND binding posts. D1, D2 and D4 are transient suppressors which also provide protection from incorrectly connected power supply leads. C25-C28, C30 and C31 provide general power supply filtering for the analog supplies. As shown in Figure 2, C10-C13 provide localized decoupling for the converter VA+ and VA- pins. Note that C13 is connected between VA- and VA+ and not VA- and AGND. Space for a ferrite bead inductor, L1, has been provided so that the board may be modified to power the converter's VD+ input directly from the VA+ supply. Note that the trace connecting the VD+ power to the VD+ of the converter

must be broken before L1 may be installed. R5 and C7 low-pass filter the analog logic power supply pin, VL+. The evaluation board uses both an analog and a digital ground plane which are connected at a single point by J1. This ground plane arrangement isolates the board's digital logic from the analog circuitry.

## Offset Calibration & Reset Circuit

Figure 1, shows the optional offset calibration circuit provided on the evaluation board. Upon power-up, this circuit provides a pulse on the Analog-to-Digital Converter's DPD pin initiating an offset calibration cycle. Releasing SW1 also initiates an offset calibration cycle. P6 (see Figure 2) selects the signal source used during offset calibration. In the "AIN" position, the AINL and AINR inputs are selected during calibration, while in the "ZERO" position, the ZEROL and ZEROR inputs are selected.

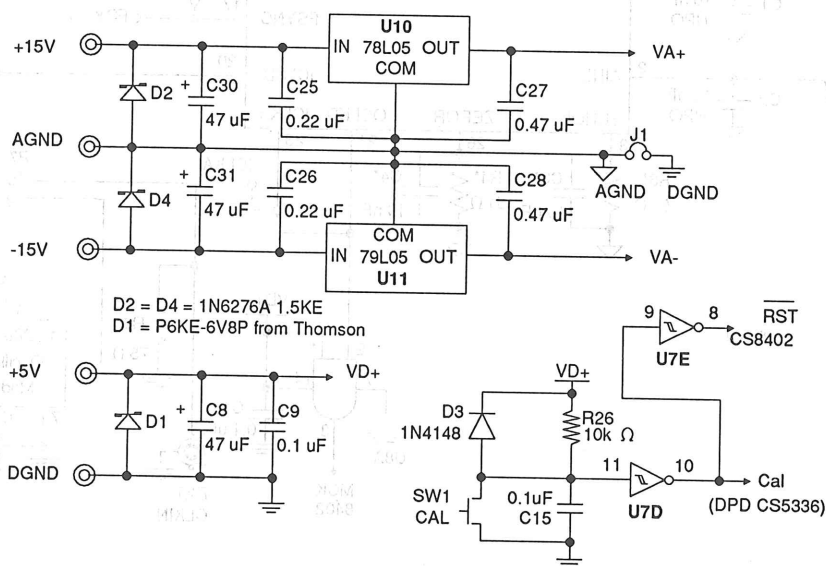
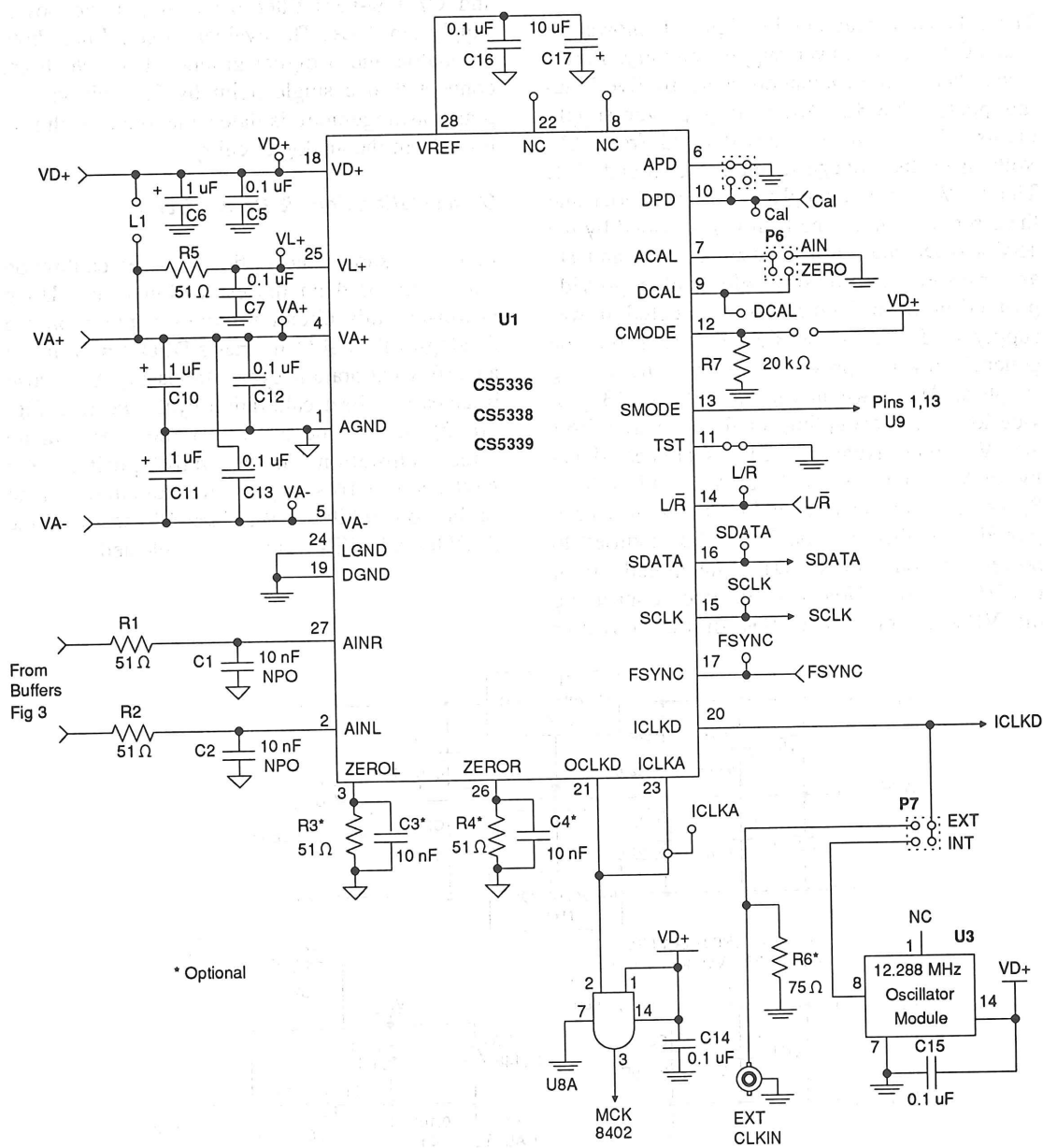


Figure 1. Power Supply and Reset Circuitry



**Figure 2 ADC Connections**



## Analog Inputs

As shown in Figure 2, the analog input signals are connected to the CS5336 via an RC network. R1 and C1 provide antialiasing and optimum source impedance for the right analog input channel while R2 and C2 do so for the left channel. The ZEROR and ZEROL inputs are tied to the analog ground plane on the board as shipped from the factory, but space is provided for an optional RC section on each. These RC sections may be added to model the output impedance of the analog signal source to minimize offset error during calibration.

Figure 3 shows the optional input buffer circuit. This can be used as an example input buffer circuit for your application. If the ADC is driven from a 50Ω source impedance signal generator, the input buffer amplifiers may be bypassed. Place P8 and P9 jumpers in the OUT position, and short circuit R1 and R2. This ensures that the ADC is driven from a 50Ω source resis-

tance. Also remove U13 op-amp, to remove the 1kΩ load impedance.

## Timing Generator

P7 selects the master clock source supplied to the ICLKD pin of the converter. As shipped from the factory, P7 is set to the "INT" position to select the 12.288 MHz clock signal provided by U3. An external master clock signal may be connected to the EXTCLKIN connector and selected by placing P7 in the "EXT" position. Note that R6, tied between EXTCLKIN and GND, is available for impedance matching an external clock source. The board is shipped with SMODE high, which selects MASTER timing mode. In this mode, SCLK, L/R and FSYNC are all outputs, generated by the converter from ICLKD.

## Serial Output Interface

The serial output interface is provided by the SDATA, SCLK, FSYNC and L/R BNC

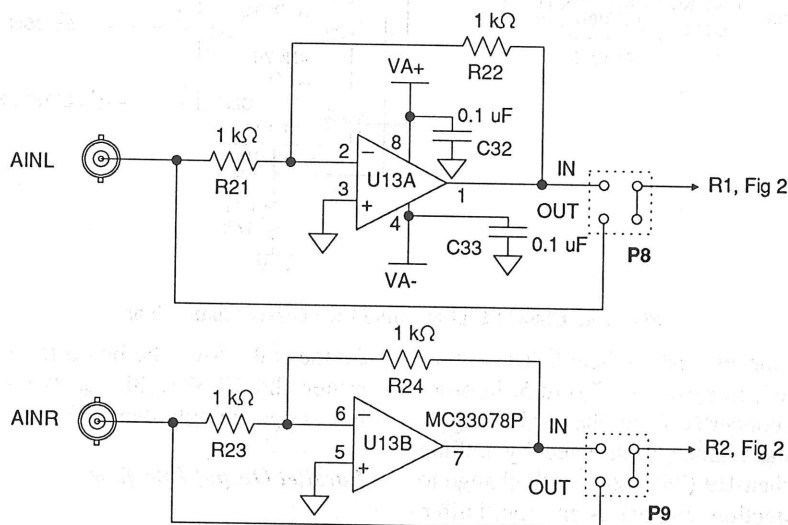


Figure 3. Input Buffer Circuit

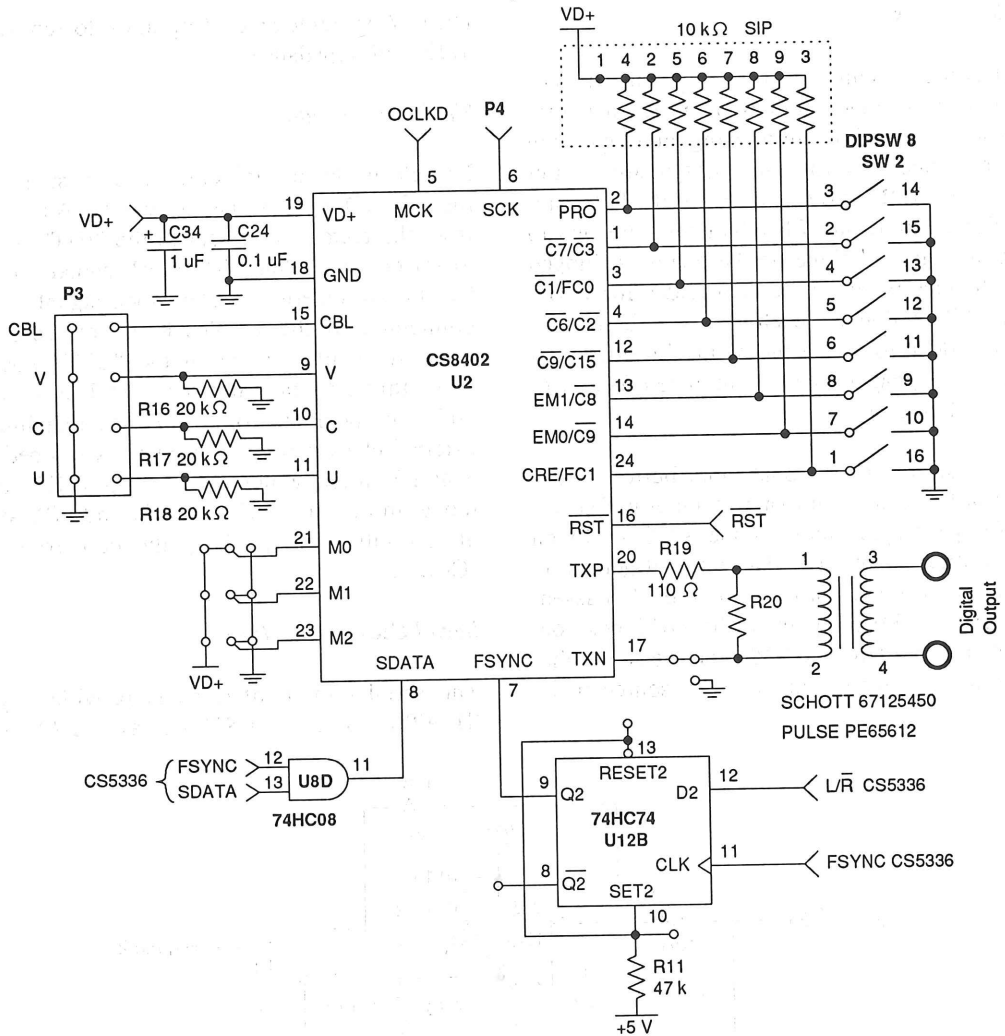


Figure 4. CS8402 Digital Audio Line Driver Connections

connectors on the evaluation board. These outputs are buffered, as shown in Figure 5, in order to isolate the converter from the digital signal processor. If slave mode is selected by pulling SMODE low, then U9 (74HC243) will change to the opposite direction, and act as an input buffer. U9 is provided to protect against inadvertent external driving of SCLK, L/R and FSYNC while in MASTER mode. U9 is not necessary in your application circuit.

Jumper P4 allows the board to be configured for either the CS5336/38, or the CS5339, which have opposite polarities of SCLK.

### Parallel Output Interface

Figure 6 depicts the parallel output interface on the evaluation board. 16-bit words are assembled from the serial data output of the converter. Each bit of serial data is clocked out of the converter



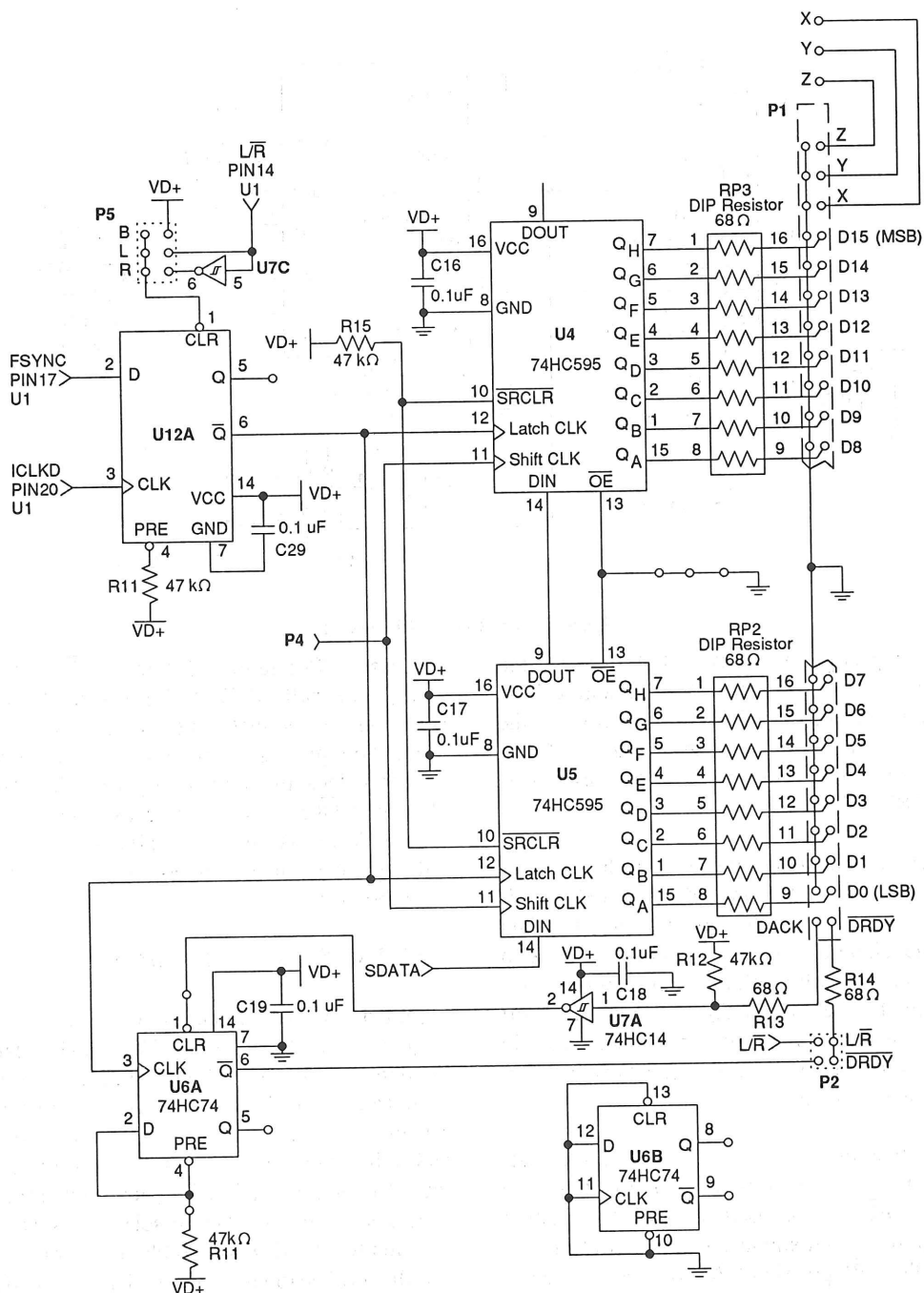


Figure 6. Parallel Output Interface

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+15	input	+15 Volts from power supply
-15	input	-15 Volts from power supply
AGND	input	analog ground connection from power supply
+5	input	+5V for ADC VD+ and discrete logic
DGND	input	digital ground connection from power supply
AINL	input	left channel analog input
AINR	input	right channel analog input
EXTCLKIN	input	external master clock input
L/R	output/input	left /right channel signal
SDATA	output	serial output data
SCLK	output/input	serial output clock
FSYNC	output/input	data framing signal
DIGITAL OUTPUT	output	CS8402 digital output via transformer
P3	output/input	CS8402 C,U,V inputs; CBL output
P1	output	parallel output data

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
P6	selects offset calibration input source	AIN *ZERO	AINL and AINR selected during offset calibration ZEROL and ZEROR selected during offset calibration
P7	selects master clock source for CS5326 CLKIN	*INT EXT	CLKIN provided by U3 CLKIN provided by EXTCLKIN BNC
P5	selects channel for serial to parallel conversion	*L R B	left channel data presented on P1 right channel data presented on P1 left then right channel data alternately presented on P1
P2	selects L/R or $\overline{\text{DRDY}}$ as the output status signal presented on P1	* $\overline{\text{DRDY}}$ L/R	$\overline{\text{DRDY}}$ selected to signal the arrival of new data for the selected channel L/R selected
P8, P9	selects optional input buffers	*IN OUT	Buffer amplifier in circuit Buffer amplifier bypassed
P4	selects device type	5337/39 5336/38	Correct SCLK for CS5337 & CS5339 Correct SCLK for CS5336 & CS5338

\* Default setting from factory

Table 2. Jumper Selectable Options

Switch#	0=Closed, 1=Open	Comment
3	$\overline{\text{PRO}}=0$	Professional Mode, C0=1 (default)
1	CRE	Local Sample Address Counter & Reliability Flags
default	0 1	Disabled Internally Generated (channel status bytes 14-17 and byte 22)
5, 2	$\overline{\text{C6}}, \overline{\text{C7}}$	C6,C7 - Sample Frequency
default	1 1 1 0 0 1 0 0	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
4	$\overline{\text{C1}}$	C1 - Audio
default	1 0	0 - Normal Audio 1 - Non-Audio
6	$\overline{\text{C9}}$	C8,C9,C10,C11 - Channel Mode (1 of 4 bits)
default	1 0	0000 - Not indicated - Default to 2-channel 0100 - Stereophonic
8, 7	EM1, EM0	C2,C3,C4 - Emphasis
default	1 1 1 0 0 1 0 0	000 - Not Indicated - default to none 100 - No emphasis 110 - 50/15 $\mu\text{s}$ 111 - CCITT J.17

Table 3. CS8402 Switch Definitions - Professional Mode

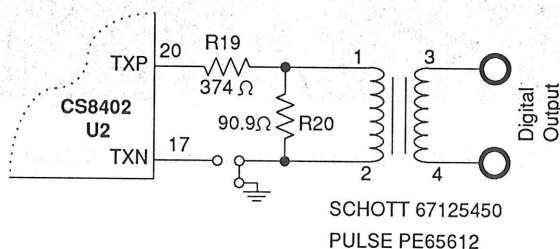
and consumer modes; however, the CS8402 output to the transformer must be modified, as shown below Table 4, to be compatible with the consumer interface. Table 4 lists the switch settings for consumer mode. If the C input of connector P3 is used, the input bits are logically OR'ed with the appropriate DIP switch bits. In Tables 3 and 4, the 'C' bits listed in the comment section are taken from the Digital Audio Interface specifications. As an example, switch 6 in the professional mode (Table 3) controls  $\overline{\text{C9}}$  which is the inverse of channel status bit 9 (also listed as byte 1, bit 1 in the CS8402 data sheet). Channel status bit 9 is one of four bits indicating channel mode. Therefore, using DIP switch 6, only two of the available channel modes may be selected. The C input port on connector P3 may be used to select other channel modes. See the

CS8401 & CS8402 part data sheet for more information on the operation of the CS8402.

Switch#	0=Closed, 1=Open	Comment
3	$\overline{PRO}=1$	Consumer Mode, C0=0 (Note 1)
1, 4	FC1, FC0	C24,C25,C26,C27 - Sample Frequency (encoded 2 of 4 bits)
	0 0	0000 - 44.1 kHz
	0 1	0100 - 48 kHz
	1 0	1100 - 32 kHz
	1 1	0000 - 44.1 kHz, CD Mode
2	$\overline{C3}$	C3,C4,C5 - Emphasis (1 of 3 bits)
	1	000 - None
	0	100 - 50/15 $\mu$ s
5	$\overline{C2}$	C2 - Copy/Copyright
	1	0 - Copy Inhibited/Copyright Asserted
	0	1 - Copy Permitted/Copyright Not Asserted
6	$\overline{C15}$	C15 - Generation Status
	1	0 - Definition is based on category code.
	0	1 - See CS8402 Data Sheet, Appendix A
8, 7	$\overline{C8}, \overline{C9}$	C8-C14 - Category Code (2 of 7 bits)
	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - Compact Disk - CD
	0 0	1100000 - Digital Audio Tape - DAT

Note: 1. The evaluation board is shipped from the factory in the Professional mode. Changing switch 3 to open places the CS8402 in Consumer mode; however, the hardware is not set up for consumer mode. To modify the hardware for Consumer mode, change R19 to 374 $\Omega$  and add R20 at 90.9 $\Omega$ . Then, as shown in the figure below, cut the trace connecting TXN to the transformer, and connect the transformer side to the ground hole provided. For a full explanation of the consumer hardware interface, see the CS8402 data sheet, Appendix B.

Table 4. CS8402 Switch Definitions - Consumer Mode





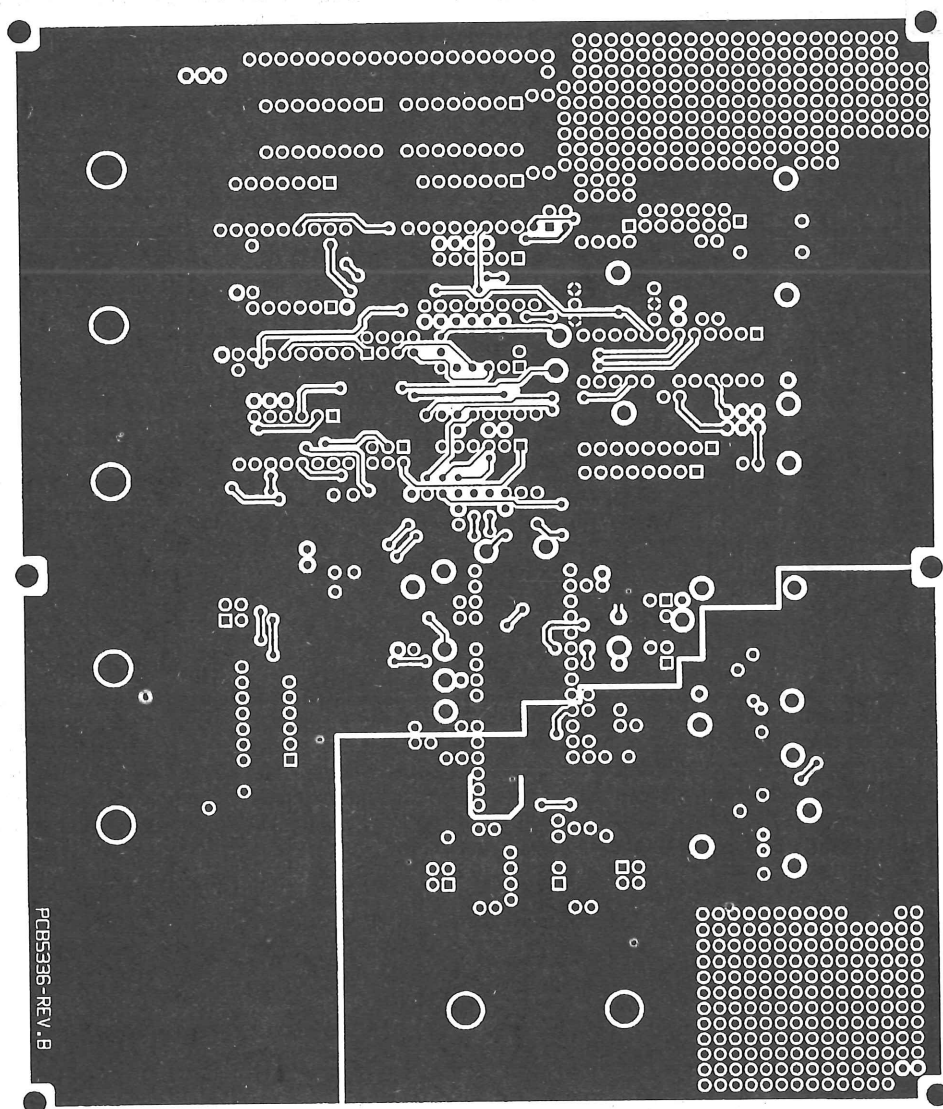


Figure 7. Top Ground Plane Layer (NOT TO SCALE)

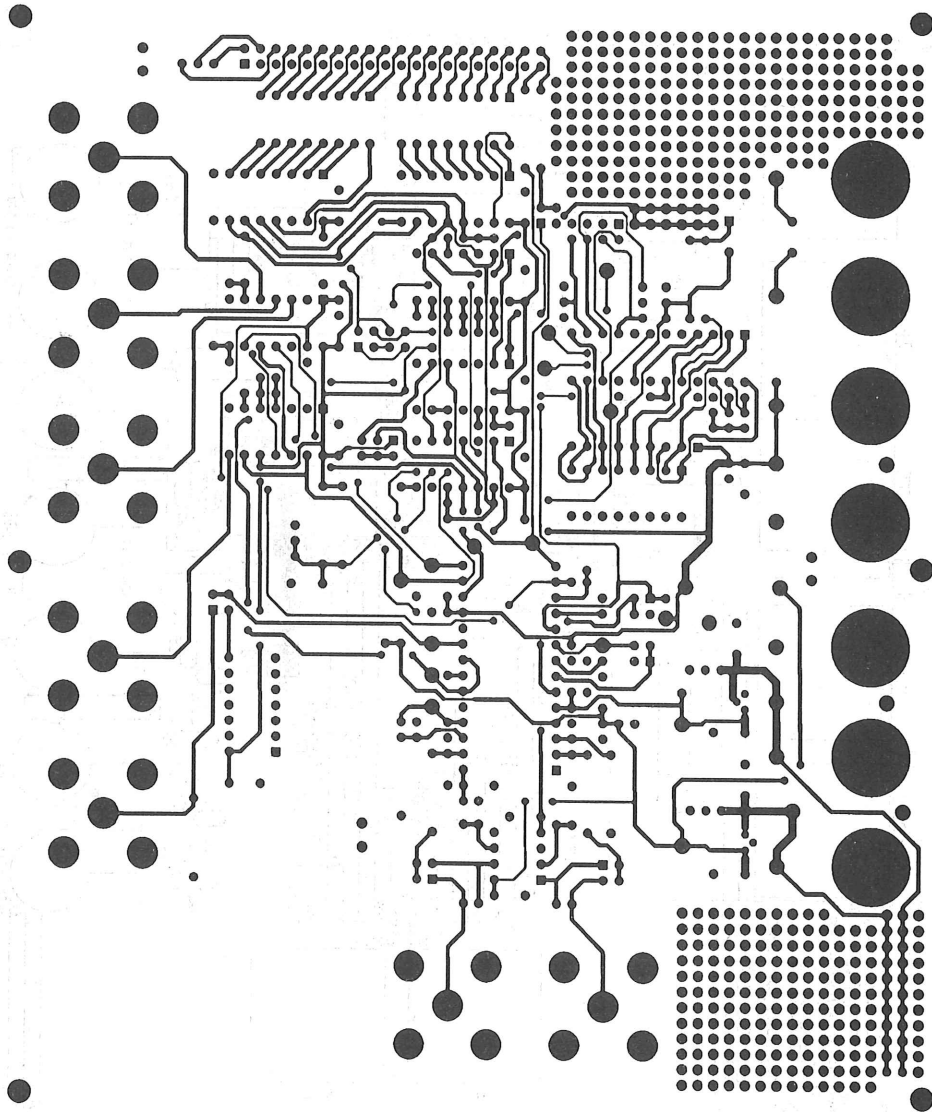


Figure 8. Bottom Trace Layer (NOT TO SCALE)

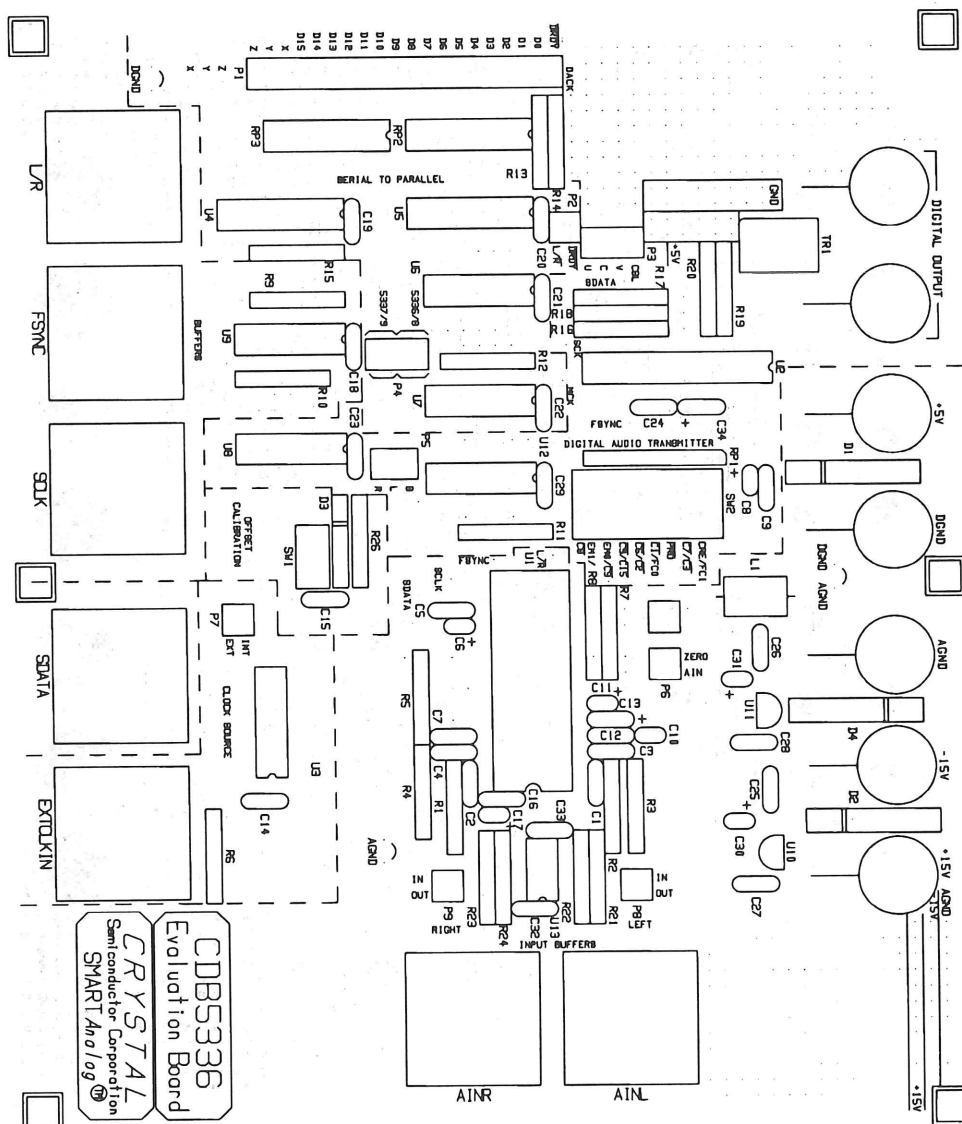


Figure 9. Component Layout (NOT TO SCALE)

# Single Supply, Stereo A/D Converter for Digital Audio

## Features

- Single +5 V Power Supply
- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- 90 dB Dynamic Range
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.01dB Passband Ripple
  - 80dB Stopband Rejection
- Low Power Dissipation: 300 mW
  - Power-Down Mode for Portable Applications
- Evaluation Board Available

## General Description

The CS5349 is a complete analog-to-digital converter which operates from a single +5V supply. It performs sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

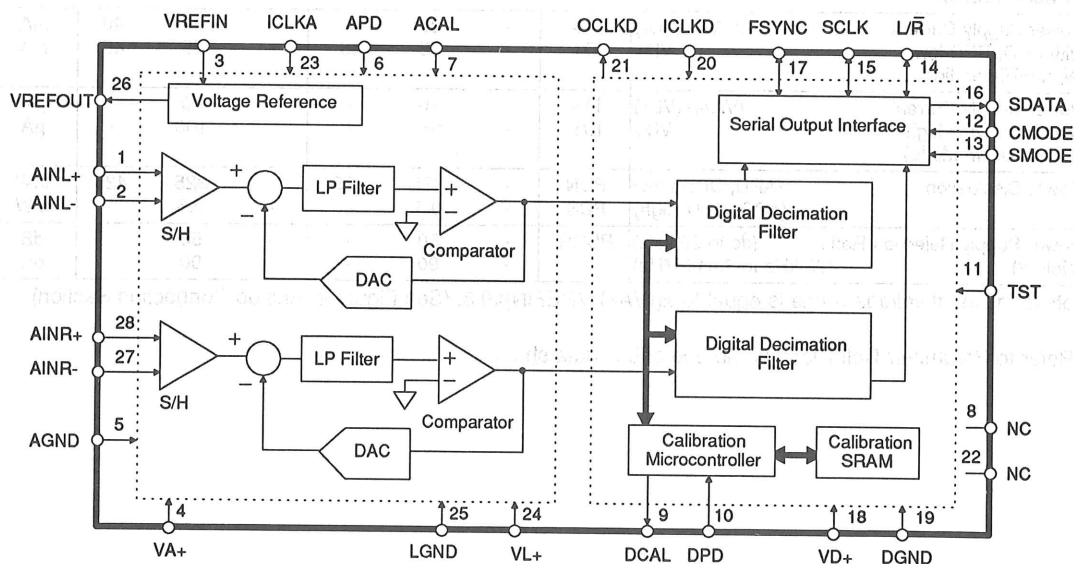
The ADC uses delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5349 has an SCLK which clocks out data on falling edges and a filter passband of dc to 24 kHz. The filter has linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The device is available housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package.

**ORDERING INFORMATION:** Page 2-213

2



**ANALOG CHARACTERISTICS** (TA = 25°C for K grade, TA = -40 °C to +85 °C for B grade; VA+, VL+, VD+ = 5V; Full-Scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 100Ω with 500 pF across AIN+, AIN-; VREFIN connected to VREFOUT; DCAL Connected to ACAL; Master Mode; Measurement Bandwidth is 10 Hz to 20 kHz; unless otherwise specified.)

Parameter*	Symbol	CS5349-K			CS5349-B			Units
		Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range	TA	0 to 70			-40 to +85			°C
Resolution		16	-	-	16	-	-	Bits
<b>Dynamic Performance</b>								
Dynamic Range		88	90	-	86	90	-	dB
Signal-to-(Noise+Distortion) THD+N	S/(N+D)	85	87	-	84	87	-	dB
Total Harmonic Distortion Vin = -10 dB, 1kHz	THD	-	0.001	0.005	-	0.001	0.005	%
Interchannel Phase Deviation		-	0.0001	-	-	0.0001	-	Degrees
Interchannel Isolation (dc to 20 kHz)		-	100	-	-	100	-	dB
<b>dc Accuracy</b>								
Interchannel Gain Mismatch		-	0.05	-	-	0.05	-	dB
Gain Error		-	±2	±5	-	±2	±5	%
Gain Drift		-	50	-	-	50	-	ppm/°C
Bipolar Offset Error (After Calibration)		-	±3	±10	-	±3	±10	LSB
Offset Calibration Range (ACAL Low)		-	±100	-	-	±100	-	mV
<b>Analog Input</b>								
Differential Input Voltage Range (Full Scale) (Note 1)	VIN	3.8	4.0	-	3.8	4.0	-	Vpp
Input Impedance	ZIN	-	50	-	-	50	-	kΩ
<b>Power Supplies</b>								
Power Supply Current (VA+)+(VL+) with APD, DPD low (Normal Operation)	IA+	-	30	40	-	30	40	mA
	ID+	-	35	45	-	35	45	mA
Power Supply Current (VA+)+(VL+) with APD, DPD high (Power-Down Mode)	IA+	-	10	-	-	10	-	μA
	ID+	-	100	-	-	100	-	μA
Power Dissipation (APD, DPD Low)	PDN	-	325	425	-	325	425	mW
	PDS	-	0.5	-	-	0.5	-	mW
Power Supply Rejection Ratio (dc to 26 kHz) (Note 2)	PSRR	-	50	-	-	50	-	dB
		-	90	-	-	90	-	dB

Notes: 1. Input voltage range is equal to ±[(VA+)-VREFIN]x0.8. (See Figure in Analog Connection Section)

\* Refer to Parameter Definitions at the end of this data sheet.

Specifications are subject to change without notice.

## DIGITAL FILTER CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ ;  $V_{A+}$ ,  $V_{L+}$ ,  $V_{D+} = 5V \pm 5\%$ ; Output word rate of 48 kHz)

Parameter	Symbol	Min	Typ	Max	Units
Passband (-3 dB)		0	to	24	kHz
(-0.01 dB)		0	to	22	kHz
Passband Ripple		-	-	$\pm 0.01$	dB
Stopband		28	to	3044	kHz
Stopband Attenuation (Note 2)		80	-	-	dB
Group Delay (OWR = Output Word Rate)	$t_{gd}$	-	18/OWR	-	s
Group Delay Variation vs. Frequency	$\Delta t_{gd}$	-	-	0.0	us

Notes: 2. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for  $n \times 3.072\text{MHz} \pm 22\text{kHz}$  where  $n = 0, 1, 2, 3, \dots$ ).

## DIGITAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ ;  $V_{A+}$ ,  $V_{L+}$ ,  $V_{D+} = 5V \pm 5\%$ )

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	$V_{IH}$	70%VD+	-	-	V
Low-Level Input Voltage	$V_{IL}$	-	-	30% VD+	V
High-Level Output Voltage at $I_o = -20\mu\text{A}$	$V_{OH}$	4.4	-	-	V
Low-Level Output Voltage at $I_o = 20\mu\text{A}$	$V_{OL}$	-	-	0.1	V
Input Leakage Current	$I_{in}$	-	1.0	-	$\mu\text{A}$

## ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to ground.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:					
Positive Analog	$V_{A+}$	-0.3	-	+6.0	V
Positive Logic	$V_{L+}$	-0.3	-	( $V_{A+}$ )+0.3	V
Positive Digital	$V_{D+}$	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies	$I_{in}$	-	-	$\pm 10$	mA
Analog Input Voltage (AIN and VREFIN pins)	$V_{INA}$	-0.3	-	( $V_{A+}$ )+0.3	V
Digital Input Voltage	$V_{IND}$	-0.3	-	( $V_{D+}$ )+0.3	V
Ambient Temperature (power applied)	$T_A$	-55	-	+125	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65	-	+150	$^\circ\text{C}$

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

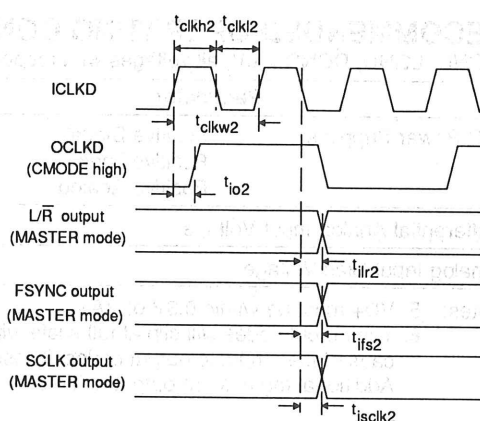
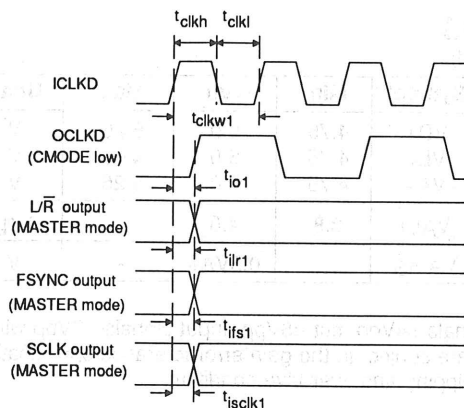
## SWITCHING CHARACTERISTICS

(T<sub>A</sub> = 25 °C; V<sub>A+</sub>, V<sub>L+</sub>, V<sub>D+</sub> = 5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = V<sub>A+</sub>, V<sub>D+</sub>; C<sub>L</sub> = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
ICLKD Period (CMODE low)	t <sub>clkw1</sub>	78	-	3906	ns
ICLKD Low (CMODE low)	t <sub>clk1</sub>	31	-	-	ns
ICLKD High (CMODE low)	t <sub>clkh1</sub>	31	-	-	ns
ICLKD rising to OCLKD rising (CMODE low)	t <sub>io1</sub>	5	-	40	ns
ICLKD Period (CMODE high)	t <sub>clkw2</sub>	52	-	2604	ns
ICLKD Low (CMODE high)	t <sub>clk2</sub>	20	-	-	ns
ICLKD High (CMODE high)	t <sub>clkh2</sub>	20	-	-	ns
ICLKD rising or falling to OCLKD rising (CMODE high, Note 3)	t <sub>io2</sub>	5	-	45	ns
ICLKD rising to L/R edge (CMODE low, MASTER mode)	t <sub>ilr1</sub>	5	-	50	ns
ICLKD rising to FSYNC edge (CMODE low, MASTER mode)	t <sub>ifs1</sub>	5	-	50	ns
ICLKD rising to SCLK edge (CMODE low, MASTER mode)	t <sub>isclk1</sub>	5	-	50	ns
ICLKD falling to L/R edge (CMODE high, MASTER mode)	t <sub>ilr2</sub>	5	-	50	ns
ICLKD falling to FSYNC edge (CMODE high, MASTER mode)	t <sub>ifs2</sub>	5	-	50	ns
ICLKD falling to SCLK edge (CMODE high, MASTER mode)	t <sub>isclk2</sub>	5	-	50	ns
SCLK falling to SDATA valid (MASTER mode)	t <sub>sdo</sub>	0	-	50	ns
SCLK duty cycle (MASTER mode)		40	50	60	%
SCLK falling to L/R (MASTER mode)	t <sub>mslr</sub>	-20	-	20	ns
SCLK falling to FSYNC (MASTER mode)	t <sub>msfs</sub>	-20	-	20	ns
SCLK Period (SLAVE mode)	t <sub>sclkw</sub>	155	-	-	ns
SCLK Pulse Width Low (SLAVE mode)	t <sub>sclkl</sub>	60	-	-	ns
SCLK Pulse Width High (SLAVE mode)	t <sub>sclkh</sub>	60	-	-	ns
SCLK falling to SDATA valid (SLAVE mode)	t <sub>dss</sub>	-	-	50	ns
L/R edge to MSB valid (SLAVE mode)	t <sub>lrdss</sub>	-	-	50	ns
Rising SCLK to L/R edge delay (SLAVE mode)	t <sub>slr1</sub>	30	-	-	ns
L/R edge to rising SCLK setup time (SLAVE mode)	t <sub>slr2</sub>	30	-	-	ns
Rising SCLK to rising FSYNC delay (SLAVE mode)	t <sub>sfs1</sub>	30	-	-	ns
Rising FSYNC to rising SCLK setup time (SLAVE mode)	t <sub>sfs2</sub>	30	-	-	ns
DPD pulse width	t <sub>pdw</sub>	2t <sub>clkw</sub>	-	-	ns
DPD rising to DCAL rising	t <sub>pcr</sub>	-	-	50	ns
DPD falling to DCAL falling (OWR = Output Word Rate)	t <sub>pcf</sub>		4096		1/OWR

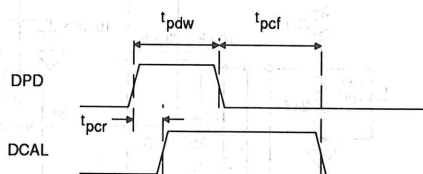
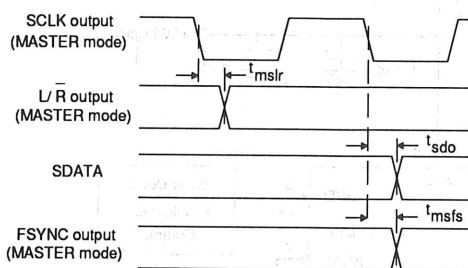
Notes: 3. ICLKD rising or falling depends on DPD to L/R timing (see Figure 2).





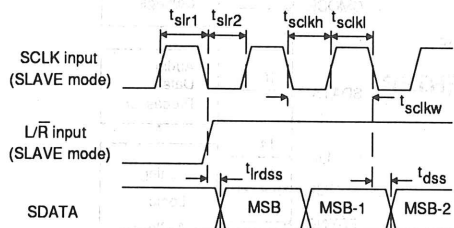
ICLKD to Outputs Propagation Delays (CMODE low)

ICLKD to Outputs Propagation Delays (CMODE high)

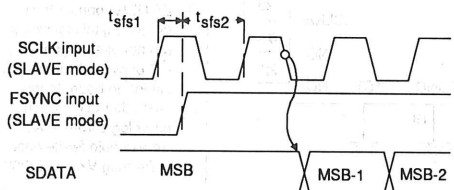


SCLK to SDATA, L/R & FSYNC - MASTER Mode

Power Down & Calibration Timing



SCLK to L/R & SDATA - SLAVE mode, FSYNC high



FSYNC to SCLK - SLAVE Mode, FSYNC Controlled.

## RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter			Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital (Note 5)	VD+	4.75	5.0	5.25	V	
	Positive Logic	VL+	4.75	5.0	VA+	V	
	Positive Analog	VA+	4.75	5.0	5.25	V	
Differential Analog Input Voltage (Note 6)			VAIN	3.8	4.0	-	Vpp
Analog Input Bias Voltage			VBIAS	-	0.5VA+	-	V

Notes: 5. VD+ must be within 0.3V of VA+.

6. The output codes will clip at full scale with input signals >4Vpp, but <8Vpp. Input signals >8Vpp will cause indeterminate output codes. These voltages are subject to the gain error tolerance specification. Additional tag bits are output to indicate a near to clipping and overdrive condition.

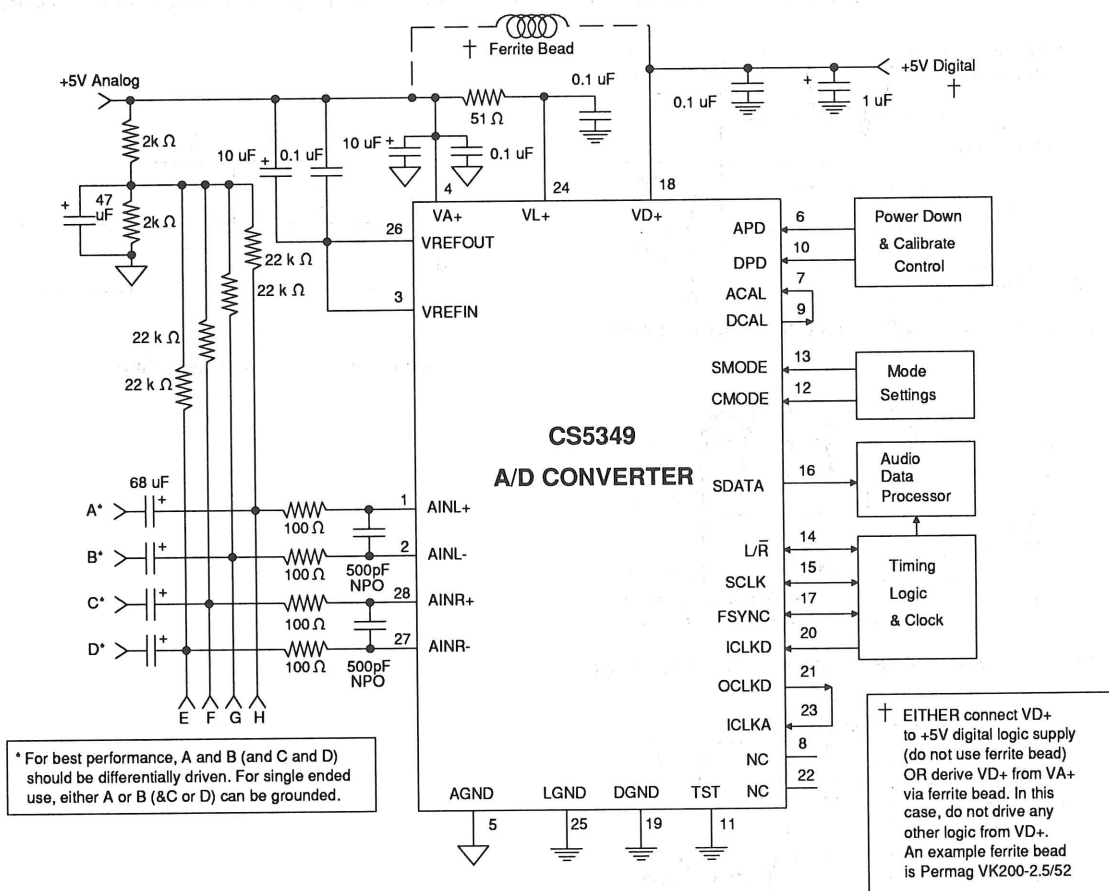


Figure 1. Typical Connection Diagram

## GENERAL DESCRIPTION

The CS5349 is a 16-bit, 2-channel A/D converter designed specifically for stereo digital audio applications that require a single +5V supply. The device uses two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 16-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for a differential input signal range of 4Vpp. Any zero offset is internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16-bit numbers. Typical power consumption of only 300 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside this ADC, see the references at the end of this data sheet.

L/R (kHz)	CMODE	ICLKD (MHz)	OCLKD/ ICLKA (MHz)	SCLK (MHz)
32	low	8.192	4.096	2.048
32	high	12.288	4.096	2.048
44.1	low	11.2896	5.6448	2.8224
44.1	high	16.9344	5.6448	2.8224
48	low	12.288	6.144	3.072
48	high	18.432	6.144	3.072

Table 1. Common Clock Frequencies

## SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

### Master Clock Input

The master input clock (ICLKD) into the ADC runs the digital filter, and is used to generate the modulator sampling clock. ICLKD frequency is determined by the desired Output Word Rate (OWR) and the setting of the CMODE pin. CMODE high will set the required ICLKD frequency to 384 X OWR, while CMODE low will set the required ICLKD frequency to 256 X OWR. Table 1 shows some common clock frequencies. The digital output clock (OCLKD) is always equal to 128 X OWR, which is always 2 X the input sample rate. OCLKD should be connected to ICLKA, which controls the input sample rate.

The phase alignment between ICLKD and OCLKD is determined as follows: when

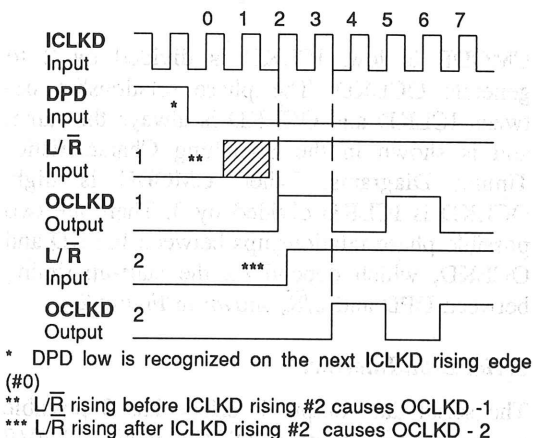


Figure 2. ICLKD to OCLKD Timing with CMODE high (384 X OWR)

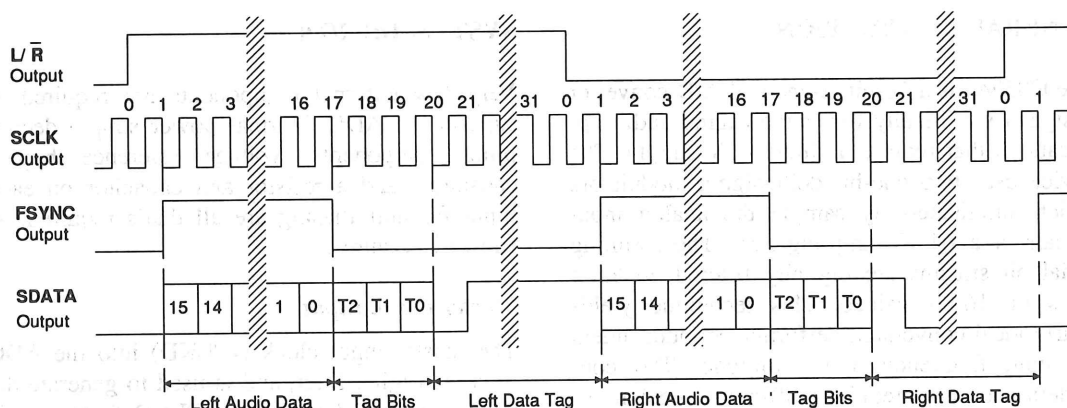


Figure 3. Data Output Timing - MASTER mode

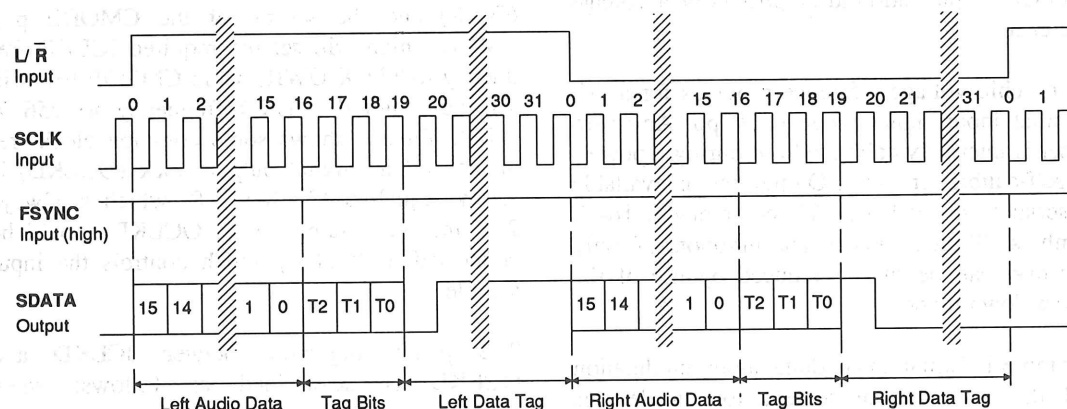


Figure 4. Data Output Timing - SLAVE Mode, FSYNC high

CMODE is low, ICLKD is divided by 2 to generate OCLKD. The phase relationship between ICLKD and OCLKD is always the same, and is shown in the Switching Characteristics Timing Diagrams. When CMODE is high, OCLKD is ICLKD divided by 3. There are two possible phase relationships between ICLKD and OCLKD, which depend on the start-up timing between DPD and  $L/\bar{R}$ , shown in Figure 2.

### Serial Data Interface

The serial data output interface has 3 possible modes of operation: MASTER mode, SLAVE mode with FSYNC high, and SLAVE mode with FSYNC controlled. In MASTER mode, the A/D

converter is driven from a master clock (ICLKD) and outputs all other clocks, derived from ICLKD (see Figure 3). Notice the one SCLK cycle delay between  $L/\bar{R}$  edges and FSYNC rising edges. FSYNC brackets the 16 data bits for each channel.

In SLAVE mode,  $L/\bar{R}$  and SCLK are inputs.  $L/\bar{R}$  must be externally derived from ICLKD, and should be equal to the Output Word Rate. SCLK should be equal to the input sample rate, which is equal to OCLKD/2. Other SCLK frequencies are possible, but may degrade dynamic range because of interference effects. Data bits are clocked out via the SDATA pin using the SCLK

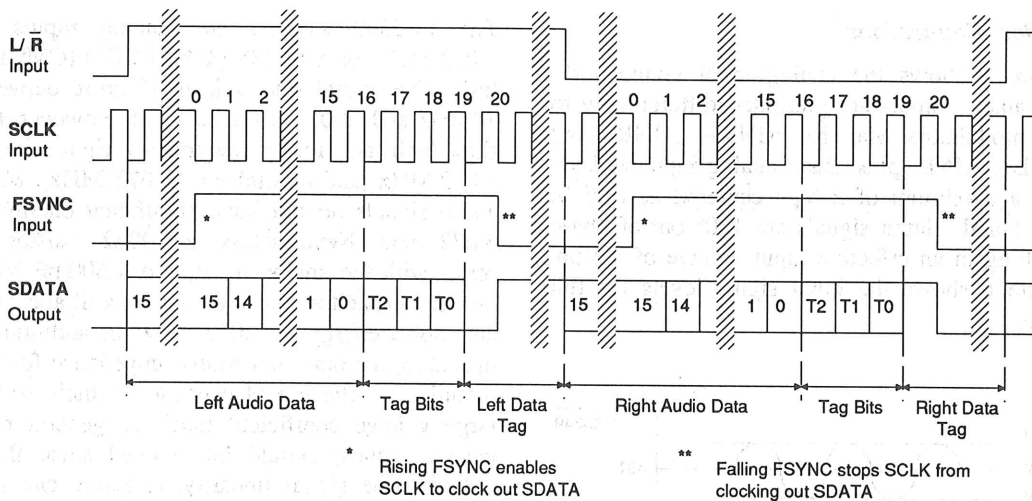


Figure 5 Data Output Timing-SLAVE Mode, FSYNC controlled

and  $L/\bar{R}$  inputs. The falling edge of SCLK causes the ADC to output each bit, except the MSB, which is clocked out by the  $L/\bar{R}$  edge. As shown in Figure 4, when FSYNC is high, serial data bits are clocked immediately following the  $L/\bar{R}$  edge.

In SLAVE mode with FSYNC controlled, as shown in Figure 5, when FSYNC is low, only the MSB is clocked out after the  $L/\bar{R}$  edge. With FSYNC low, SCLK is ignored. When it is desired to start clocking out data, bring FSYNC

high which enables SCLK to start clocking out data. Bringing FSYNC low will stop the data being clocked out. This feature is particularly useful to position in time the data bits onto a common serial bus.

The serial nature of the output data results in the left and right data words being read at different times. However, the words within an  $L/\bar{R}$  cycle represent simultaneously sampled analog inputs.

In all modes, additional bits are output after the data bits: 3 tag bits and a left/right indicator. The tag bits indicate a near-to-clipping input condition for the data word to which the tag bits are attached. Table 2 shows the relationship between input level and the tag bit values. The serial bit immediately following the tag bits is 0 for the left channel, and 1 for the right channel. The remaining bits before the next  $L/\bar{R}$  edge will be 1's for the left channel and 0's for the right channel. Normally, the tag bits are separated from the audio data by the digital signal processor. However, if the tag bits are interpreted as audio data, their position below the LSB would result as a very small dc offset.

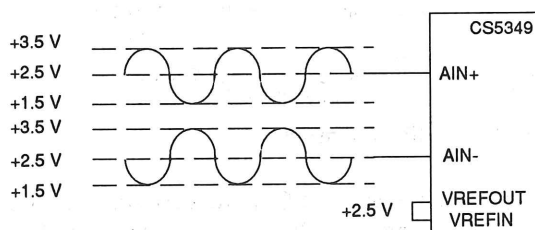
Input Level	T2	T1	T0
1.375 x FS	1	1	1
1.250 x FS to 1.375 x FS	1	1	0
1.125 x FS to 1.250 x FS	1	0	1
1.000 x FS to 1.125 x FS	1	0	0
-1.006dB to 0.000dB	0	1	1
-3.060dB to -1.006dB	0	1	0
-6.000dB to -3.060dB	0	0	1
< -6.000dB	0	0	0

FS = Full Scale (0dB) Input

Table 2. Tag Bit Definition

### Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the modulators via the AINR+, AINR- and AINL+, AINL- pins. Each analog input will accept a maximum of 2 Vpp centered at +2.5 V. The + and - input signals are 180° out of phase resulting in an effective input voltage of 4 Vpp. Figure 6 shows the input signal levels for full scale.

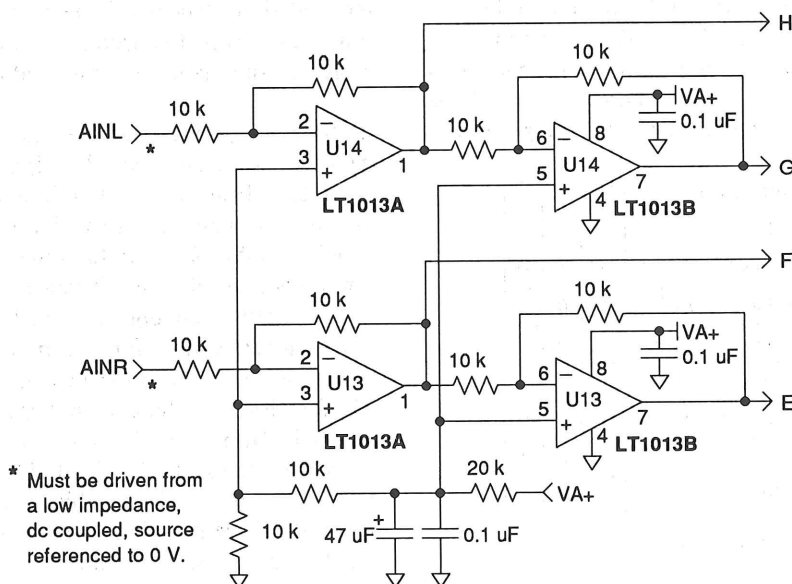


Full Scale Input level = (AIN+) - (AIN-) = 2 Vp or 4 Vpp

**Figure 6. Full Scale Input Voltage**

The CS5349 samples the analog inputs at 3.072 MHz for a 12.288 MHz ICLKD (CMODE low). The digital filter rejects all noise between 28 kHz and (3.072 MHz-28 kHz). However, the filter will not reject frequencies right around 3.072 MHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 100 Ω resistor in series with the analog input, and a 500 pF NPO or COG capacitor across the inputs will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these will degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

As an alternative to Figure 1 input arrangements, Figure 7 shows an active input buffer circuit



**Figure 7. Example Input Buffer Circuit**

which produces a differential output and level shifts up to +2.5 V. This circuit must be driven from a source which is referred to 0V dc. If this circuit is used, then the level shifting and AC coupling components shown in Figure 1 are not required.

The on-chip voltage reference output (2.5 V) is brought out to the VREFOUT pin, and normally connected to VREFIN. External reference voltages between 1.5 V and 3.0 V may be used. A 10  $\mu$ F electrolytic capacitor in parallel with a 0.1  $\mu$ F ceramic capacitor attached between VREFIN and VA+ eliminates the effects of high frequency noise. No load current may be taken from the VREFOUT output pin.

### Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 0.5 mW. In addition, exiting the power-down state initiates an offset calibration procedure.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle. If not using the power down feature, APD should be tied to AGND. When using the power down feature, DPD and APD may be tied together if the capacitor on VREF is not greater than 10  $\mu$ F, as stated in the "Power-Up Considerations" section.

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input comes from either the analog input signals or by the value obtained from shorting the differential inputs together. This input is determined by the state of the ACAL pin. With ACAL low, the calibration input is obtained from the analog inputs. With ACAL in a high state, the differential inputs are disconnected from the device input pins and shorted internally to provide the calibration input value.

As shown in Figure 8, the DCAL output is high during calibration, which takes 4096 L/R clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage resulting from the shorted inputs. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to control a multiplexer which grounds the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present in the front end input circuitry.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any

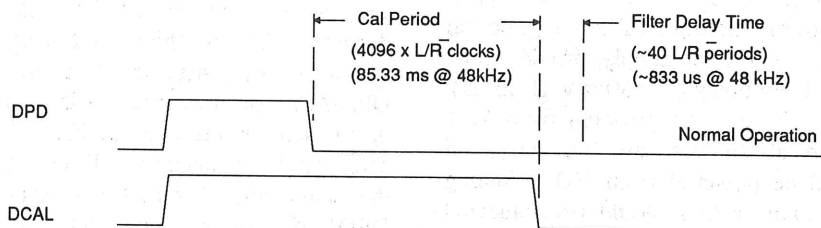


Figure 8. Initial Calibration Cycle Timing



power-on click that might otherwise be experienced. A short delay of approximately 40 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals.

### ***Power-up Considerations***

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/ $\mu$ F. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10  $\mu$ F. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

### ***Grounding and Power Supply Decoupling***

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+ and VL+ connected to a clean +5 V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy ( $< \pm 50$  mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling

capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

### ***Synchronization of Multiple CS5349***

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling. In the absence of this synchronization, the sampling difference could be one ICLKD period which is typically 81.4 nsec for a 48 kHz sample rate.

### ***SLAVE MODE***

Synchronous sampling in the slave mode is achieved by connecting all DPD and APD pins to a single control signal and supplying the same ICLKD and  $L/\bar{R}$  to all converters.

### ***MASTER MODE***

The internal counters of the CS5349 are reset during DPD/APD high and will start simultaneously by insuring that the release of DPD/APD for all converters is internally latched on the same rising edge of ICLKD. This can be achieved by connecting all DPD/APD pins to the same control signal and insuring that the DPD/APD falling edge occurs outside a  $\pm 30$  ns window either side of an ICLKD rising edge.

### PERFORMANCE

#### Digital Filter

Figures 10 through 12 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz. The filter frequency response will scale precisely with changes in output word rate. The passband ripple is flat to  $\pm 0.01$  dB maximum. Stopband rejection is greater than 80 dB. Figure 12 is an expanded view of the transition band.

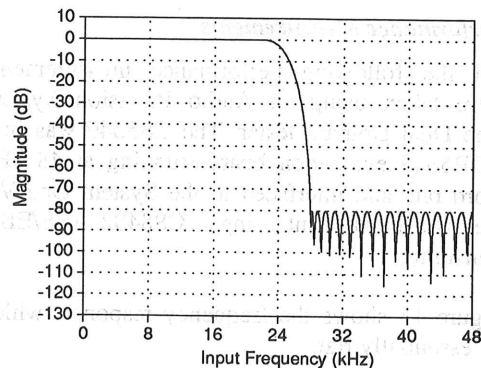


Figure 10. CS5349 Digital Filter Stopband Rejection

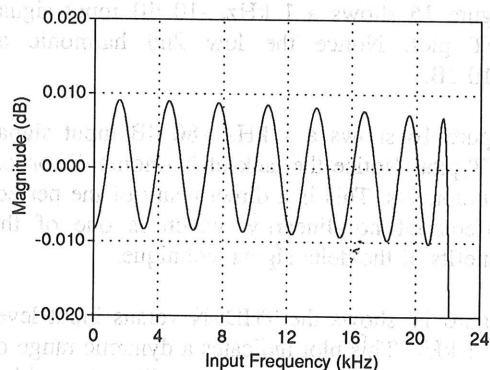


Figure 11. CS5349 Digital Filter Passband Ripple

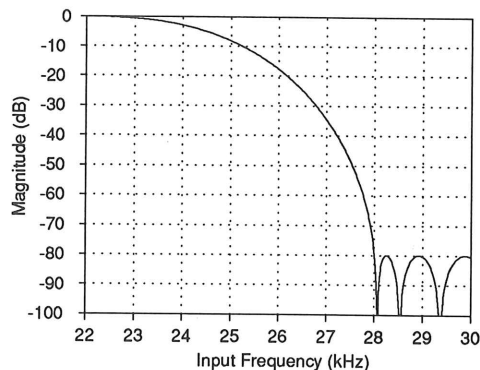


Figure 12. CS5349 Digital Filter Transition Band

### Performance Measurements

All the following performance measurements were taken using an Audio Precision System One Dual Domain tester. The CS5349 was in a CDB5349 evaluation board, running at 48 kHz word rate and interfaced to the System One Via the AES/EBU input using a CS8402 AES/EBU transmitter.

Figure 13 shows the frequency response, which is essentially flat.

Figure 14 shows the noise floor with zero input signal level. A 16 K point FFT was used.

Figure 15 shows a 1 kHz, -10 dB input signal FFT plot. Notice the low 2nd harmonic at -110 dB.

Figure 16 shows a 1 kHz, -80 dB input signal FFT plot. Notice the lack of harmonic distortion components. This is a direct result of the perfect differential non-linearity, which is one of the benefits of the delta-sigma technique.

Figure 17 shows the THD+N versus input level at 1 kHz. This plot indicates a dynamic range of 90 dB, with a small increase in distortion with a full scale input.

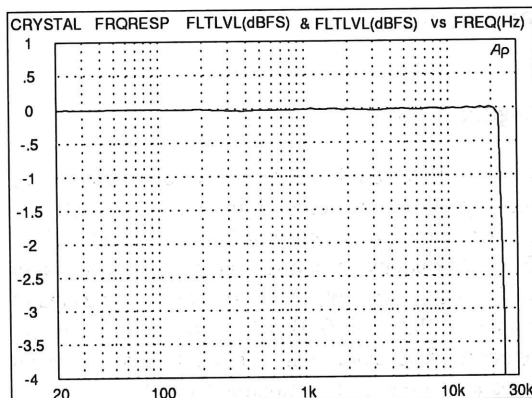


Figure 13. Frequency Response

Figure 18 shows THD+N versus frequency at -10 dB input. This indicates a value of 90 dB, with minor degradation at high frequency.

Figure 19 shows the linearity of the CS5349. The input signal is at 500 Hz and is varied from 0 dB (full scale) to -120 dB. At each input level, the output level is measured and compared to the perfect value. Any deviation is plotted as a deviation away from 0 dB. Notice the close conformance to perfect linearity, until the noise starts to influence the readings at about -100 dB.

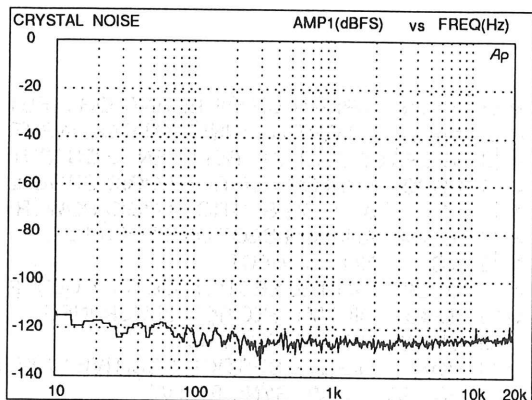


Figure 14 Noise Floor

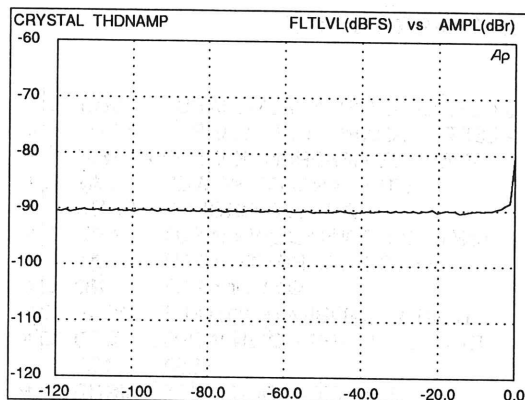


Figure 17. THD+N vs Input level at 1 kHz

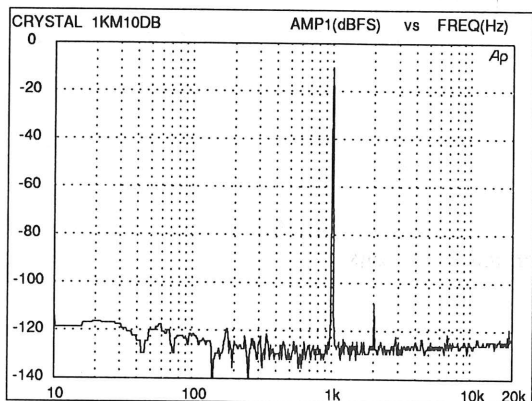


Figure 15. 1 kHz, -10 dB input FFT

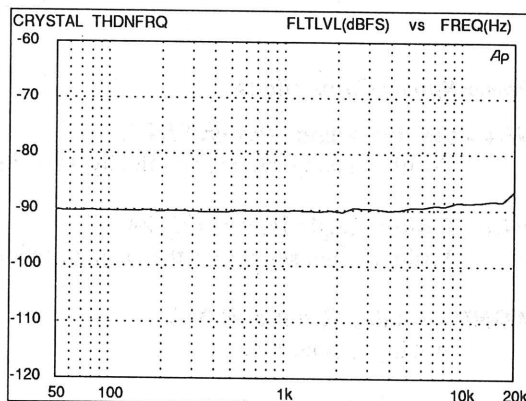


Figure 18. THD+N vs Frequency at -10 dB

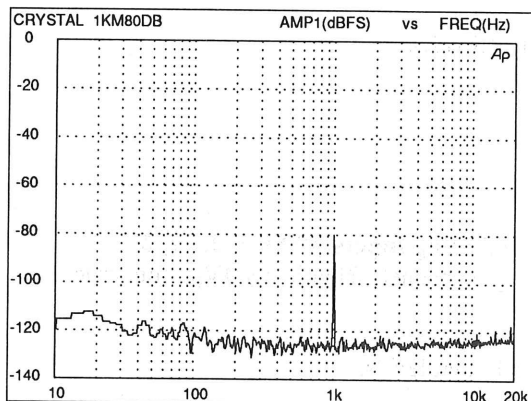


Figure 16. 1 kHz, -80 dB input FFT

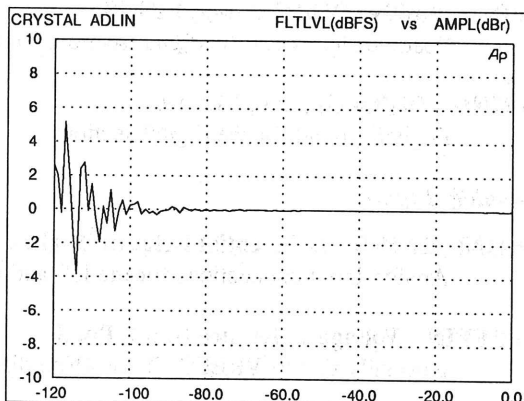


Figure 19. Output level Error vs. Input level at 500 Hz

## PIN DESCRIPTIONS

+ LEFT CHANNEL ANALOG INPUT	AINL+	1	28	AINR+	+ RIGHT CHANNEL ANALOG INPUT
- LEFT CHANNEL ANALOG INPUT	AINL-	2	27	AINR-	- RIGHT CHANNEL ANALOG INPUT
VOLTAGE REFERENCE INPUT	VREFIN	3	26	VREFOUT	VOLTAGE REFERENCE OUTPUT
POSITIVE ANALOG POWER	VA+	4	25	LGND	ANALOG SECTION LOGIC GROUND
ANALOG GROUND	AGND	5	24	VL+	ANALOG SECTION LOGIC POWER
ANALOG POWER DOWN INPUT	APD	6	23	ICLKA	ANALOG SECTION CLOCK INPUT
ANALOG CALIBRATE INPUT	ACAL	7	22	NC	NO CONNECT
NO CONNECT	NC	8	21	OCLKD	DIGITAL SECTION OUTPUT CLOCK
DIGITAL CALIBRATE OUTPUT	DCAL	9	20	ICLKD	DIGITAL SECTION CLOCK INPUT
DIGITAL POWER DOWN INPUT	DPD	10	19	DGND	DIGITAL GROUND
TEST	TST	11	18	VD+	DIGITAL SECTION POSITIVE POWER
SELECT CLOCK MODE	CMODE	12	17	FSYNC	FRAME SYNC SIGNAL
SELECT SERIAL I/O MODE	SMODE	13	16	SDATA	SERIAL DATA OUTPUT
LEFT/RIGHT SELECT	L/R	14	15	SCLK	SERIAL DATA CLOCK

### Power Supply Connections

#### VA+ - Positive Analog Power, PIN 4.

Positive analog supply. Nominally +5 volts.

#### VL+ - Positive Logic Power, PIN 24.

Positive logic supply for the analog section. Nominally +5 volts.

#### AGND - Analog Ground, PIN 5.

Analog ground reference.

#### LGND - Logic Ground, PIN 25

Ground for the logic portions of the analog section.

#### VD+ - Positive Digital Power, PIN 18.

Positive supply for the digital section. Nominally +5 volts.

#### DGND - Digital Ground, PIN 19.

Digital ground for the digital section.

### Analog Inputs

#### ±AINL, ±AINR - Differential Left and Right Channel Analog Inputs, PINS 1, 2, 27, 28

Analog input connections for the left and right input channels. Nominally 4Vpp full scale.

#### VREFIN - Voltage Reference Input, Pin 3

Normally tied to VREFOUT for 4Vpp differential input levels.

## Analog Outputs

### VREFOUT - Voltage Reference Output, PIN 26.

Nominally +2.5 volts. Must be bypassed to VA+ with a 0.1  $\mu$ F ceramic capacitor in parallel with a 10  $\mu$ F electrolytic capacitor. Normally connected to VREFIN.

## Digital Inputs

### ICLKA - Analog Section Input Clock, PIN 23.

This clock is internally divided by 2 to set the modulators' sample rate. Sampling rates, output rates, and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is 128 X the output word rate. For example, a 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD.

### ICLKD - Digital Section Input Clock, PIN 20.

This is the clock which runs the digital filter. ICLKD frequency is determined by the required output word rate and by the CMODE pin. If CMODE is low, ICLKD frequency should be 256 X the desired output word rate. If CMODE is high, ICLKD should be 384 X the desired output word rate. For example, with CMODE low, ICLKD should be 12.288 MHz for an output word rate of 48 kHz. This clock also generates OCLKD, which is always 128 X the output word rate.

### APD - Analog Power Down, PIN 6.

Analog section power-down command. When high, the analog circuitry is in power-down mode. APD is normally connected to DPD when using the power down feature. If power down is not used, then connect APD to AGND.

### DPD - Digital Power Down, PIN 10

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 L/R periods (85.33 ms with a 12.288 MHz ICLKD). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD when using the power down feature. A calibration cycle should always be initiated after applying power to the supply pins.

### ACAL - Analog Calibrate, PIN 7.

Analog section calibration command. When high, causes the left and right channel modulator differential inputs to be shorted together. May be connected to DCAL.

### CMODE - Clock Mode Select, PIN 12.

CMODE should be tied low to select an ICLKD frequency of 256 X the output word rate. CMODE should be tied high to select an ICLKD frequency of 384 X the output word rate.

**SMODE - Serial Interface Mode Select, PIN 13.**

SMODE should be tied high to select serial interface master mode, where SCLK, FSYNC and L/R are all outputs, generated by internal dividers operating from ICLKD. SMODE should be tied low to select serial interface slave mode, where SCLK, FSYNC and L/R are all inputs. In slave mode, L/R, FSYNC and SCLK need to be derived from ICLKD using external dividers.

**Digital Outputs****SDATA - Serial Data Output, PIN 16.**

Audio data bits are presented MSB first, in 2's complement format. Additional tag bits, which indicate input overload and left/right channel data, are output immediately following each audio data word.

**DCAL - Digital Calibrate Output, PIN 9.**

DCAL rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 L/R periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 12.288 MHz ICLKD). May be connected to ACAL.

**OCLKD - Digital Section Output Clock, PIN 21.**

OCLKD is always 128 X the output word rate. Normally connected to ICLKA.

**Digital Inputs or Outputs****SCLK - Serial Data Clock, PIN 15.**

Data is clocked out on the falling edge of SCLK.

In master mode (SMODE high), SCLK is a continuous output clock at 64 X the output word rate.

In slave mode (SMODE low), SCLK is an input, which requires a clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). When FSYNC is high, SCLK clocks out serial data, except for the MSB which appears on SDATA when L/R changes.

**L/R - Left/Right Select, PIN 14.**

In master mode (SMODE high), L/R is an output whose frequency is at the output word rate. L/R edges occur 1 SCLK cycle before FSYNC rises. When L/R is high, left channel data is on SDATA, except for the first SCLK cycle. When L/R is low, right channel data is on SDATA, except for the first SCLK cycle. The MSB data bit appears on SDATA one SCLK cycle after L/R changes.

In slave mode (SMODE low), L/R is an input which selects the left or right channel for output on SDATA. The rising edge of L/R starts the MSB of the left channel data. L/R frequency must be equal to the output word rate.

Although the outputs of each channel are transmitted at different times, the two words in an L/R cycle represent simultaneously sampled analog inputs.



**FSYNC - Frame Synchronization Signal, PIN 17.**

In master mode (SMODE high), FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB) and falls low immediately after the last SDATA audio data bit (LSB).

In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/R transitions. If it is desired to delay the data bits from the L/R edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the L/R edge, independent of the state of FSYNC.

**Miscellaneous****NC - No Connection, PINS 8, 22.**

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

**TST -Test Input, PIN 11.**

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

---

**PARAMETER DEFINITIONS**

**Resolution** - The total number of possible output codes is equal to  $2^N$ , where N = the number of bits in the output word for each channel.

**Dynamic Range** - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

**Signal-to-Noise plus Distortion Ratio** - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

**Total Harmonic Distortion** - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

**Interchannel Phase Deviation** - The difference between the left and right channel sampling times.

**Interchannel Isolation** - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

**Interchannel Gain Mismatch** - The gain difference between left and right channels. Units in decibels.

**Gain Error** - The deviation of the measured full scale amplitude from the ideal full scale amplitude value.

**Gain Drift** - The change in gain value with temperature. Units in ppm/°C.

**Bipolar Offset Error** - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

## REFERENCES

- 1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988. Reprinted in the 1990 VOL 1 Crystal Data Book.
- 2) "The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.
- 3) "An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989. Reprinted in the 1990 VOL 1 Crystal Data Book.

## Ordering Guide

Model	Resolution	Passband	SCLK	Temperature	Package
CS5349-KP	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin Plastic DIP
CS5349-BP	16-bits	24 kHz	↓ active	-40°C to 85 °C	28-pin Plastic DIP
CS5349-KS	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin SOIC
CS5349-BS	16-bits	24 kHz	↓ active	-40°C to 85 °C	28-pin SOIC

CDB5349 CS5349 Evaluation Board

"KP" and "KS" suffix parts are guaranteed to operate over 0°C to 70°C, but tested only at 25°C. "BP" and "BS" suffix parts are tested at the temperature extremes -40°C and +85°C.

## Evaluation Board for CS5349

### Features

- Demonstrates recommended layout and grounding arrangements
- CS8402 Generates AES/EBU, SPDIF & EIAJ-340 Compatible Digital Audio
- Buffered Serial Output Interface
- 16-Bit Parallel Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

### General Description

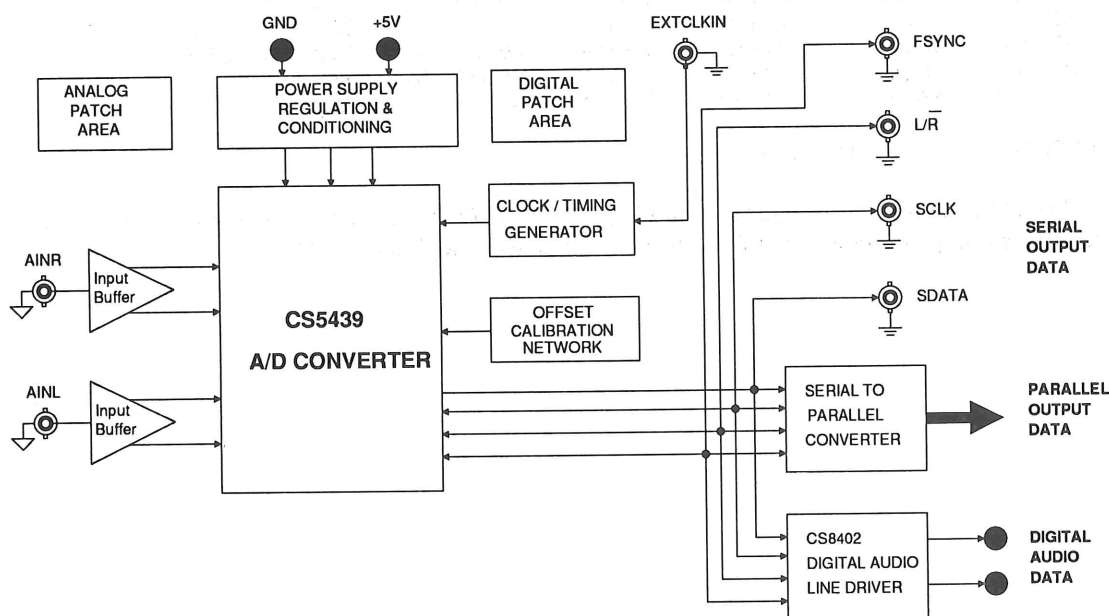
The CDB5349 evaluation board allows fast evaluation of the CS5349 16-bit, stereo A/D converter. The board generates all converter timing signals and provides both parallel and serial output interfaces. Evaluation requires a digital signal processor, a low-distortion signal source, and a power supply.

Also included is a CS8402 digital audio transmitter I.C., which can generate AES/EBU, SPDIF & EIAJ-340 compatible audio data.

The evaluation boards may also be configured to accept external timing signals for operation in a user application during system development.

### ORDERING INFORMATION:

CDB5349



## Power Supply Circuitry

The schematic diagram in Figure 1 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by four binding posts. The +5 Volt analog power supply input for the converter is provided by the +5V and AGND binding posts. The +5 Volt digital supply for the converter and the discrete logic on the board is provided by the +5V and DGND binding posts. D1 and D2 are transient suppressors which also provide protection from incorrectly connected power supply leads. C30 provides general power supply filtering for the analog supply. As shown in Figure 2, C10 and C12 provide localized decoupling for the converter VA+ pin. Space for a ferrite bead inductor, L1, has been provided so that the board may be modified to power the converter's VD+ input directly from the VA+ supply. Note that the trace connecting VD+ to L1 must be broken before L1 may be installed. R5 and C7 low-pass filter the analog logic power supply pin, VL+. The evaluation board uses both an analog and a digi-

tal ground plane which are connected at a single point by J1. This ground plane arrangement isolates the board's digital logic from the analog circuitry.

## Offset Calibration & Reset Circuit

Figure 1, shows the optional offset calibration circuit provided on the evaluation board. Upon power-up, this circuit provides a pulse on the Analog to Digital Converter's DPD pin initiating an offset calibration cycle. Releasing SW1 also initiates an offset calibration cycle. P6 (see Figure 2) selects the signal source used during offset calibration. In the "AIN" position, the AINL and AINR inputs are selected during calibration. In the "ZERO" position, the AINL and AINR inputs are disconnected and the differential inputs shorted for calibration.

## Analog Inputs

As shown in Figure 2, the analog input signals are connected to the CS5349 via an RC network.

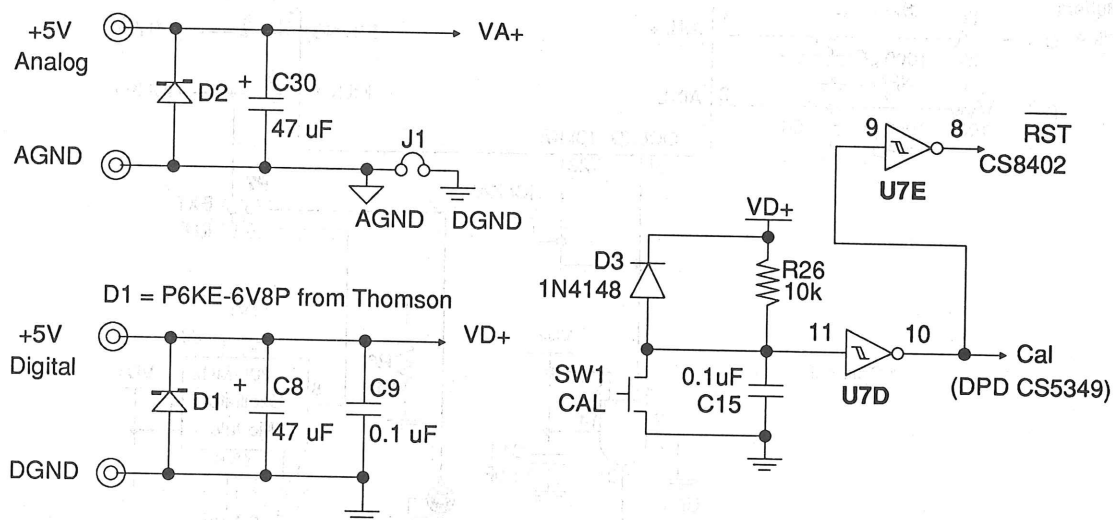


Figure 1. Power Supply and Reset Circuitry

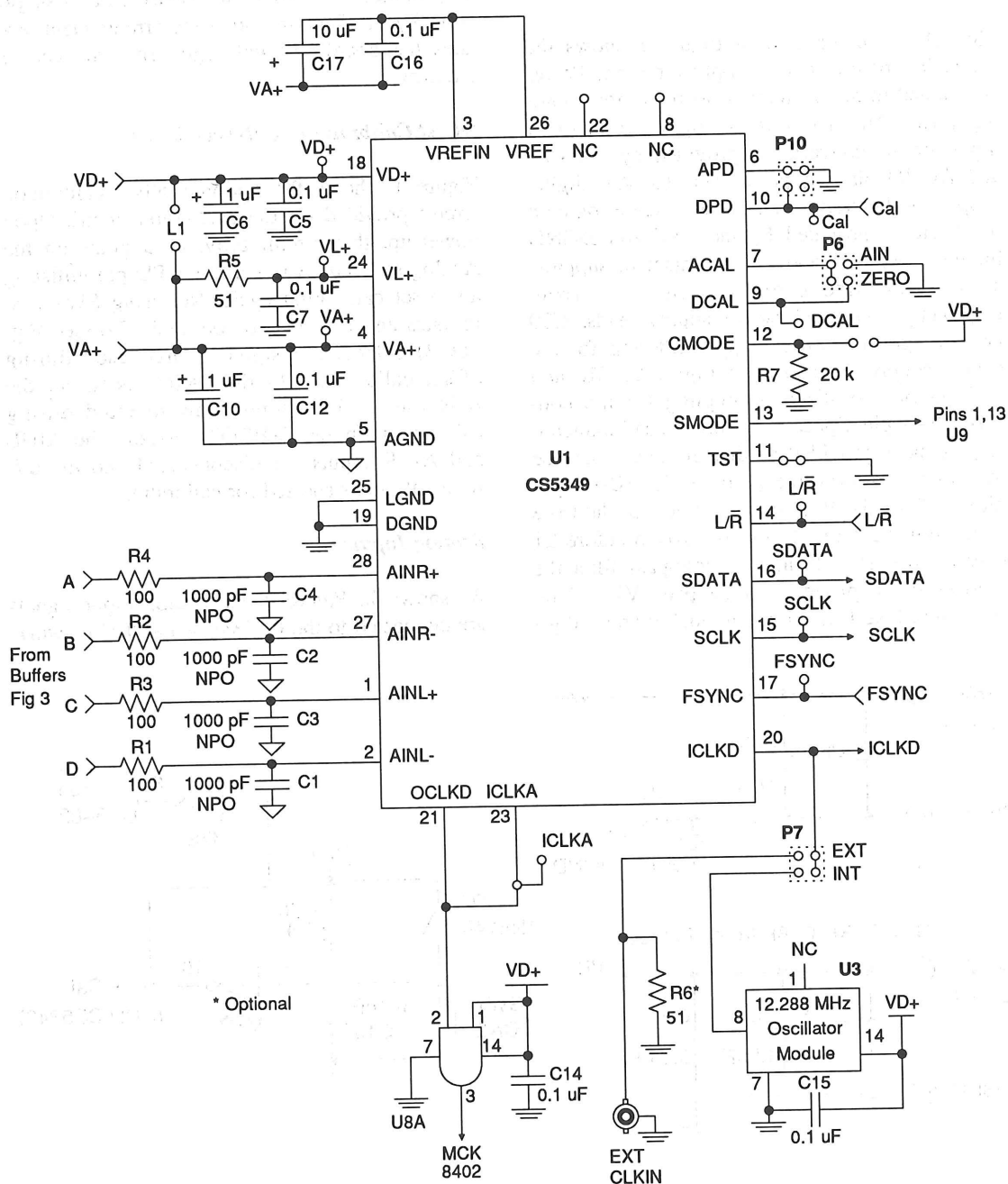


Figure 2. ADC Connections





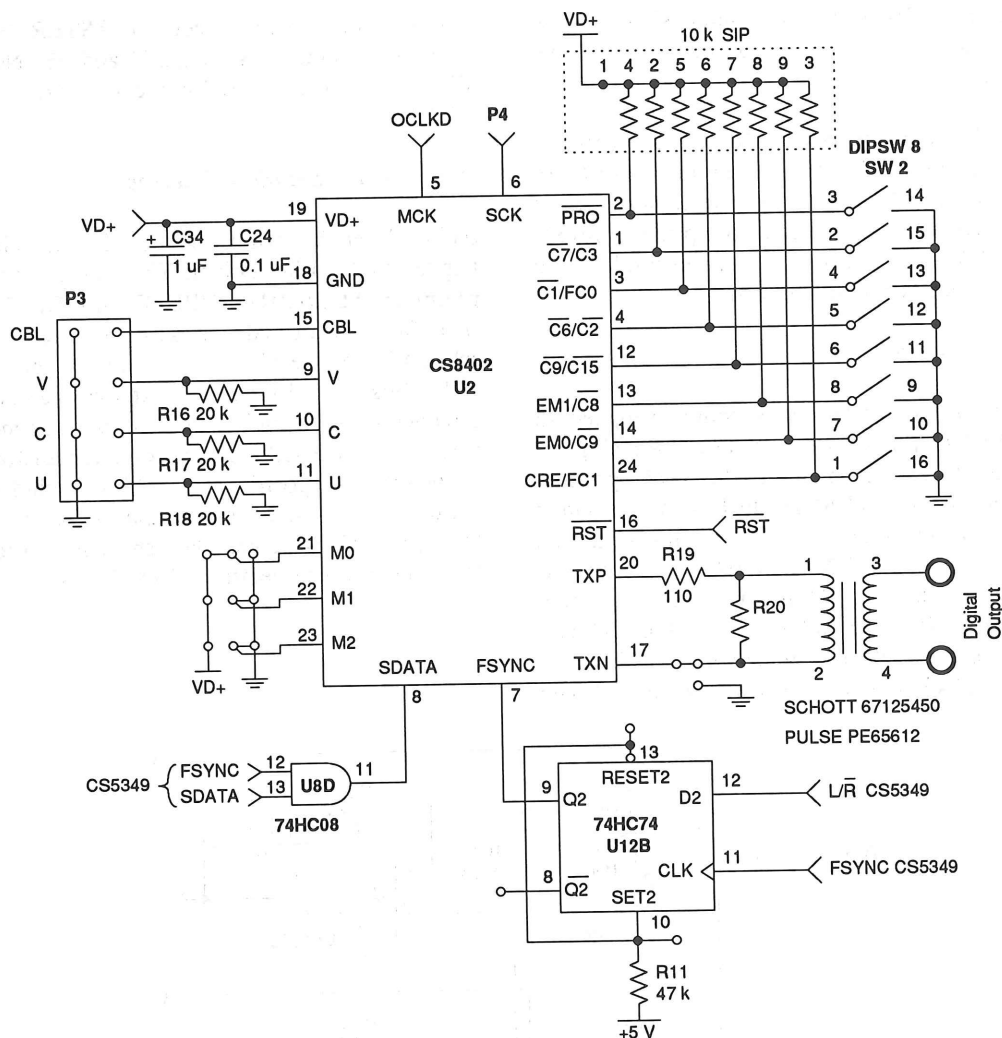


Figure 4. CS8402 Digital Audio Line Driver Connections

### Serial Output Interface

The serial output interface is provided by the SDATA, SCLK, FSYNC and L/R BNC connectors on the evaluation board. These outputs are buffered, as shown in Figure 5, in order to isolate the converter from the digital signal processor. If slave mode is selected by pulling SMODE low, then U9 (74HC243) will change to the opposite direction, and act as an input buffer.

U9 is provided to protect against inadvertent external driving of SCLK, L/R and FSYNC while in MASTER mode. U9 is not necessary in your application circuit.

Jumper P4 allows the board to be configured for either the CS5346, or the CS5349, which have opposite polarities of SCLK.

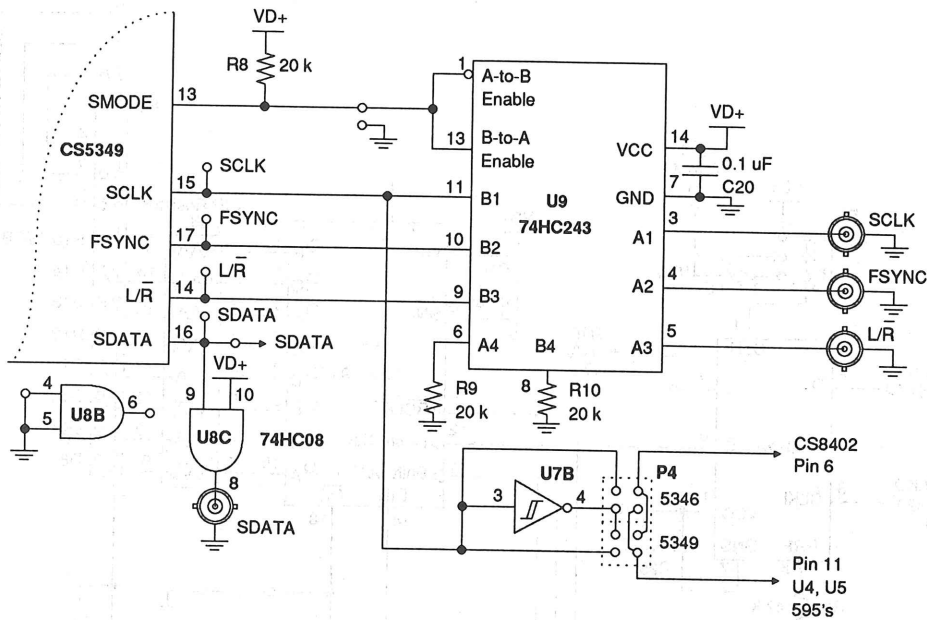


Figure 5. Serial Output Interface

### Parallel Output Interface

Figure 6 depicts the parallel output interface on the evaluation board. 16-bit words are assembled from the serial data output of the converter. Each bit of serial data is clocked out of the converter on the rising edge of SCLK and shifted into the 16-bit shift register formed by U4 and U5 on SCLK's falling edge. After all data bits for the selected channel have been shifted into U4 and U5 the data is latched onto P1 by a delayed version of FSYNC.

P5 selects the channel whose output data will be converted to parallel form and presented on P1. With P5 in the "B" (both) position, parallel data from one channel will be presented first with data from the other channel presented subsequently. In the "L" (left) position, only left channel conversions will be presented, while in the "R" (right) position only right channel conversions are presented.

Two interface mechanisms are provided for reading the data from this port. With the first, the edges of  $\overline{L/R}$  may be used to clock the parallel data into the digital signal processor. (Set jumper P2 into the  $\overline{L/R}$  position.) Alternatively, a handshake protocol implemented with  $\overline{DACK}$  and  $\overline{DRDY}$  may be used to transfer data to the signal processor. (Set jumper P2 to the  $\overline{DRDY}$  position.) The fall of  $\overline{DRDY}$  informs the digital signal processor that a new data word is available. The processor then reads the port and acknowledges the transfer by asserting  $\overline{DACK}$ . Note that  $\overline{DRDY}$  will not be asserted again unless  $\overline{DACK}$  is momentarily brought high although new data will continue to be latched onto the port.



CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5 ANALOG	input	+5 Volts from analog power supply
AGND	input	analog ground connection from power supply
+5 DIGITAL	input	+5V digital supply for ADC VD+ and discrete logic
DGND	input	digital ground connection from power supply
AINL	input	left channel analog input
AINR	input	right channel analog input
EXTCLKIN	input	external master clock input
$\overline{L/R}$	output/input	left /right channel signal
SDATA	output	serial output data
SCLK	output/input	serial output clock
FSYNC	output/input	data framing signal
DIGITAL OUTPUT	output	CS8402 digital output via transformer
P3	output/input	CS8402 C,U,V inputs; CBL output
P1	output	parallel output data

Table 1. Systems Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
P6	selects signal offset or shorted inputs for calibration	AIN ZERO	offset cal to signal input offset cal to shorted inputs
P7	selects master clock source for CS5349	*INT EXT	CLKIN provided by U2 CLKIN provided by EXTCLKIN BNC
P5	selects channel for serial to parallel conversion	*L R B	left channel data presented on P5 right channel data presented on P5 left then right channel data alternately presented on P5
P2	selects $\overline{L/R}$ or $\overline{DRDY}$ as the output status signal presented on P1	* $\overline{DRDY}$ $\overline{L/R}$	$\overline{DRDY}$ selected to signal the arrival of new data for the selected channel $\overline{L/R}$ selected
P4	selects device type	5349 5346	Correct SCLK for CS5349 Correct SCLK for CS5346

\* Default setting from factory

Table 2. Jumper Selectable Options

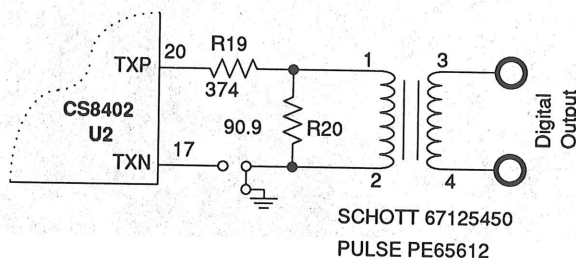
Switch#	0=Closed, 1=Open	Comment
3	$\overline{\text{PRO}}=0$	Professional Mode C0=1(default)
1	CRE	Local Sample Address Counter & Reliability Flags
default	0 1	Disabled Internally Generated
2,5	$\overline{\text{C6}}, \overline{\text{C7}}$	C6,C7 - Sample Frequency
default	1 1 1 0 0 1 0 0	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
4	$\overline{\text{C1}}$	C1 - Audio
default	1 0	0 - Normal Audio 1 - Non-Audio
6	$\overline{\text{C9}}$	C8,C9,C10,C11 - Channel Mode (1 of 4 bits)
default	1 0	0000 - Not indicated - Default to 2-channel 0100 - Stereophonic
8,7	EM1, EM0	C2,C3,C4 - Emphasis (2 of 3 bits)
default	1 1 1 0 0 1 0 0	000 - Not Indicated - default to none 100 - No emphasis 110 - 50/15 $\mu\text{s}$ 111 - CCITT J.17

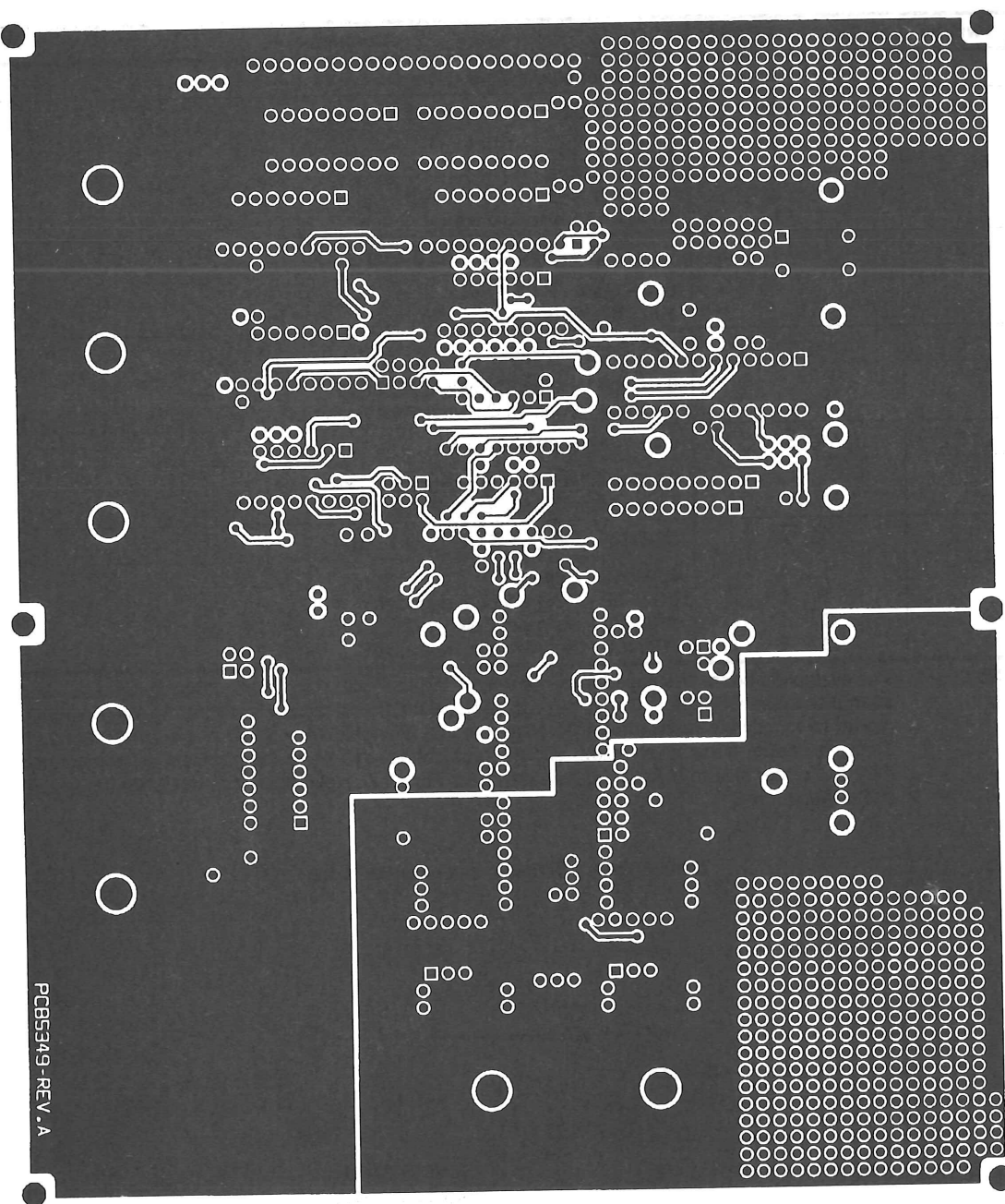
**Table 3. Switch Definitions - Professional Mode**

Switch#	0=Closed, 1=Open	Comment
3	$\overline{\text{PRO}}=1$	Consumer Mode C1=0 (Note 1)
1,4	FC1, FC0	C24,C25,C26,C27 - Sample Frequency
	0 0	0000 - 44.1 kHz
	0 1	0100 - 48 kHz
	1 0	1100 - 32 kHz
	1 1	0000 - 44.1 kHz, CD Mode
2	$\overline{\text{C3}}$	C3,C4,C5 - Emphasis (1 of 3 bits)
	1	000 - None
	0	100 - 50/15 $\mu\text{s}$
5	$\overline{\text{C2}}$	C2 - Copy/Copyright
	1	0 - Copy Inhibited/Copyright Asserted
	0	1 - Copy Permitted/Copyright Not Asserted
6	$\overline{\text{C15}}$	C15 - Generation Status
	1	0 - Definition is based on category code.
	0	1 - See CS8402 Data Sheet, App. A
8,7	$\overline{\text{C8}}, \overline{\text{C9}}$	C8-C14 - Category Code (2 of 7 bits)
	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - Compact Disk - CD
	0 0	1100000 - Digital Audio Tape - DAT

Note: 1. The evaluation board is shipped from the factory in the Professional mode. Changing switch 3 to open places the CS8402 in Consumer mode; however, the hardware is not set up for consumer mode. To modify the hardware for Consumer mode, change R19 to 374 $\Omega$  and add R20 at 90.9 $\Omega$ . Then, as shown in the figure below, cut the trace connecting TXN to the transformer, and connect the transformer side to the ground hole provided. For a full explanation, see the CS8402 data sheet, Appendix B.

Table 4. Switch Definitions - Consumer Mode



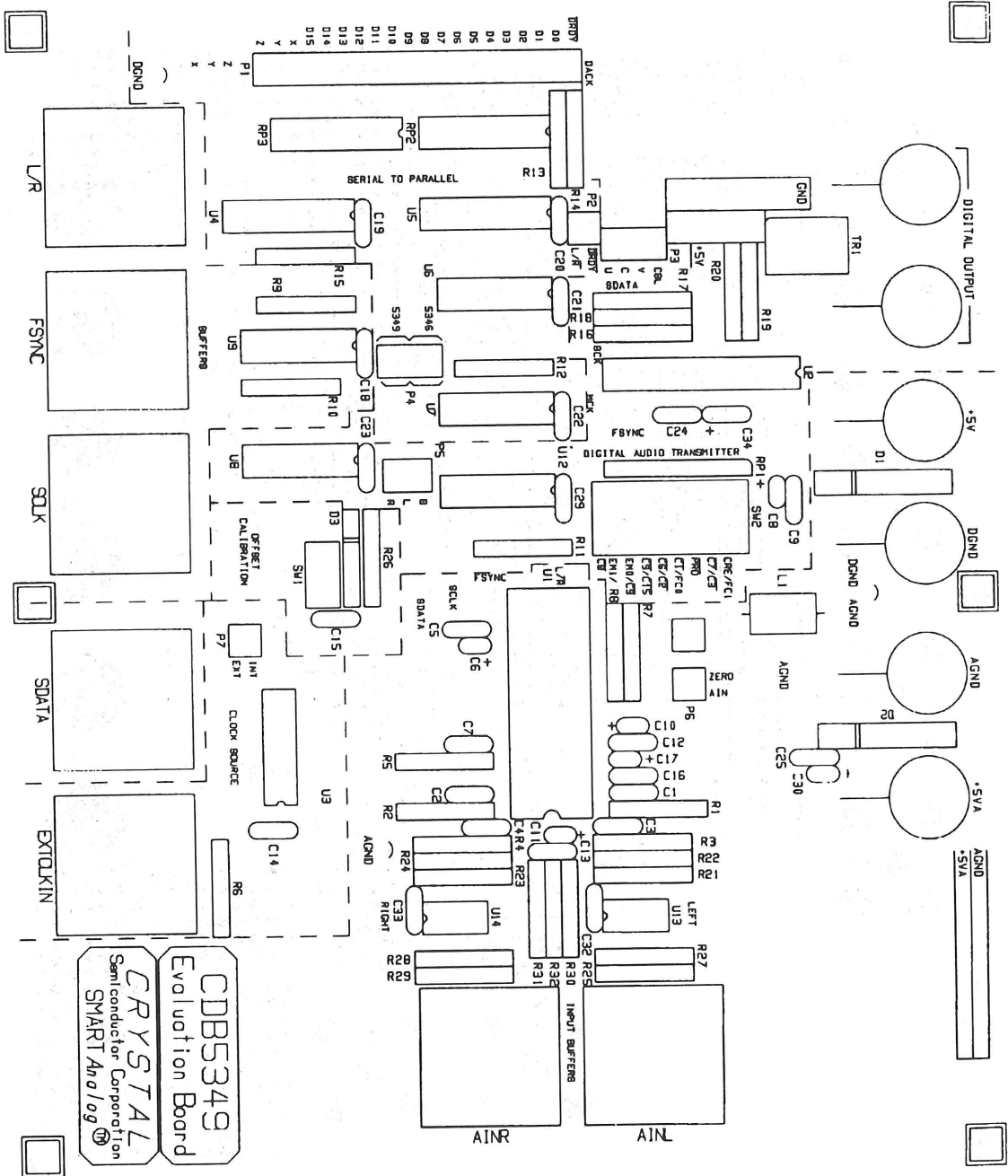


**Top Ground Plane Layer (NOT TO SCALE)**



A:V3R-04E2B39

Bottom Trace Layer (NOT TO SCALE)



Silk Screen Layer (NOT TO SCALE)

# 18-Bit, Stereo A/D Converter for Digital Audio

## Features

- Complete CMOS Stereo A/D System  
Delta-Sigma A/D Converters  
Digital Anti-Alias Filtering  
S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates  
including 32kHz, 44.1 kHz & 48kHz
- 107 dB SNR (A-Weighted)
- Low Noise and Distortion  
100 dB S/(N+D)
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
- Low Power Dissipation: 550 mW  
Power-Down Mode
- Evaluation Board Available

## General Description

The CS5389 is a complete analog-to-digital converter for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5389 uses 5th order, delta-sigma modulation with 64X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5389 has a filter passband of dc to 24kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

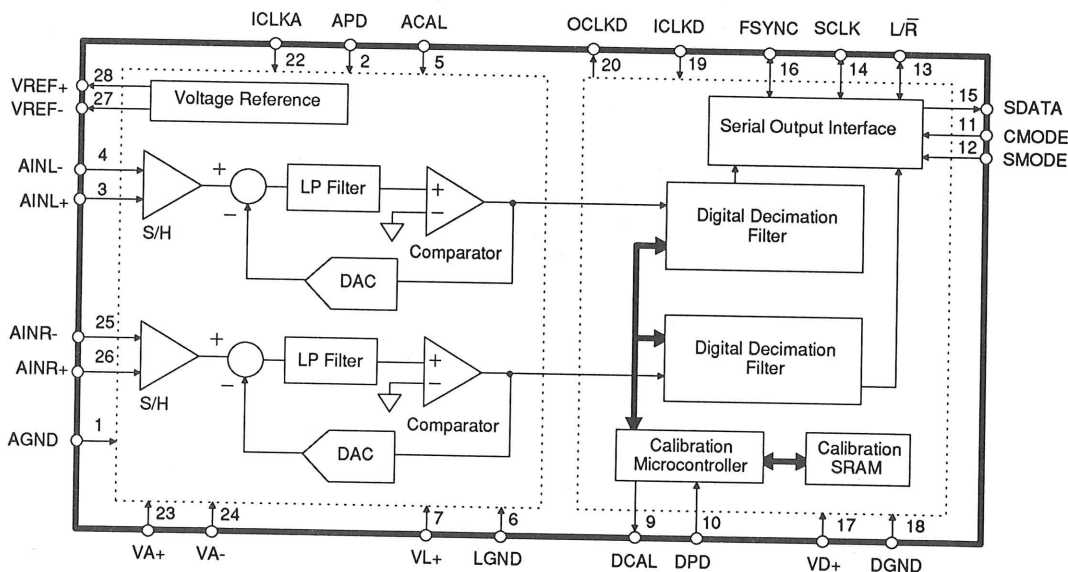
The ADC is housed in a 0.6", 28-pin plastic DIP.

The CS5389 is targeted for the most demanding professional audio systems requiring wide dynamic range and low noise and distortion.

### ORDERING INFORMATION:

Contact Crystal Semiconductor.

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## Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

**Crystal Semiconductor Corporation**  
P.O. Box 17847, Austin, TX 78760  
(512) 445-7222 FAX: (512) 445-7581

APR '92  
DS87PP2  
2-227

• Notes •

## Digital Audio Interface Transmitter

### Features

- Monolithic Digital Audio Interface Transmitter
- Supports: AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 Professional and Consumer Formats
- Host Mode and Stand Alone Modes
- Generates CRC Codes and Parity Bits
- On-Chip RS422 Line Driver
- Configurable Buffer Memory (CS8401A)
- Transparent Mode Allows Direct Connection of CS8402A and CS8412 or CS8401A and CS8411A

### General Description

The CS8401/2A are monolithic CMOS devices which encode and transmit audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8401/2A accept audio and digital data, which is then multiplexed, encoded and driven onto a cable. The audio serial port is double buffered and capable of supporting a wide variety of formats.

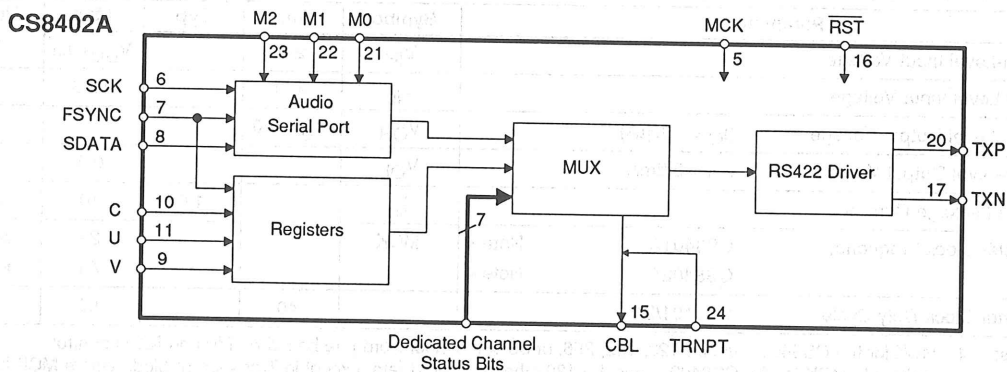
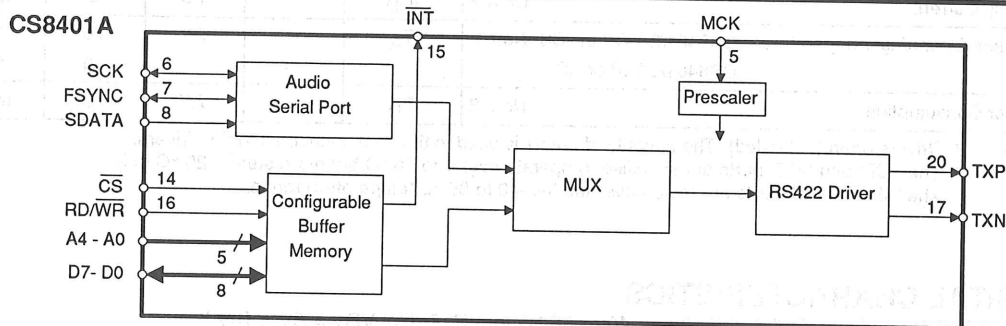
The CS8401A has a configurable internal buffer memory, loaded via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8402A multiplexes the channel, user, and validity data directly from serial input pins with dedicated input pins for the most important channel status bits.

### ORDERING INFORMATION: TABLE OF CONTENTS:

page 2-258  
page 2-259

2



### Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation  
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MAR '92  
DS60PP5  
2-229

**ABSOLUTE MAXIMUM RATINGS** (GND = 0V, all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supply	VD+		6.0	V
Input Current, Any Pin Except Supply	Note 1 $I_{in}$	-	±10	mA
Digital Input Voltage	V <sub>IND</sub>	-0.3	VD+	V
Ambient Operating Temperature (power applied)	T <sub>A</sub>	-55	125	°C
Storage Temperature	T <sub>stg</sub>	-65	150	°C

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS**

(GND = 0V; all voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
DC Voltage	VD+	4.5	5.0	5.5	V
Supply Current	Note 2 I <sub>DD</sub>		1.5	5	mA
Ambient Operating Temperature: CS8401/2A-CP or -CS	Note 3 T <sub>A</sub>	0	25	70	°C
CS8401/2A-IP or -IS		-40		85	°C
Power Consumption	Note 2 P <sub>D</sub>		7.5	25	mW

Notes: 2. Drivers open (unloaded). The majority of power is used in the load connected to the drivers.  
3. The '-CP' and '-CS' parts are specified to operate over 0 to 70 °C but are tested at 25 °C only.  
The '-IP' and '-IS' parts are tested over the full -40 to 85 °C temperature range.

**DIGITAL CHARACTERISTICS**

(T<sub>A</sub> = 25 °C for suffixes 'CP' & 'CS', T<sub>A</sub> = -40 to 85 °C for 'IP' & 'IS'; VD+ = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V <sub>IH</sub>	2.0		V <sub>DD</sub> +0.3	V
Low-Level Input Voltage	V <sub>IL</sub>	-0.3		+0.8	V
High-Level Output Voltage (I <sub>O</sub> = 200µA)	V <sub>OH</sub>	V <sub>DD</sub> -1.0			V
Low-Level Output Voltage (I <sub>O</sub> = 3.2mA)	V <sub>OL</sub>			0.4	V
Input Leakage Current	I <sub>in</sub>		1.0	10	µA
Master Clock Frequency: CS8401A	Note 4 MCK			22	MHz
CS8402A	Note 4			7.1	MHz
Master Clock Duty Cycle	CS8401/2A	40		60	%

Notes: 4. MCK for the CS8401 must be 128, 192, 256, or 384x the input word rate based on M0 and M1 in control register 2. MCK for the CS8402A must be 128x the input word rate, except in Transparent Mode where MCK is 256x the input word rate.

Specifications are subject to change without notice.

### DIGITAL CHARACTERISTICS - RS422 DRIVERS

(TXP, TXN pins only;  $V_{D+} = 5V \pm 10\%$ )

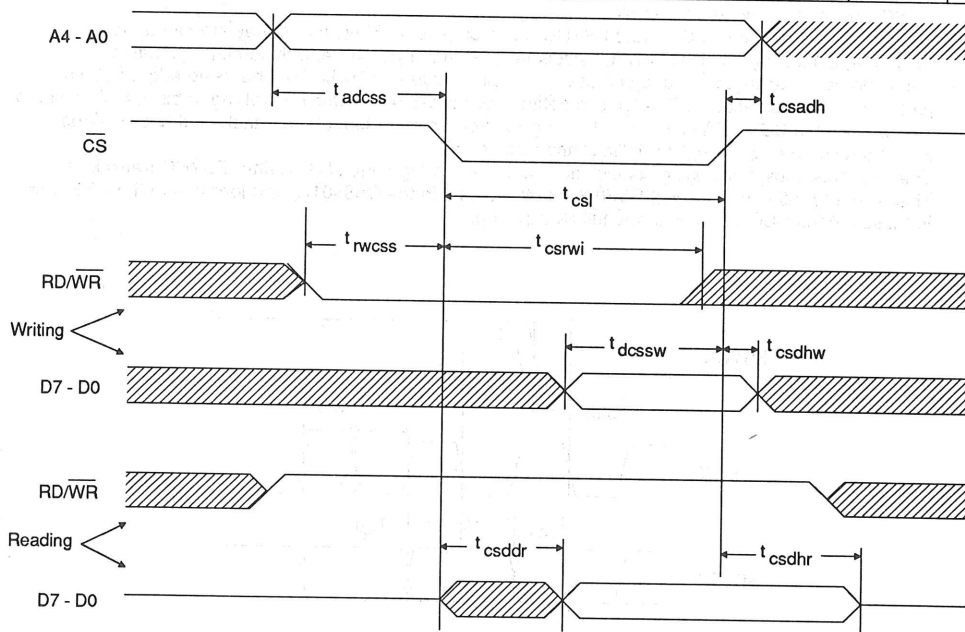
Parameter	Symbol	Min	Typ	Max	Units
Output High Voltage $I_{OH} = -30 \text{ mA}$	$V_{OH}$	$V_{D+} - 0.7$	$V_{D+} - 0.4$		V
Output Low Voltage $I_{OL} = 30 \text{ mA}$	$V_{OL}$		0.4	0.7	V

2

### SWITCHING CHARACTERISTICS - CS8401A PARALLEL PORT

( $T_A = 25^\circ\text{C}$  for suffixes '-CP' and '-CS';  $T_A = -40$  to  $85^\circ\text{C}$  for suffixes '-IP' and '-IS')

Parameter	Symbol	Min	Typ	Max	Units
ADDRESS valid to $\overline{\text{CS}}$ low	$t_{\text{adcss}}$	13.5			ns
$\overline{\text{CS}}$ high to ADDRESS invalid	$t_{\text{csadh}}$	0			ns
RD/ $\overline{\text{WR}}$ valid to $\overline{\text{CS}}$ low	$t_{\text{rwcsw}}$	10			ns
$\overline{\text{CS}}$ low to RD/ $\overline{\text{WR}}$ invalid	$t_{\text{csrwi}}$	35			ns
$\overline{\text{CS}}$ low	$t_{\text{csl}}$	35			ns
DATA valid to $\overline{\text{CS}}$ rising RD/ $\overline{\text{WR}}$ low (writing)	$t_{\text{dcsw}}$	32			ns
$\overline{\text{CS}}$ high to DATA invalid RD/ $\overline{\text{WR}}$ low (writing)	$t_{\text{csdhw}}$	0			ns
$\overline{\text{CS}}$ falling to DATA valid RD/ $\overline{\text{WR}}$ high (reading)	$t_{\text{csddr}}$			35	ns
$\overline{\text{CS}}$ rising to DATA Hi-Z RD/ $\overline{\text{WR}}$ high (reading)	$t_{\text{csdhr}}$	5			ns



CS8401A Parallel Port Timing

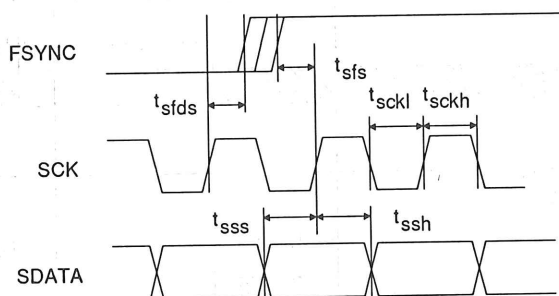


## SWITCHING CHARACTERISTICS - SERIAL PORTS

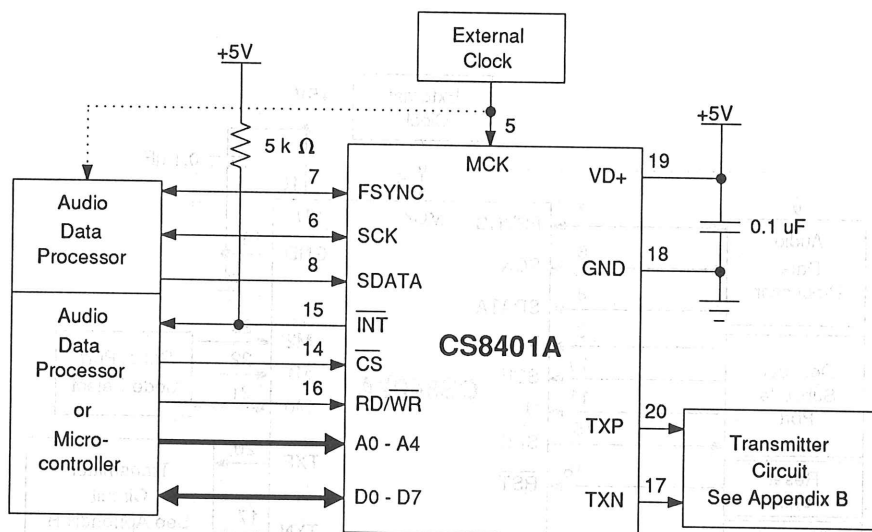
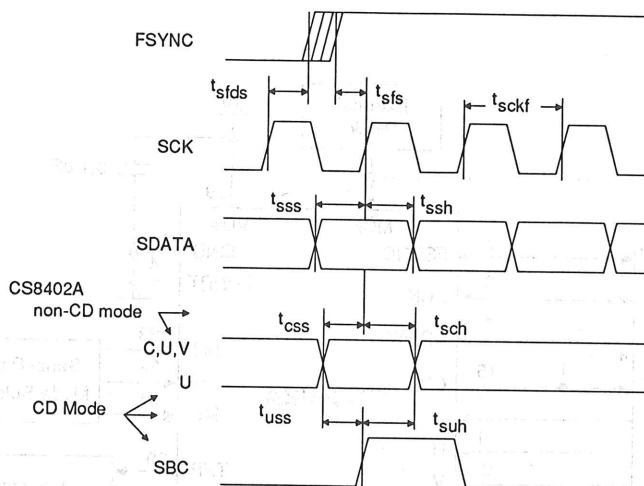
( $T_A = 25\text{ }^{\circ}\text{C}$  for suffixes '-CP' and '-CS';  $T_A = -40$  to  $85\text{ }^{\circ}\text{C}$  for suffixes '-IP' and '-IS';  
Inputs: Logic 0 = GND, logic 1 =  $V_{DD}$ ;  $C_L = 20\text{ pF}$ )

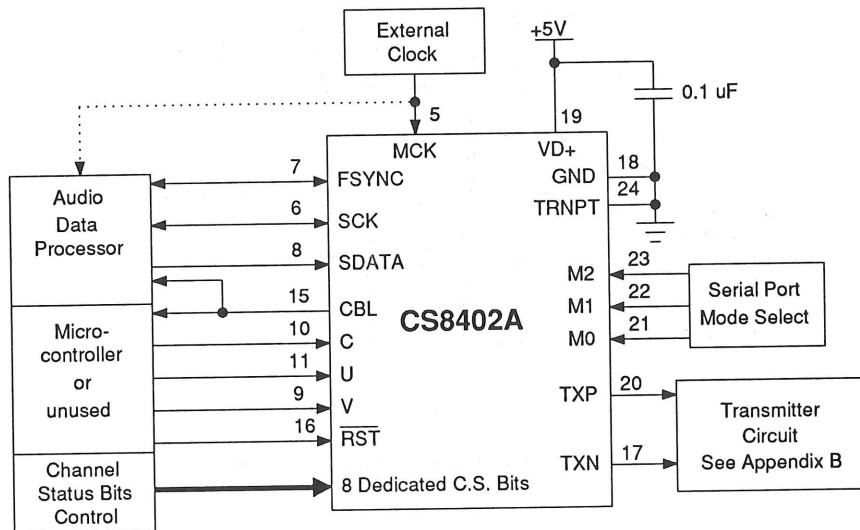
Parameter		Symbol	Min	Typ	Max	Units
SCK Frequency	Master Mode Notes 5,6 Slave Mode Note 6	$t_{sckf}$		IWRx64	12.5	Hz MHz
SCK Pulse Width Low	Slave Mode Note 6	$t_{sckl}$	25			ns
SCK Pulse Width High	Slave Mode Note 6	$t_{sckh}$	25			ns
SCK rising to FSYNC edge delay	Notes 6,7	$t_{sfds}$	20			ns
SCK rising to FSYNC edge setup	Notes 6,7	$t_{sfs}$	20			ns
SDATA valid to SCK rising setup	Note 7	$t_{sss}$	20			ns
SCK rising to SDATA hold time	Note 7	$t_{ssh}$	20			ns
C, U, V valid to SCK rising setup	CS8402A non-CD Mode Notes, 7,8	$t_{css}$	0			ns
SCK rising to C, U, V hold time	CS8402A non-CD mode Notes 7, 8	$t_{scs}$	50			ns
U valid to SBC rising setup	CS8402A, CD mode Note 8	$t_{uss}$	0			ns
SBC rising to U hold time	CS8402A, CD mode Note 8	$t_{suh}$	80			ns
RST Pulse Width	CS8402A		150			ns

- Notes:
5. The input word rate, IWR, refers to the frequency at which stereo audio input samples are input to the part. (A stereo pair is two audio samples.) Therefore, in Master mode, there are always 32 SCK periods in one audio sample.
  6. Master mode is defined as SCK and FSYNC being outputs. In Slave mode they are inputs. In the CS8401A, control reg. 3 bit 1, MSTR, selects master. In the CS8402A, only format 0 is master.
  7. The table above assumes data is output on the falling edge and latched on the rising edge. In both parts the edge is selectable. The table is defined for the CS8401A with control reg. 3 bit 0, SCED, set to one, and for the CS8402A in formats 4 through 7. For the other formats, the table and figure edges must be reversed (ie. "rising" to "falling" and vice versa).
  8. The diagrams show SBC rising coincident with the first rising edge of SCK after FSYNC transitions. This is true for all modes except FSF0 & 1 both equal 1 in the CS8401A, and format 4 in the CS8402A. In these modes SBC is delayed one full SCK period.

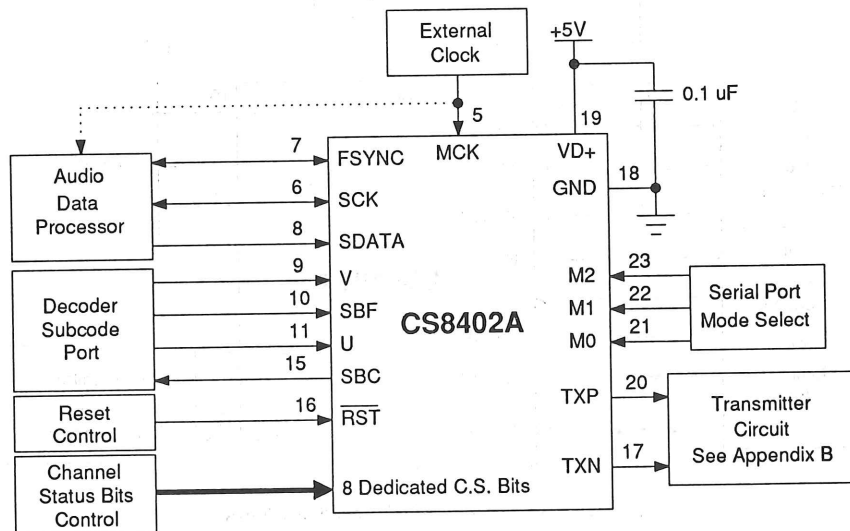


Serial Input Timing - Slave Mode





**Figure 2. CS8402A Professional & Consumer Modes Typical Connection Diagram**



**Figure 3. Consumer CD Submode Typical Connection Diagram**

## GENERAL DESCRIPTION

The CS8401A/2A are monolithic CMOS circuits that encode and transmit audio and digital data according to the AES/EBU, IEC 958, S/PDIF, and EIAJ CP-340 interface standards. Both chips accept audio and control data separately; multiplex and biphasemark encode the data internally; and drive it, directly or through a transformer, to a transmission line. The CS8401A is fully software programmable through a parallel port and contains buffer memory for control data, while the CS8402A has dedicated pins for the most important control bits and a serial input port for the C, U, and V bits.

Familiarity with the AES/EBU and IEC 958 specifications are assumed throughout this data sheet. Many terms such as channel status, user data, auxiliary data, professional mode, etc. are not defined. The Application Note, Overview of AES/EBU Digital Audio Interface Data Structures, provides an overview of the AES/EBU and IEC 958 specifications and is included for clarity; however, it is not meant to be a complete reference, and the complete standards should be obtained from the Audio Engineering Society or ANSI for the AES/EBU document, and the International Electrotechnical Commission for the IEC document.

### Line Drivers

The RS422 line drivers for both the CS8401A and CS8402A are low skew, low impedance, differential outputs capable of driving 110  $\Omega$  transmission lines with a 4 volt peak-to-peak signal when configured as shown in Appendix A. To prevent possible short circuits, both drivers are set to ground when no master clock (MCK) is provided. They can also be disabled by resetting the device ( $\overline{\text{RST}}$  = low). Appendix A contains more information on the line drivers. A 0.1  $\mu\text{F}$  capacitor, with short leads, should be placed as close as possible to the VD+ and GND pins.

## CS8401A DESCRIPTION

The CS8401A accepts 16- to 24-bit audio samples through a configurable serial port, and channel status, user, and auxiliary data through an 8-bit parallel port. The parallel port allows access to 32 bytes of internal memory which is used to store control information and buffer channel status, user, and auxiliary data. This data is multiplexed with the audio data from the serial port, the parity bit is generated, and the bit stream is biphasemark encoded and driven through an RS422 line driver. A block diagram of the CS8401A is shown in Figure 4. In accordance with the professional definition of channel status, the CRCC code (C.S. byte 23) can be internally generated.

### Parallel Port

The parallel port accesses one status register, three control registers, and 28 bytes of dual port buffer memory. The address bus, and  $\text{RD}/\overline{\text{WR}}$  line must be valid when  $\overline{\text{CS}}$  goes low. If  $\text{RD}/\overline{\text{WR}}$  is low, the value on the data bus will be written into the buffer memory at the specified address. If  $\text{RD}/\overline{\text{WR}}$  is high, the value in the buffer memory, at the specified address, is placed on the data bus. The detailed timing for reading and writing the CS8401A can be found in the Digital Switching Characteristics table. The memory space is allocated as shown in Figure 5. There are three defined buffer memory modes selectable by two bits in control register 2.

### Status and Control Registers

Upon power up the CS8401A control registers contain all zeros. Therefore, the part is initially in reset and is muted. One's must be written to control register 2, bits  $\overline{\text{RST}}$  and  $\overline{\text{MUTE}}$ , before the part will transmit data. *The remaining registers are not initialized on power-up and may contain random data.*

The first register, shown in Figure 6, is the status register in which only three bits are valid. The lower three bits contain flags indicating the position of the transmit pointer in the buffer memory. These flags

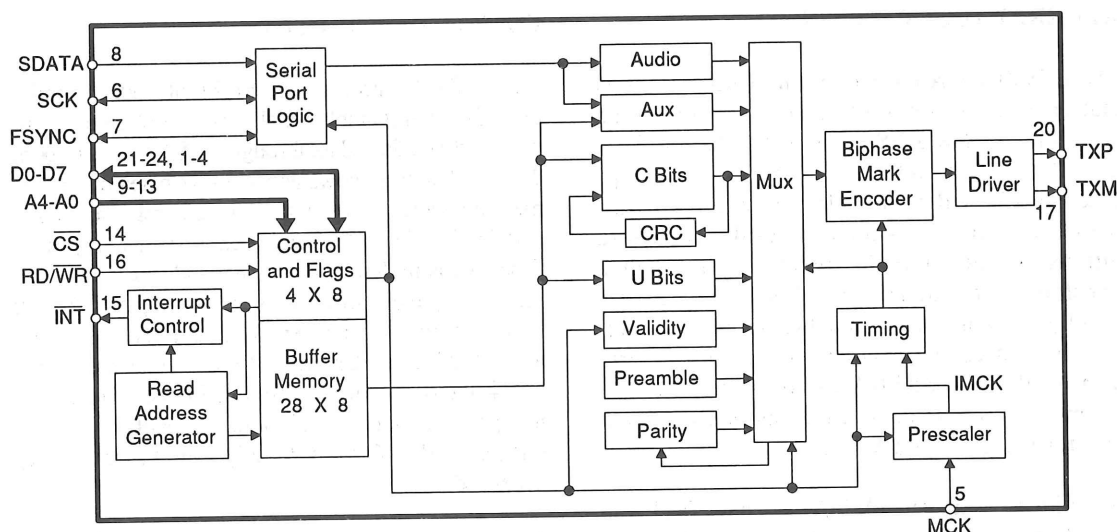


Figure 4. CS8401A Block Diagram

may be used to avoid contention between the transmit pointer reading the data and the user updating the buffer memory. Besides indicating the byte location being transmitted, the flags indicate the block of memory the part is currently addressing, thereby telling the user which block is free to be written to. Each flag has a corresponding mask bit (control register 1) which, when set, allows a transition on the flag to generate a pulse on the interrupt pin. Flag 0 and flag 1 cause interrupts on both edges whereas flag 2 causes an interrupt only on the rising edge. Timing and further explanation of the flags can be found in the buffer memory section.

The two most significant bits of control register 1, BKST and TRNPT, are used for Transparent Mode operation of the CS8401A. Transparent Mode is used for those applications where it is useful to maintain frame alignment between the received and transmitted audio data signals. In Transparent Mode (TRNPT = "1") the MCK, FSYNC, SCK and SDATA inputs of the CS8401A can be connected to their corresponding outputs of the CS8411. In Transparent Mode, FSYNC synchronizes the transmitter and the receiver. The data delay through the

CS8401A is set so that three frame delays occur from the input of the CS8411 to the output of the CS8401A. In Transparent Mode, 32 SCK's are required per subframe.

Channel status block alignment between the CS8411 and the CS8401A is accomplished by setting BKST high at the occurrence of the Flag 2 rising edge of the CS8411. If FSYNC is a left/right signal, BKST is sampled once per frame; if FSYNC is a word clock, BKST is sampled once per subframe. A low to high transition of BKST (based on two successive internal samples) resets the channel status block boundary to the beginning.

Control register 2, shown in Figure 8, contains various system level functions. The two most significant bits, M1 and M0, select the frequency at the MCK pin as shown in Table 1. As an example, if the audio sample frequency is 44.1 kHz and M0 and M1 are both zero, MCK would then be 128x the audio sample rate or 5.6448 MHz. The next bit (5) in control register 2, V, indicates the validity of the current audio sample. According to the digital audio specifications, V = 0 signifies the audio

signal is suitable for conversion to analog. B1 and B0 select one of three modes for the buffer memory. The different modes are shown in Figure 5 and the bit combinations in Table 2. More information on the different modes can be found in the *Buffer Memory* section. Bit 2, CRCE, is the channel status CRCC enable and should only be used in professional mode. When CRCE is high, the channel status data cyclic redundancy check

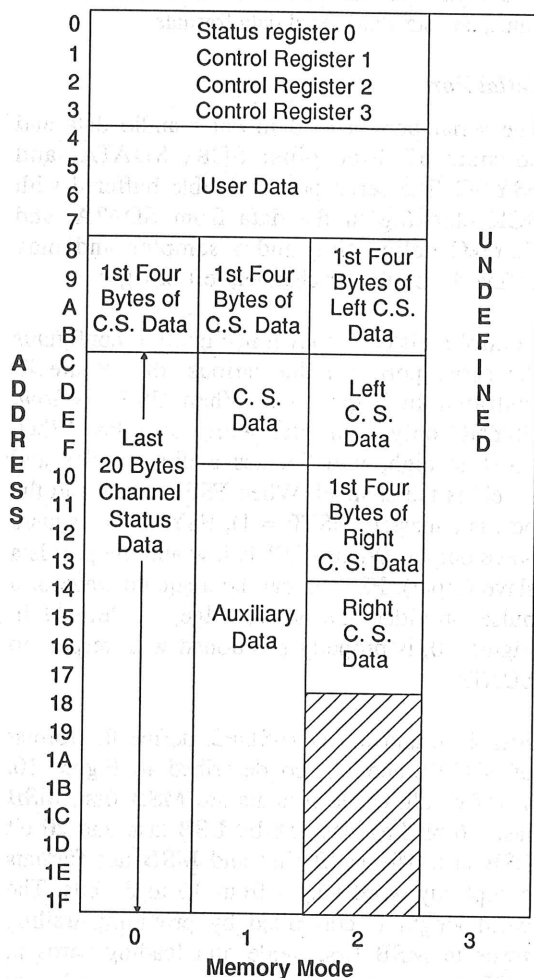


Figure 5. CS8401A Buffer Memory Modes



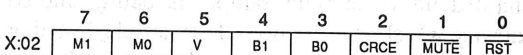
FLAG2: High for first four bytes of channel status  
FLAG1: Memory mode dependent - See figure 11  
FLAG0: High for last two bytes of user data.

Figure 6. Status Register



BKST: Causes realignment of data block when set to "1".  
TRNPT: Selects Transparent Mode appropriately setting data delay through device  
MASK2: Interrupt mask for FLAG2. A "1" enables the interrupt.  
MASK1: Interrupt mask for FLAG1.  
MASK0: Interrupt mask for FLAG0.

Figure 7. Control Register 1



M1: with M0, selects MCK frequency.  
M0: with M1, selects MCK frequency.  
V: Validity bit of current sample.  
B1: with B0, selects the buffer memory mode.  
B0: with B1, selects the buffer memory mode.  
CRCE: Channel status CRC Enable. Professional mode only.  
MUTE: When clear, transmitted audio data is set to zero.  
RST: When clear, drivers are disabled, frame counters cleared.

Figure 8. Control Register 2

M1	M0	MCLK
0	0	128x Input Word Rate
0	1	192x Input Word Rate
1	0	256x Input Word Rate
1	1	384x Input Word Rate

Table 1. MCLK Frequencies

B1	B0	Mode	Buffer Memory Contents
0	0	0	Channel Status
0	1	1	Auxiliary Data
1	0	2	Independent Channel Status
1	1	3	Reserved

Table 2. Buffer Memory Modes

characters are generated independently for channels A and B and are transmitted at the end of the channel status block. When  $\overline{\text{MUTE}}$  (bit 1) is low, the transmitted audio data is forced to zero. Both  $\overline{\text{RST}}$  and  $\overline{\text{MUTE}}$  are set to zero upon power up.

When  $\overline{\text{RST}}$  is low, the differential line drivers are set to ground and the block counters are reset to the beginning of the first block. In order to properly synchronize the rest of the CS8401A to the audio serial port, the transmit timing counters, which include the flags in the status register, are not enabled after  $\overline{\text{RST}}$  is set high until eight and one half SCK periods after the active edge (first edge after reset is exited) of FSYNC.

When FSYNC is configured as a left/right signal (FSF1 = 1), the counters and flags are not enabled until the right sample is being entered (during which the previous left sample is being transmitted). This guarantees that channel A is left and Channel B is right as per the digital audio interface specs.

Control register 3 contains format information for the serial audio input channel. The MSB is unused and the next three bits, SDF2-SDF0, select the format for the serial input data with respect to FSYNC. There are five valid combinations of these bits as shown in Figure 10. The next two bits, FSF1 and FSF0, select the format of FSYNC. Two of the formats delineate each channel's data and do

not indicate the particular channel. The other two formats also indicate the specific channel. The formats are shown in Figure 10. Bit 1, MSTR, determines whether FSYNC and SCK are inputs, MSTR low, or outputs, MSTR high. Bit 0, serial clock edge select, SCED, selects the edge that audio data gets latched on. When SCED is low, the falling edge of SCK latches data in the chip and when SCED is high, the rising edge is used.

The multitude of combinations allow for a zero glue logic interface to almost all DSP's, encoder chips, and standard serial data formats.

### Serial Port

The serial port is used to enter audio data and consists of three pins: SCK, SDATA, and FSYNC. The serial port is double buffered with SCK clocking in the data from SDATA, and FSYNC delineating audio samples and may define the particular channel, left or right.

Control register 3, shown in Figure 9, configures the serial port. All the various formats are illustrated in Figure 10. When FSF1 is low, FSYNC only delineates audio samples. When FSF1 is high, it delineates audio samples and specifies the channel. When FSF1 is low and the port is a master (MSTR = 1), FSYNC is a square wave output. When FSF1 is low and the port is a slave (input), FSYNC can be a square wave or a pulse provided the active edge, as defined in Figure 10, is properly positioned with respect to SDATA.

Bits 4, 5, and 6, SDF0-SDF2, define the format of SDATA and is also described in Figure 10. The five allowable formats are MSB first, MSB last, 16-bit LSB last, 18-bit LSB last, and 20-bit LSB last. The MSB first and MSB last formats accept any word length from 16 to 24 bits. The word length is controlled by providing trailing zeros in MSB first mode and leading zeros in MSB last mode, or by restricting the number of SCK periods between samples to the sample

	7	6	5	4	3	2	1	0
X:03		SDF2	SDF1	SDF0	FSF1	FSF0	MSTR	SCED

SDF2: with SDF0 & SDF1, select serial data format.  
 SDF1: with SDF0 & SDF2, select serial data format.  
 SDF0: with SDF1 & SDF2, select serial data format.  
 FSF1: with FSF0, select FSYNC format.  
 FSF0: with FSF1, select FSYNC format.  
 MSTR: When set, SCK and FSYNC are outputs.  
 SCED: When set, rising edge of SCK latches data.  
 When clear, falling edge of SCK latches data.

Figure 9. Control Register 3



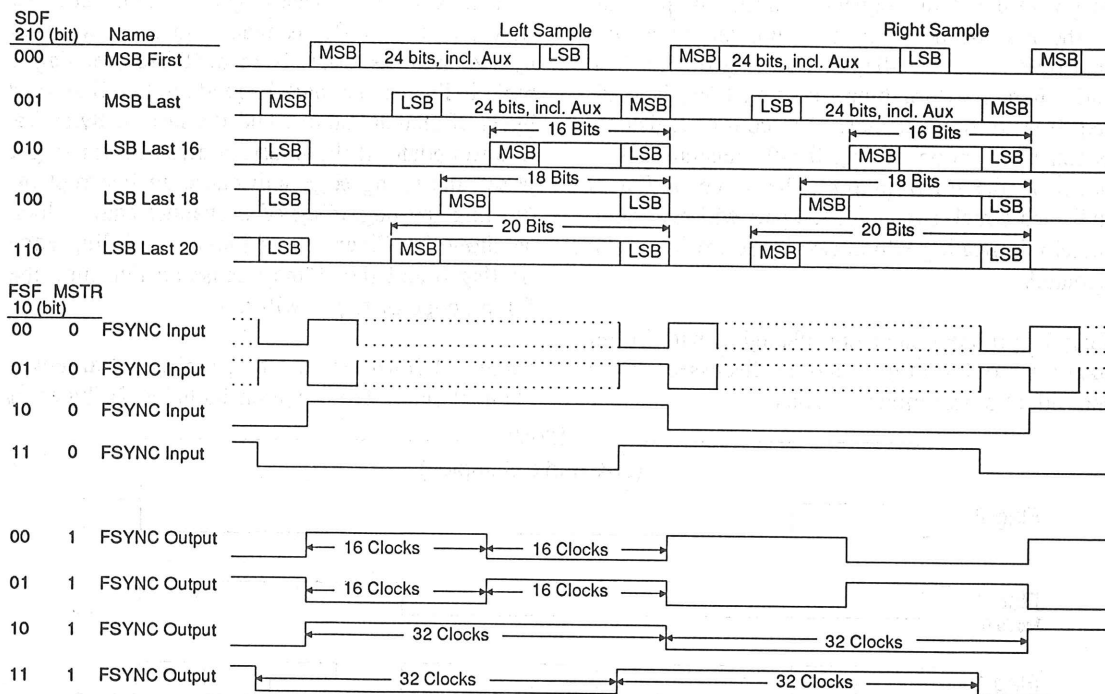


Figure 10. CS8401A Serial Port SDATA and FSYNC Timing

word length. The 16-, 18-, and 20-bit LSB-last modes require at least 16, 18, or 20 SCK periods per sample respectively. As a master, 32 SCK periods are output per sample.

FSYNC must be derived from MCK via a DSP using the same clock or by external counters. If FSYNC moves (jitters) with respect to MCK by more than 4 MCK periods, the CS8401A may reset the channel status block and flags. Appendix C contains more information on the relationship of FSYNC and MCK.

### Buffer Memory

In all buffer modes, the status register and control registers are located at addresses 0-3 respectively, and the user data is buffered in locations 4-7. The parallel port can access any

location in the user data buffer at any time; however, care must be taken not to modify a location when that location is being read internally. This internal reading is done through the second port of the buffer and is done in a cyclic manner.

Reset initializes the internal pointer to 04H (Hex). Data is read from this location and stored in an 8-bit shift register which is shifted once per audio sample. (An audio sample is defined as a single channel, not a stereo pair.) The byte is transmitted LSB first, D0 being the first bit. After transmitting 8 samples, i.e. 8 user bits, the address pointer is incremented and the next byte of user data is loaded into the shift register. After transmitting all four bytes, 32 audio samples, the user read pointer is reset to 04H (Hex) and the cycle repeats.

Flag 0 in the status register monitors the position of the internal user data read pointer. When the first byte, location 04H, is read, flag 0 is set low and when the third byte, location 06H, is read, flag 0 is set high. If mask 0 in control register 1 is set, a transition of flag 0 will generate a low pulse on the interrupt pin. The value of flag 0 indicates which two bytes the part will read next, thereby indicating which two bytes are free to be updated.

Flag 1 is mode dependent, changing with buffer memory configuration, and is discussed in the individual buffer mode sections.

Flag 2 is set high when byte 0 of the channel status, address 08H, is read, and set low when byte 4, address 0BH, is read. Therefore, flag 2 high indicates the part is reading the first four bytes of channel status, and the last 20 bytes are free to update. If the interrupt mask bit for flag 2 is set, the rising edge will cause an interrupt indicating the beginning of a channel status block as shown in Figure 11. Although a falling edge on flag 0 and flag 1 may cause an interrupt, the falling edge of flag 2 will not.

Figure 11 illustrates the flag timing for an entire channel status block which includes 24 bytes of

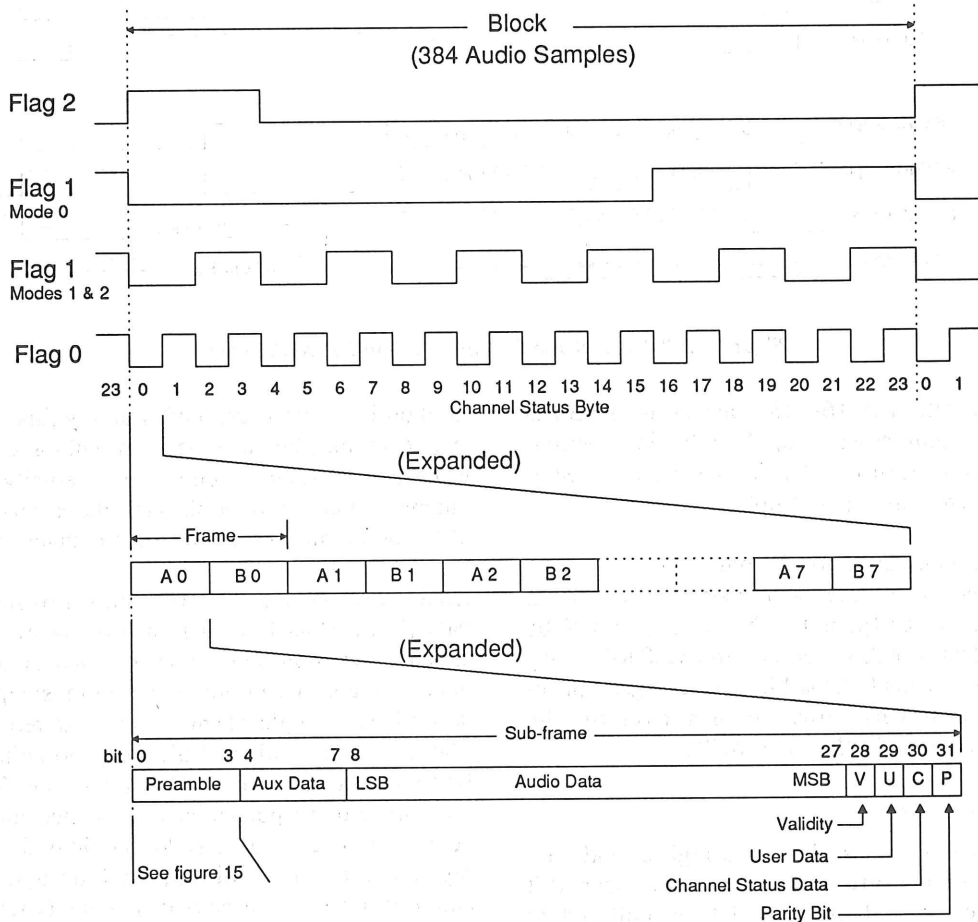


Figure 11. CS8401A Status Register Flag Timing

channel status data and 384 audio samples. (This figure assumes the channel status bit is the same for the audio pair.) The lower portion of Figure 11 expands the first byte of channel status showing eight pairs of data with a pair defined as a frame. This is further expanded showing the first sub-frame (A0) to contain 32 bits as per the AES/EBU specifications (see Appendix A). When transmitting stereo, channel A is left and channel B is right. The preamble at the bottom of Figure 11 is expanded in Figure 15 to show the exact timing between flags, the interrupt pin, and internal buffer-read timing.

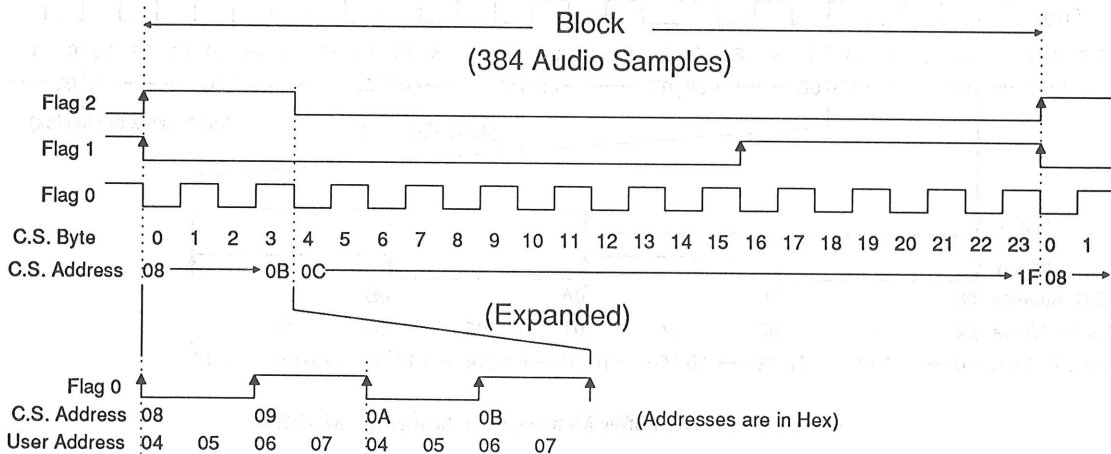
## Buffer Mode 0

In buffer mode 0, in addition to the user-data buffer previously discussed, one entire block of channel status data is buffered in 24 memory locations from address 08H to 1FH. This block will be transmitted in both channel A and channel B, one bit per frame. Like the user-data buffer, the parallel port can access any location in this buffer at any time. The transmitter section reads this buffer in a cyclic non-destructive manner and stores the byte in an 8-bit shift register that is shifted once per two transmitted audio samples (once per frame).

Flag 1 in the status register can be used to monitor the channel status buffer. In mode 0, flag 1 is set low when byte 0, location 08H, is read, and set high when byte 16, location 18H, is read. If mask 1 in control register 1 is set, a transition on flag 1 will generate a pulse on the interrupt pin. Figure 12 illustrates the memory read sequence for buffer mode 0 along with the flag timing. The arrows on the flags indicate an interrupt if the appropriate mask bit is set. Flag 0 can cause an interrupt on either edge, which is shown only in the expanded portion of the Figure for clarity. The expanded section also shows that the user buffer is reread when location 0AH of the channel status is read.

## Buffer Mode 1

In buffer mode 1, eight bytes are allocated for channel status data and 16 bytes for auxiliary data as shown in Figure 5. The channel status buffer, locations 08H to 0FH, is divided into two sections. The first four locations always contain the first four bytes of channel status, identical to mode 0, and are read once per channel status block. The second four locations, addresses 0CH to 0FH, provide a cyclic buffer for the last 20 bytes of channel status data.



Similar to mode 0, transmitted channel status data will be the same for channel A and channel B (one channel status bit per frame). Flag 1 and flag 2 can be used to monitor this buffer. Flag 1 is set low when byte 0 of channel status data, location 08H, is read and is toggled when every other byte is read. As shown in Figure 13, flag 2 is set high when byte 0, location 08H, is read and set low when byte 4, location 0CH, is read. Flag 2 determines whether the channel status pointer is reading the first four-byte section or the second four-byte section, while flag 1 indicates which two bytes of the section are free to update.

The auxiliary data buffer, locations 10H to 1FH, is read in a cyclic manner similar to the data buffer; however, four auxiliary data bits are transmitted per audio sample (sub-frame). Since the auxiliary buffer must be read four times as often as the user data buffer and is four times as large, flag 0 can be used to monitor both.

### Buffer Mode 2

In buffer mode 2, two 8-byte buffers are available for buffering both channel A and channel B channel status data independently. Both buffers are identical to the channel status buffer in mode 1 except that each channel can have unique channel status data. The two buffers are read simultaneously with locations 08H to 0FH transmitted in channel A and locations 10H to 17H transmitted in channel B. Figure 5 contains the buffer memory modes and Figure 14 illustrates the buffer read sequence for mode 2.

### Buffer-Read and Interrupt Timing

As mentioned previously in the buffer mode sections, conflicts between externally writing to the buffer ram and the CS8401A internally reading bytes of ram for transmission may be averted by using the flag levels to avoid the section currently being addressed by the part. Interrupts occur at flag edges indicating the exact byte that the

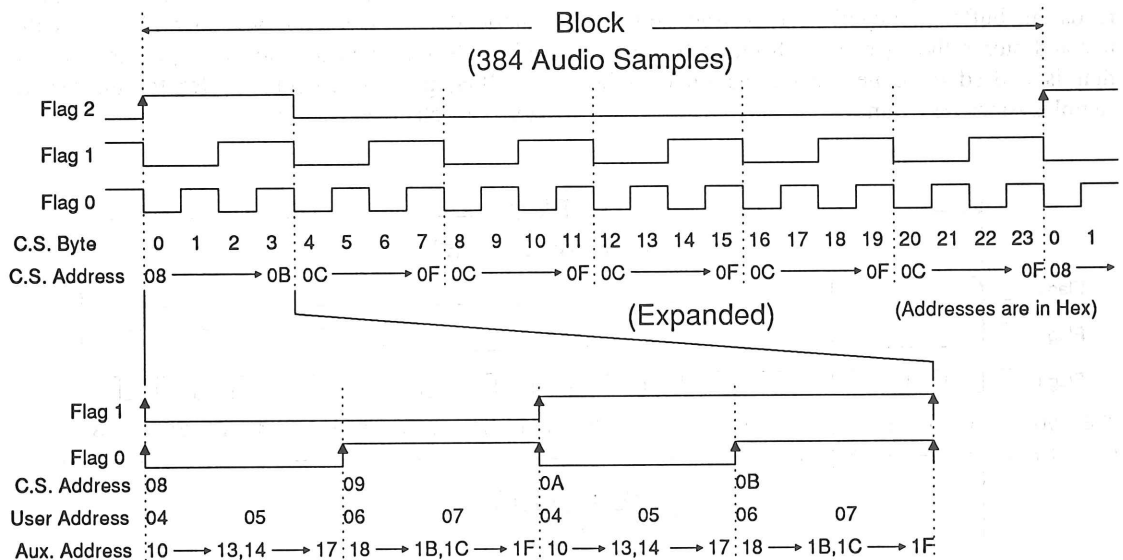


Figure 13. CS8401A Buffer Memory Read Sequence - MODE 1

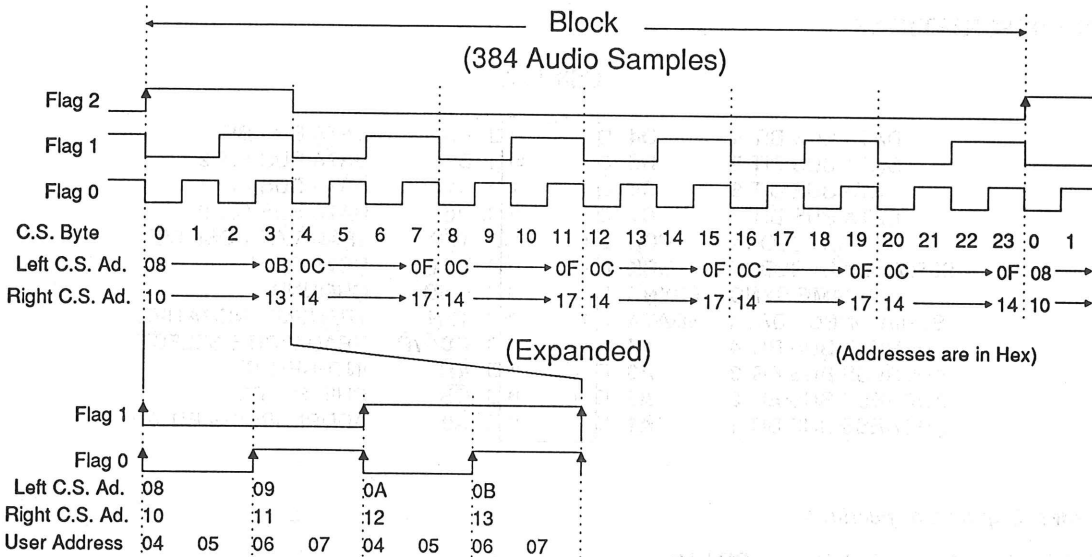


Figure 14. CS8401A Buffer Memory Read Sequence - MODE 2

part is currently reading. Utilizing  $\overline{\text{INT}}$  along with the flags, the byte currently being read by the part can be avoided allowing access to all other bytes instead of just a section. Figure 15 illustrates the timing between flags,  $\overline{\text{INT}}$ , and the internal reading of the buffer for transmission. The master clock IMCK is shown as  $128 \times F_s$ . Other MCK frequencies are initially divided to obtain  $128 \times F_s$ , defined as IMCK (internal MCK), which is then used for all internal timing, so the timing in Figure 15 is valid for all MCK frequencies. When the parity bit (P) is transmitted, a transition on a flag causes  $\overline{\text{INT}}$  to go low if the

appropriate mask bit is set. Concurrently, the part starts reading from the internal buffer. Writing to the buffer ram location being read by the part should be avoided while the internal "ram read" signal is high.

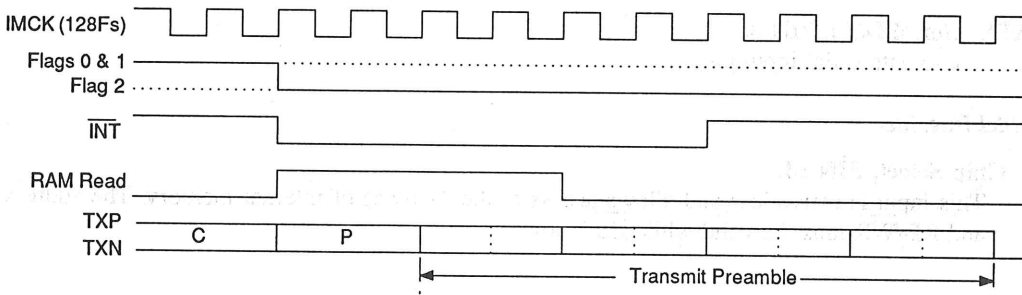
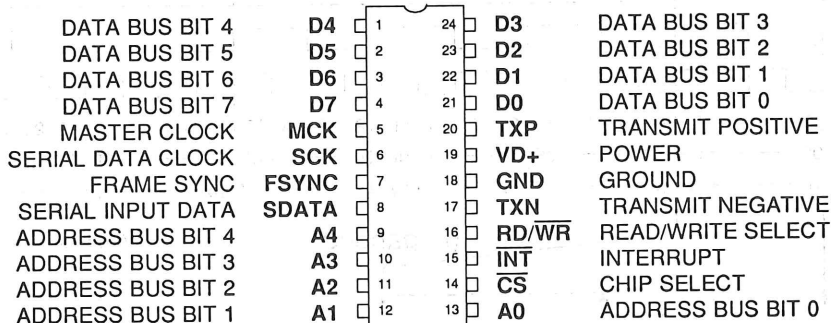


Figure 15. RAM/Buffer-Read and Interrupt Timing

## PIN DESCRIPTIONS

**CS8401A**



### Power Supply Connections

#### VD+ - Positive Digital Power, PIN 19.

Positive supply for the digital section. Nominally +5 volts.

#### GND - Ground, PIN 18.

Ground for the digital section.

### Audio Input Interface

#### SCK - Serial Clock, PIN 6.

Serial clock for SDATA pin which can be configured (via control register 3) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will contain 32 clocks for every audio sample. As an input, it does not need to be continuous and can be up to 15 MHz.

#### FSYNC - Frame Sync, PIN 7.

Delineates the serial data and may indicate the particular channel, left or right. Also, FSYNC may be configured as an input or output. The format is based on bits in control register 3.

#### SDATA - Serial Data, PIN 8.

Audio data serial input pin.

### Parallel Interface

#### CS - Chip Select, PIN 14.

This input is active low and allows access to the 32 bytes of internal memory. The address bus and RD/WR must be valid while CS is low.

#### **RD/WR - Read/Write, PIN 16.**

If RD/WR is low when CS goes active (low), the data on the data bus is written to internal memory. If RD/WR is high when CS goes active, the data in the internal memory is placed on the data bus.

#### **A4-A0 - Address Bus, PINS 9-13.**

Parallel port address bus that selects the internal memory location to be read from or written to.

#### **D0-D7 - Data Bus, PINS 21-24, 1-4.**

Parallel port data bus used to check status, write control words, or write internal buffer memory.

#### **INT - Interrupt, PIN 15.**

Open drain output that can signal the state of the internal buffer memory. A 5kΩ resistor to VD+ is typically used to support logic gates. All bits affecting INT are maskable allowing total control over the interrupt mechanism.

#### **Transmitter Interface**

#### **MCK - Master Clock, PIN 5.**

Clock input which defines the transmit timing. It can be configured, via control register 2, for 128, 192, 256, or 384 times the sample rate.

#### **TXP, TXN - Differential Line Drivers, PINS 20, 17.**

RS422 compatible line drivers.



## CS8402A DESCRIPTION

The CS8402A accepts 16- to 24-bit audio samples through a serial port configured in one of seven formats; provides several pins dedicated to particular channel status bits; and allows all channel status, user, and validity bits to be serially input through port pins. This data is multiplexed, the parity bit is generated, and the bit stream is biphase-mark encoded and driven through an RS422 line driver.

The CS8402A operates as a professional or consumer interface transmitter selectable by pin 2, PRO. As a professional interface device, the dedicated channel status input pins are defined according to the professional standard, and the CRC code (C.S. byte 23) can be internally generated.

As a consumer device, the dedicated channel status input pins are defined according to the consumer standard. A submode provided under the consumer mode is compact disk, CD, mode. When transmitting data from a compact disk, the CD subcode port can accept CD subcode data, extract channel status information from it, and transmit it as user data.

The master clock, MCK, controls timing for the entire chip and must be 128×Fs. As an example, if stereo data is input to the CS8402A at 44.1 kHz, MCK input must be 128 times that or 5.6448 MHz.

### Audio Serial Port

The audio serial port is used to enter audio data and consist of three pins: SCK, SDATA, and FSYNC. SCK clocks in SDATA, which is double buffered, while FSYNC delineates the audio samples and may indicate the particular channel, left or right. To support many different interfaces, M2, M1, and M0 select one of seven different formats for the serial port. The coding is shown in Table 3 while the formats are shown in Figure 16. Format 0 and 1 are designed to interface with Crystal ADCs. Format 2 communicates with Motorola and TI DSPs. Format 3 is reserved. For-

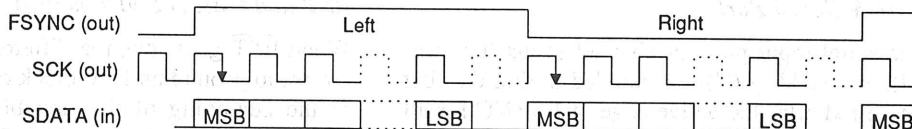
mat 4 is compatible with the I<sup>2</sup>S standard. Formats 5 and 6 make the CS8402A look similar to existing 16- and 18-bit DACs, and interpolation filters. Format 7 is an MSB-last format and is conducive to serial arithmetic. SCK and FSYNC are outputs in Format 0 and inputs in all other formats. In Format 2, the rising edge of FSYNC delineates samples and the falling edge must occur a minimum of one bit period before or after the rising edge. In all formats except 2, FSYNC contains left/right information requiring both edges of FSYNC to delineate samples. Formats 5 and 6 require a minimum of 16- or 18-bit audio words respectively. In all formats other than 5 and 6, the CS8402A can accept any word length from 16 to 24 bits by adding leading zeros in format 7 and trailing zeros in the other formats, or by restricting the number of SCK periods between active edges of FSYNC to the sample word length.

FSYNC must be derived from MCK, either thru a DSP using the same clock, or using counters. If FSYNC moves (jitters) with respect to MCK by four MCK periods, the internal counters and CBL may be reset. Appendix B contains more information on the relationship between FSYNC and MCK.

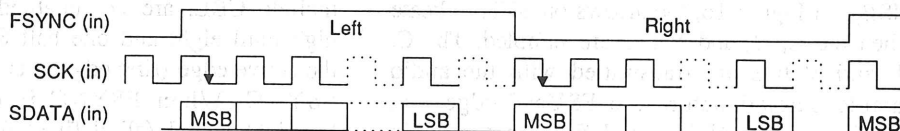
M2	M1	M0	Format
0	0	0	0 - FSYNC & SCK Output
0	0	1	1 - Left/Right, 16-24 Bits
0	1	0	2 - Word Sync, 16-24 Bits
0	1	1	3 - Reserved
1	0	0	4 - Left/Right, I <sup>2</sup> S Compatible
1	0	1	5 - LSB Justified, 16 Bits
1	1	0	6 - LSB Justified, 18 Bits
1	1	1	7 - MSB Last, 16-24 Bits

**Table 3. CS8402A Audio Port Modes**

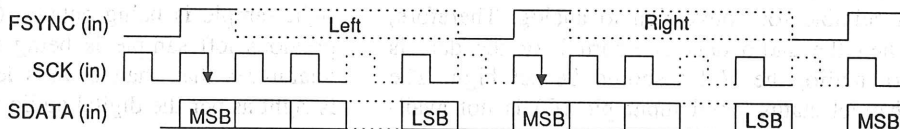
**FORMAT 0:**



**FORMAT 1:**



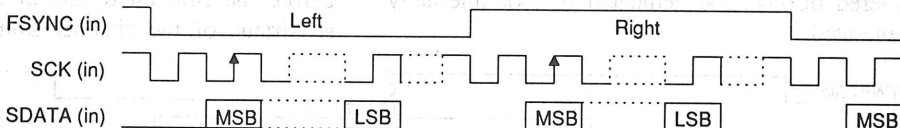
**FORMAT 2:**



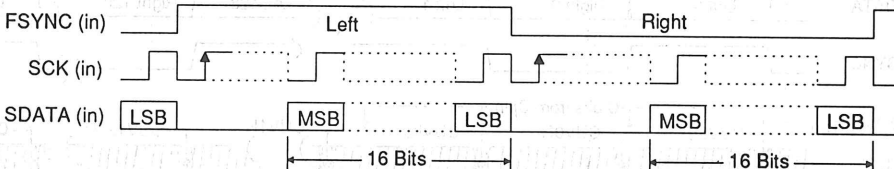
**FORMAT 3:**

(RESERVED)

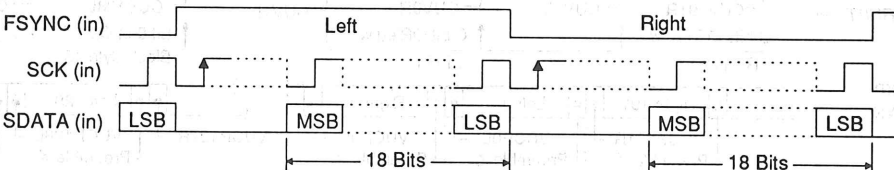
**FORMAT 4:**



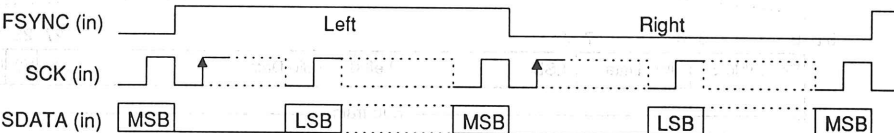
**FORMAT 5:**



**FORMAT 6:**



**FORMAT 7:**



Arrows indicate where C, U, and V bits are latched

**Figure 16. CS8402A Audio Serial Port Formats**

## C, U, V Serial Port

The serial input pins for channel status (C), user (U), and validity (V) are sampled during the first bit period after the active edge of FSYNC for all formats except Format 4, which is sampled during the second bit period (coincident with the MSB). In Figure 16, the arrows on SCK indicate when the C, U, and V bits are sampled. The C, U, and V bits are transmitted with the audio sample entered before the FSYNC edge that sampled it. The V bit, as defined in the audio standards, is set to zero to indicate the audio data is suitable for conversion to analog. Therefore, when the audio data is errored, or the data is not audio, the V bit should be set high. The channel status serial input pin (C) is not available in consumer mode when the CD subcode port is enabled (FC1 = FC0 = high). Any channel status data entered through the channel status serial input (C) is logically OR'ed with the data entered through the dedicated pins or internally generated.

## RST and CBL (TRNPT is low)

When  $\overline{RST}$  goes low, the differential line drivers are set to ground and the block counters are reset to the beginning of the first block. In order to properly synchronize the CS8402A to the audio serial port, the transmit timing counters, which include CBL, are not enabled after  $\overline{RST}$  goes high until eight and one half SCK periods after the active edge (first edge after reset is exited) of FSYNC. When FSYNC is configured as a left/right signal (all defined formats except 2), the counters and CBL are not enabled until the right sample is being entered (during which the previous left sample is being transmitted). This guarantees that channel A is left and channel B is right as per the digital audio interface specs.

As shown in Figure 17, CBL, channel block start output, can assist in serially inputting the C, U and V bits as CBL goes high one bit period before the first bit of the preamble of the first sub-frame of the channel status block is trans-

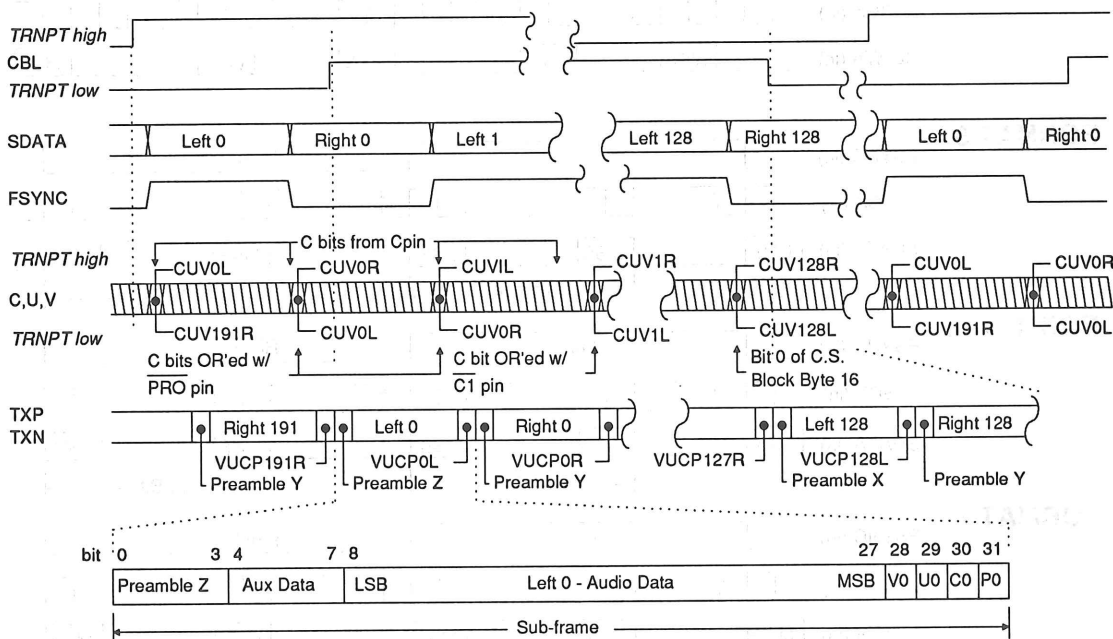


Figure 17. CBL and Transmitter Timing

mitted. This sub-frame contains channel status byte 0, bit 0. CBL returns low one bit period before the start of the frame that contains bit 0 of channel status byte 16. CBL is the exact inverse of flag 1 in mode 0 on the CS8401 (see Figure 11). CBL is not available when the CD subcode port is enabled.

Figure 17 illustrates timing for stereo data input on the audio port. Notice how CBL rises while the right channel data (Right 0) is input, but the previous left channel data (Left 0) is being transmitted as the first sub-frame of the channel status block (starting with preamble Z). The C, U, and V input ports only need to be valid for a short period after FSYNC changes. A sub-frame includes one audio sample while a frame includes a stereo pair. A channel status (C.S.) block contains 24 bytes of channel status and 384 audio samples (or 192 stereo pairs, or frames, of samples).

Figure 17 shows the CUV ports as having left and right bits (e.g. CUV0L, CUV0R). Since the C.S. block is defined as 192 bits, or one bit per frame, there are actually 2 C.S. blocks, one for channel A (left) and one for channel B (right). When inputting stereo audio data, both blocks normally contain the same information, so COL and COR from the input port pin are both channel status bit 0 of byte 0, which is defined as professional/consumer. These first two bits from the port, COL and COR, are logically OR'ed with the inverse of  $\overline{PRO}$ , since  $\overline{PRO}$  is a dedicated channel status pin defined as C.S. bit 0. Also, if in professional mode,  $\overline{C1}$ ,  $\overline{C6}$ ,  $\overline{C7}$  and  $\overline{C9}$  are dedicated C.S. pins. The inverse of  $\overline{C1}$  is logically OR'ed with channel status input port bits C1L and C1R. In similar fashion,  $\overline{C6}$ ,  $\overline{C7}$  and  $\overline{C9}$  are OR'ed with their respective input bits. Also, the C bits in CUV128L and CUV128R are both channel status block bit 128, which is bit 0 of channel status byte 16.

### Transparent Mode

In certain applications it is desirable to receive digital audio data with the CS8412 and retransmit it with the CS8402A. In this case, channel status, user and validity information must pass through unaltered. For studio environments, AES recommends that signal timing synchronization be maintained throughout the studio. Frame synchronization of digital audio signals input to and output from a piece of equipment must be within  $\pm 5\%$ .

The transparent mode of the CS8402A is selected by setting TRNPT, pin 24, high. In this mode, the CBL pin becomes an input, allowing direct connection of the outputs of the CS8412 to the inputs of the CS8402A as shown in Figure 18. The transmitter and receiver are synchronized by the FSYNC signal. CBL specifies the start of a new channel status block boundary, allowing the transmit block structure to be slaved to the block structure of the receiver. In the transparent mode, C, U, and V are now transmitted with the current audio sample as shown in Figure 17 (TRNPT high), and the dedicated channel status pins are ignored. When in the transparent mode, the propagation delay of data through the CS8402A is set so that the total propagation delay from the receive inputs of the CS8412 to the transmit outputs of the CS8402A is three frames.

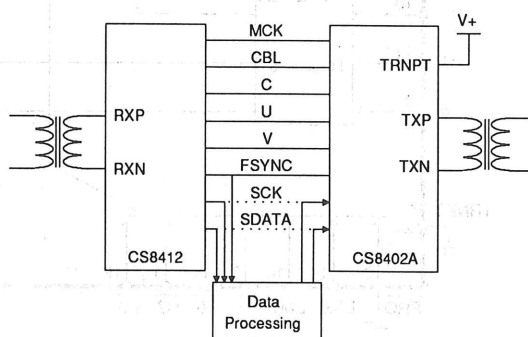


Figure 18. Transparent Mode Interface

When FSYNC is a word clock (Format 2), CBL is sampled when left C,U,V are sampled. When FSYNC is Left/Right, CBL is sampled when left C,U,V are sampled. The channel status block boundary is reset when CBL transitions from low to high (based on two successive samples of CBL). MCK for the CS8402A is normally expected to be 128 times the sample frequency, in the transparent mode MCK must be 256 Fs.

### Professional Mode

Setting  $\overline{\text{PRO}}$  low places the CS8402A in professional mode as shown in Figure 19. In professional mode, channel status bit 0 is transmitted as a one and bits 1, 2, 3, 4, 6, 7, and 9 can be controlled via dedicated pins. The pins are actually the inverse of the identified bit. For example, tying the  $\overline{\text{C1}}$  pin low places a one in channel status bit 1. As shown in the Application Note, Overview of AES/EBU Digital Audio Interface Data Structures, C1 indicates audio/non-audio; C6 and C7 determine the sample frequency; and C9 allows the encoded channel mode to be stereophonic. EM1 and EM0 determine emphasis and encode C2, C3, C4 as

shown in Table 4. The dedicated channel status pins are read at the appropriate time and are logically OR'ed with data input on the channel status port, C. In Transparent Mode, these dedicated channel status pins are ignored; and channel status bits are input at the C pin.

The channel status data cyclic redundancy check character (C.S. byte 23) is always generated independently for channels A and B and is transmitted at the end of the channel status block.

Data should not be input thru the channel status port, C, during the CRCC byte time frame, since inputs on C are logically OR'ed with internally generated data.

### Consumer Mode

Setting  $\overline{\text{PRO}}$  high places the CS8402A in consumer mode which redefines the pins as shown in Figure 20. In consumer mode, channel status bit 0 is transmitted as a zero and channel status bits 2, 3, 8, 9, 15, 24, and 25 are controlled via dedicated pins. The pins are actually the inverse of the bit so if pin

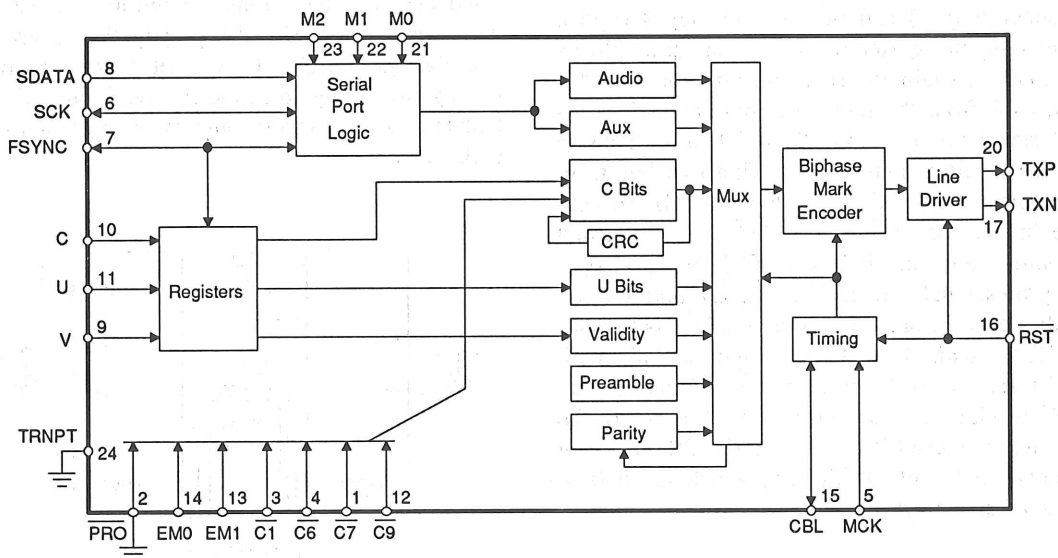


Figure 19. CS8402A Block Diagram - Professional Mode

$\overline{C2}$  is tied high, channel status bit 2 will be transmitted as a zero. Also, FC0 and FC1 are encoded versions of channel status bits 24 and 25, which define the sample frequency. When FC0 and FC1 are both high, the part is placed in a CD submode which activates the CD subcode port. This submode is described in detail in the next section. Table 5 describes the encoding of C24 and C25 through the FC1 and FC0 pins. According to AES/EBU standards, C2 is copy prohibit/permit, C3 specifies pre-emphasis, C8 and C9 define the category code, and C15 identifies the generation status of the transmitted material (ie. first generation, second generation).

### Consumer - CD Submode

The consumer CD submode is invoked by placing the part in consumer mode ( $\overline{PRO}$  = high) and

setting both FC1 and FC0 high. This mode redefines some of the pins for a CD subcode port as shown in Figure 21. The CD subcode port pins, SBF and SBC, replace the channel status serial input, C, and the channel status block start output, CBL. The user data serial input, U, becomes the subcode input. Figure 22 describes the timing for the CD subcode port. When SBF is low, SBC goes high one and a half SCK periods after the active edge of FSYNC for audio serial input port format 4, and one half SCK period after the active edge of FSYNC for all other formats. SBC stays high for one SCK period. SBF high for more than 16 SBC periods indicates the start of a subcode block. The first, third, and fourth Q bits after the start of a subcode block become channel status bits 5, 2, and 3 respectively.

EM1	EM0	C2	C3	C4
0	0	1	1	1
0	1	1	1	0
1	0	1	0	0
1	1	0	0	0

FC1	FC0	C24	C25	Comments
0	0	0	0	44.1 kHz
0	1	0	1	48 kHz
1	0	1	1	32 kHz
1	1	0	0	44.1 kHz, CD Mode

Table 4. Emphasis Encoding

Table 5. Sample Frequency Encoding

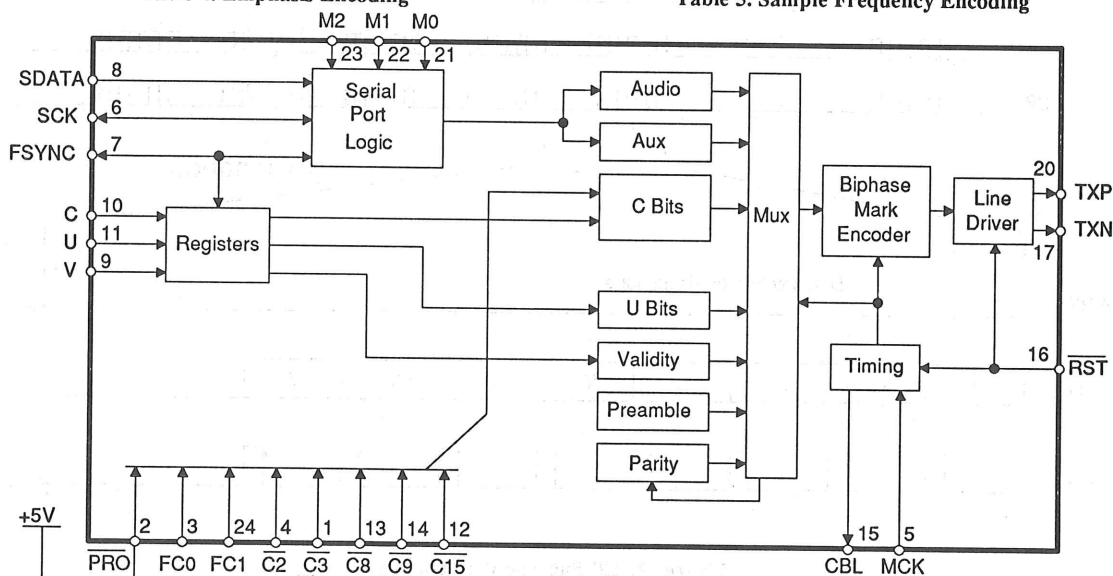
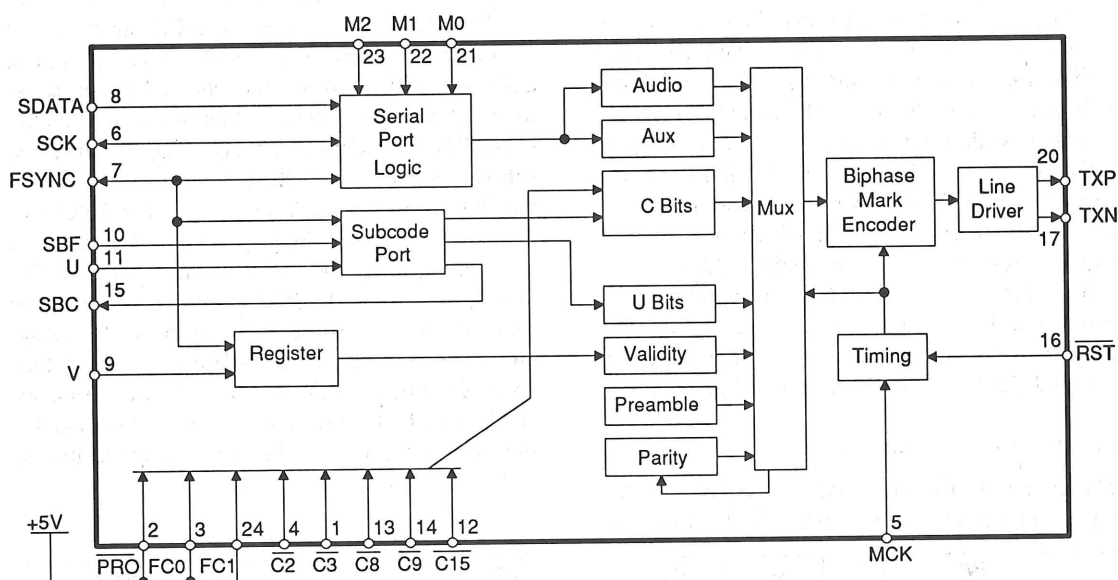
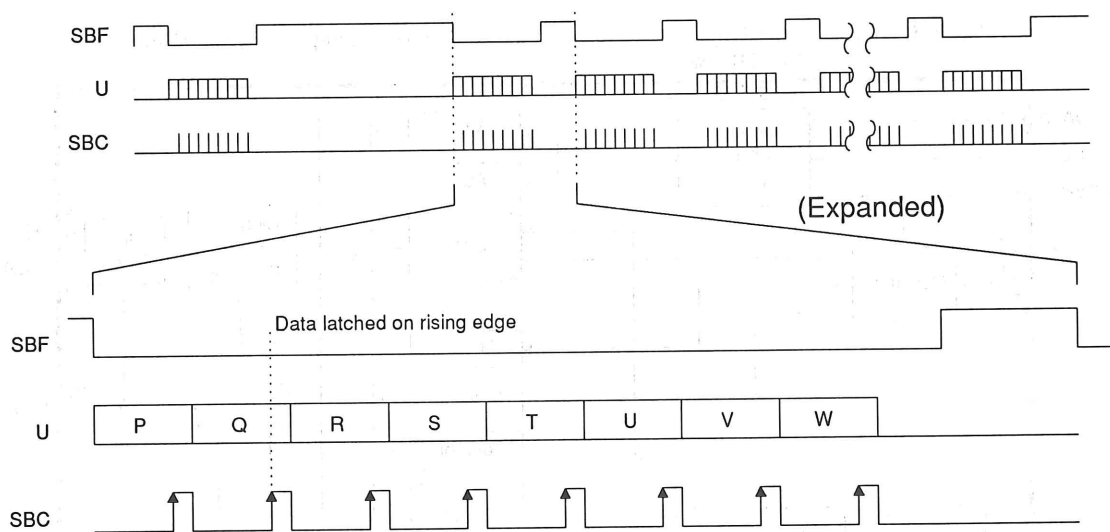


Figure 20. CS8402A Block Diagram - Consumer Mode



**Figure 21. CS8402A Block Diagram - Consumer Mode, CD Submode**



**Figure 22. CD Subcode Port Timing**



### PIN DESCRIPTIONS

#### CS8402A

CS BIT 7 / CS BIT 3	<b>C7/C3</b>	1	24	<b>TRNPT/FC1</b>	SAMPLE ADDR. / FREQ. CTRL 1
PROFESSIONAL MODE	<b>PRO</b>	2	23	<b>M2</b>	SERIAL PORT MODE SELECT 2
CS BIT 1 / FREQ. CTRL. 0	<b>C1/FC0</b>	3	22	<b>M1</b>	SERIAL PORT MODE SELECT 1
CS BIT 6 / CS BIT 2	<b>C6/C2</b>	4	21	<b>M0</b>	SERIAL PORT MODE SELECT 0
MASTER CLOCK	<b>MCK</b>	5	20	<b>TXP</b>	TRANSMIT POSITIVE
SERIAL DATA CLOCK	<b>SCK</b>	6	19	<b>VD+</b>	POWER
FRAME SYNC	<b>FSYNC</b>	7	18	<b>GND</b>	GROUND
SERIAL INPUT DATA	<b>SDATA</b>	8	17	<b>TXN</b>	TRANSMIT NEGATIVE
VALIDITY INPUT	<b>V</b>	9	16	<b>RST</b>	MASTER RESET
CS SERIAL IN / SC FRAME CLOCK	<b>C/SBF</b>	10	15	<b>CBL/SBC</b>	CS BLOCK OUT / SC BIT CLOCK
USER DATA INPUT	<b>U</b>	11	14	<b>EM0/C9</b>	EMPHASIS 0 / CS BIT 9
CS BIT 9 / CS BIT 15	<b>C9/C15</b>	12	13	<b>EM1/C8</b>	EMPHASIS 1 / CS BIT 8

2

### Power Supply Connections

#### VD+ - Positive Digital Power, PIN 19.

Positive supply for the digital section. Nominally +5 volts.

#### GND - Ground, PIN 18.

Ground for the digital section.

### Audio Input Interface

#### SCK - Serial Clock, PIN 6.

Serial clock for SDATA pin which can be configured (via the M0, M1, and M2 pins) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will contain 32 clocks for every audio sample. As an input, it does not need to be continuous and can be up to 15 MHz.

#### FSYNC - Frame Sync, PIN 7.

Delineates the serial data and may indicate the particular channel, left or right, and may be an input or output. The format is based on M0, M1, and M2 pins.

#### SDATA - Serial Data, PIN 8.

Audio data serial input pin.

#### M0, M1, M2 - Serial Port Mode Select, PINS 21, 22, 23.

Selects the format of FSYNC and the sample edge of SCK with respect to SDATA.

### Control Pins

#### RST - Master Reset, PIN 16.

When low, all internal counters are reset and the line drivers are disabled.

**V - Validity, PIN 9.**

Validity bit serial input port. This bit is defined as per the digital audio standards wherein  $V = 0$  signifies the audio signal is suitable for conversion to analog.  $V = 1$  signifies the audio signal is not suitable for conversion to analog, i.e. invalid.

**U - User Bit, PIN 11.**

User bit serial input port.

 **$\overline{PRO}$  - Professional/Consumer Select, PIN 2.**

Selects between professional mode ( $\overline{PRO}$  low) and consumer mode ( $\overline{PRO}$  high). This pin defines the functionality of the next seven pins.  $\overline{PRO}$  is ignored in Transparent Mode.

 **$\overline{C9/C15}$  - Channel Status Bit 9 / Channel Status Bit 15, PIN 12.**

In professional mode,  $\overline{C9}$  is the inverse of channel status bit 9 (bit 1 of byte 1). In consumer mode,  $\overline{C15}$  is the inverse of channel status bit 15 (bit 7 of byte 1).  $\overline{C9/C15}$  are ignored in Transparent Mode.

 **$\overline{EM0/C9}$  - Emphasis 0 / Channel Status Bit 9, PIN 14.**

In professional mode,  $\overline{EM0}$  and  $\overline{EM1}$  encode channel status bits 2, 3, and 4. In consumer mode,  $\overline{C9}$  is the inverse of channel status bit 9 (bit 1 of byte 1).  $\overline{EM0/C9}$  are ignored in Transparent Mode.

 **$\overline{EM1/C8}$  - Emphasis 1 / Channel Status Bit 8, PIN 13.**

In professional mode,  $\overline{EM0}$  and  $\overline{EM1}$  encode channel status bits 2, 3, and 4. In consumer mode,  $\overline{C8}$  is the inverse of channel status bit 8 (bit 0 of byte 1).  $\overline{EM1/C8}$  are ignored in Transparent Mode.

 **$\overline{C7/C3}$  - Channel Status Bit 7 / Channel Status Bit 3, PIN 1.**

In professional mode,  $\overline{C7}$  is the inverse of channel status bit 7. In consumer mode,  $\overline{C3}$  is the inverse of channel status bit 3.  $\overline{C7/C3}$  are ignored in Transparent Mode.

 **$\overline{C6/C2}$  - Channel Status Bit 6 / Channel Status Bit 2, PIN 4.**

In professional mode,  $\overline{C6}$  is the inverse of channel status bit 6. In consumer mode,  $\overline{C2}$  is the inverse of channel status bit 2.  $\overline{C6/C2}$  are ignored in Transparent Mode.

 **$\overline{C1/FC0}$  - Channel Status Bit 1 / Frequency Control 0, PIN 3.**

In professional mode,  $\overline{C1}$  is the inverse of channel status bit 1. In consumer mode,  $\overline{FC0}$  and  $\overline{FC1}$  are encoded versions of channel status bits 24 and 25 (bits 0 and 1 of byte 3). When  $\overline{FC0}$  and  $\overline{FC1}$  are both high, CD mode is selected.  $\overline{C1/FC0}$  are ignored in Transparent Mode.

**TRNPT/FC1 - Transparent Mode / Frequency Control 1, PIN 24.**

In professional mode, setting TRNPT low selects normal operation & CBL is an output. Setting TRNPT high, allows the CS8402A to be connected directly to a CS8412. In transparent mode, CBL is an input & MCK must be at 256 Fs.

In consumer mode, FC0 and FC1 are encoded versions of channel status bits 24 and 25. When FC0 and FC1 are both high, CD mode is selected.

**C/SBF - Channel Status Serial Input / Subcode Frame Clock, PIN 10.**

In professional and consumer modes this pin is the channel status serial input port. In CD mode this pin inputs the CD subcode frame clock.

**CBL/SBC - Channel Status Block Output / Subcode Bit Clock, PIN 15.**

In professional and consumer modes, the channel status block output is high for the first 16 bytes of channel status. In CD mode, this pin outputs the subcode bit clock.

***Transmitter Interface*****MCK - Master Clock, PIN 5.**

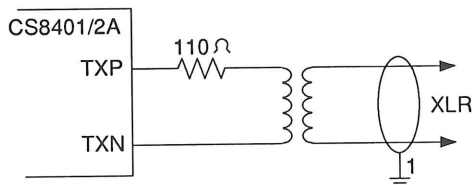
Clock input at  $128\times$  the sample frequency which defines the transmit timing.

**TXP, TXN - Differential Line Drivers, PINS 20, 17.**

RS422 compatible line drivers.

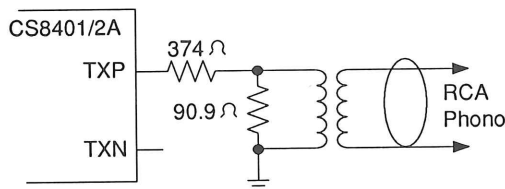
## Appendix A: RS422 Driver Information

The RS422 drivers on the CS8401A and CS8402A are designed to drive both the professional and consumer interfaces. The AES/EBU specification for professional/broadcast use calls for a  $110\Omega$  source impedance and a balanced drive capability. Since the transmitter impedance is very low, a  $110\Omega$  resistor should be placed in series with one of the transmit pins. (A  $110\Omega$  resistor in parallel with the transformer would, with the receiver impedance of  $110\Omega$ , provide a  $55\Omega$  load to the part which is too low.) The specifications call for a balanced output drive of 2-7 volts peak-to-peak into a  $110\Omega$  load with no cable attached. Using the circuit in Figure A1, the output of the transformer is short-circuit protected, has the proper source impedance, and provides a 5 volt peak-to-peak signal into a  $110\Omega$  load. Lastly, the two output pins should be attached to an XLR connector with male pins and a female shell, and with pin 1 of the connector grounded.

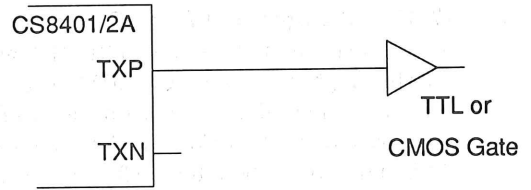


**Figure A1. Professional Output Circuit**

In the case of consumer use, the specifications call for an unbalanced drive circuit with an output impedance of  $75\Omega$  and a output drive level of 0.5 volts peak-to-peak  $\pm 20\%$  when measured across a  $75\Omega$  load using no cable. The circuit



**Figure A2. Consumer Output Circuit**



**Figure A3. TTL/CMOS Output Circuit**

shown in Figure A2 only uses the TXP pin and provides the proper output impedance and drive level using standard 1% resistors. The connector for consumer would be an RCA phono socket. This circuit is also short circuit protected.

The TXP pin may be used to drive TTL or CMOS gates as shown in Figure A3. This circuit may be used for optical connectors for digital audio since they are usually TTL compatible. This circuit is also useful when driving multiple digital audio outputs since RS422 line drivers have TTL interfaces.

The transformer should be capable of operating from 1.5 to 7 MHz, which is the audio data rate of 25 kHz to 55 kHz after biphasemark encoding. Transformers provide isolation from ground loops, 60 Hz noise, and common mode noise and interference. One of the important considerations when choosing transformers is minimizing shunt capacitance between primary and secondary windings. The higher the shunt capacitance, the lower the isolation between primary and secondary, and the more coupling of high frequency energy. This energy appears in the form of common mode noise on the receive side and has the potential to degrade analog performance. Therefore, for best performance, shielded transformers optimized for minimum shunt capacitance should be used. The following are a few typical transformers:

Pulse Engineering  
Telecom Products Group  
7250 ConvoY Ct.  
San Diego, CA 92111

(619) 268-2400

Part Number: PE65612

Schott Corporation

1000 Parkers Lane Rd.

Wayzata, MN 55391

(612) 475-1173

FAX (612) 475-1786

Part Number:

67125450 - compatible with Pulse

67128990 - lower cost

67129000 - surface mount

67129600 - single shield

Scientific Conversions Inc.

2800 Third Street

San Francisco, CA 94107

(415) 821-6464

Part Number: SC916-01 - single shield

### Appendix B: MCK and FSYNC Relationship

FSYNC should be derived either directly or indirectly from MCK. The indirect case could be a DSP, providing FSYNC through its serial port, using the same master oscillator that generates MCK. In either case, FSYNC's relationship to MCK is fixed and does not move. Since this appendix provides information on what would happen if FSYNC did move with respect to MCK, it does not apply to the majority of users.

All internal timing is derived from MCK. On the CS8402A, MCK is always  $128 \times F_s$ . On the CS8401A, the external MCK is programmable and is initially divided to  $128 \times F_s$  before being used by the part. The internal clock IMCK used in the following discussion is always  $128 \times F_s$  regardless of the external MCK pin.

After  $\overline{RST}$ , the CS8401A and CS8402A synchronize the internal timing to the audio data port, more specifically FSYNC, to guarantee that channel A is left channel data and channel B is right channel data as per the AES/EBU specification. If FSYNC moves with respect to IMCK, the transmitter could lose synchronization, which causes an internal reset.

Figure B1 shows the structure of the serial port input, to the transmitter output. The audio data is serially shifted into R1. PLD is an internal signal that parallel loads R1 into the R2 buffer, and, at the same time, the C, U, and V bits are latched. On the CS8401A, the C, U, and V bits are held in RAM, whereas on the CS8402A, they are latched from external pins. The PLD signal rises on the first SCK edge that can latch data. This is coincident with the latching of the MSB of audio data in MSB-first, left-justified modes. PLD stays high for one SCK period. In the CS8402A section, the arrows on SCK in Figure 16 indicate when PLD goes high. Also, SBC in the CS8402A CD submode is an external version of PLD gated by the SBF input.

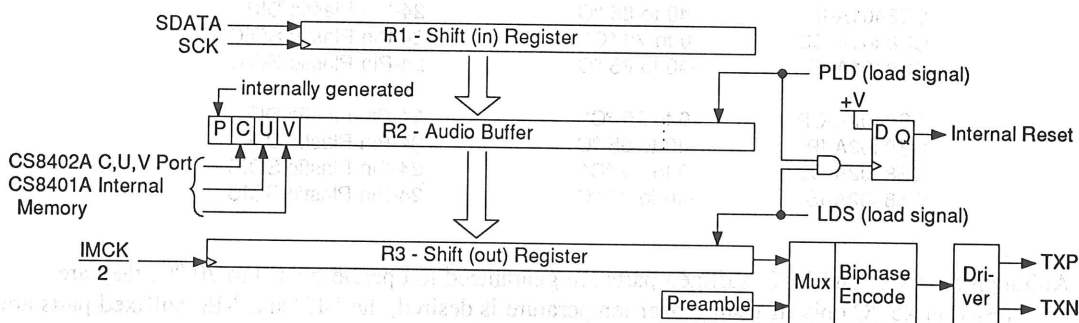
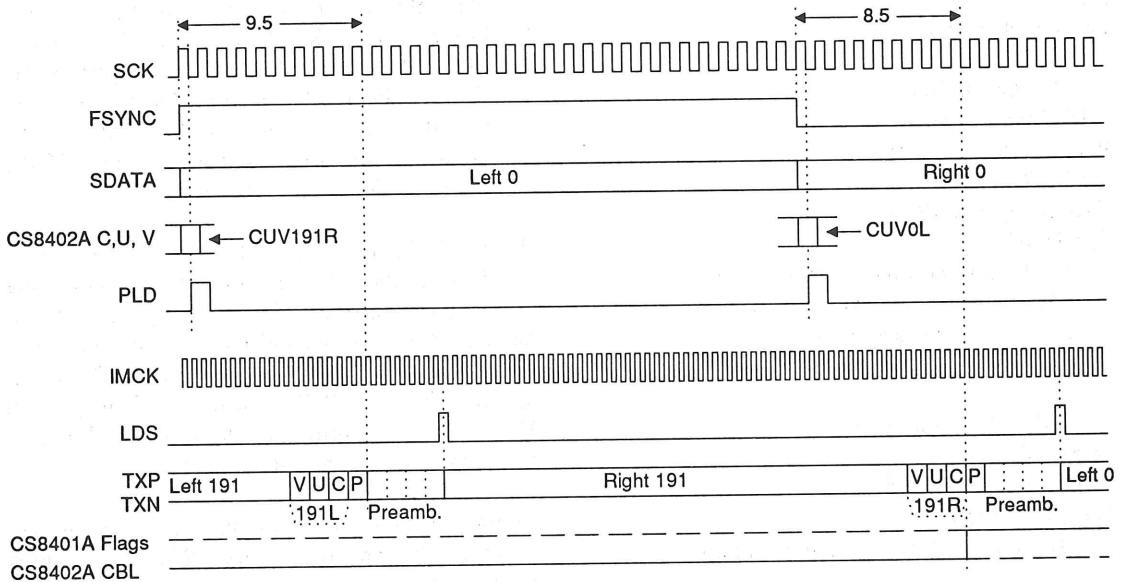


Figure B1. Serial Port-to-Transmitter Block Diagram



**Figure B2. Serial Ports-to-Transmitter Timing**

When the part is finished transmitting the preamble of a sub-frame, the internal signal LDS rises to parallel-load R2 into R3 for transmission. After  $\overline{\text{RST}}$ , the part synchronizes the audio port to IMCK as shown in Figure B2. Since PLD is based on FSYNC and LDS is based on

IMCK, if FSYNC moves with respect to IMCK until PLD and LDS occur at the same time, the data would not be properly loaded into R3. If LDS and PLD overlap, an internal reset is initiated causing the timing to return to the initial state shown in Figure B2.

### Ordering Guide

Model	Temperature Range	Package
CS8401A-CP	0 to 70 °C*	24-Pin Plastic DIP
CS8401A-IP	-40 to 85 °C	24-Pin Plastic DIP
CS8401A-CS	0 to 70 °C*	24-Pin Plastic SOIC
CS8401A-IS	-40 to 85 °C	24-Pin Plastic SOIC
CS8402A-CP	0 to 70 °C*	24-Pin Plastic DIP
CS8402A-IP	-40 to 85 °C	24-Pin Plastic DIP
CS8402A-CS	0 to 70 °C*	24-Pin Plastic SOIC
CS8402A-IS	-40 to 85 °C	24-Pin Plastic SOIC

\* Although the '-CP' and '-CS' suffixed parts are guaranteed to operate over 0 to 70 °C, they are tested at 25 °C only. If testing over temperature is desired, the '-IP' and '-IS' suffixed parts are tested over their specified temperature range.

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## •Notes•

## Digital Audio Interface Receiver

### Features

- Monolithic CMOS Receiver
- Low-Jitter, On-Chip Clock Recovery  
256xFs Output Clock Provided
- Supports: AES/EBU, IEC 958,  
S/PDIF, & EIAJ CP-340  
Professional and Consumer Formats
- Extensive Error Reporting  
Repeat Last Sample on Error Option
- On-Chip RS422 Line Receiver
- Configurable Buffer Memory (CS8411)

### General Description:

The CS8411/12 are monolithic CMOS devices which receive and decode audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8411/12 receive data from a transmission line, recover the clock and synchronization signals, and de-multiplex the audio and digital data. Differential or single ended inputs can be decoded.

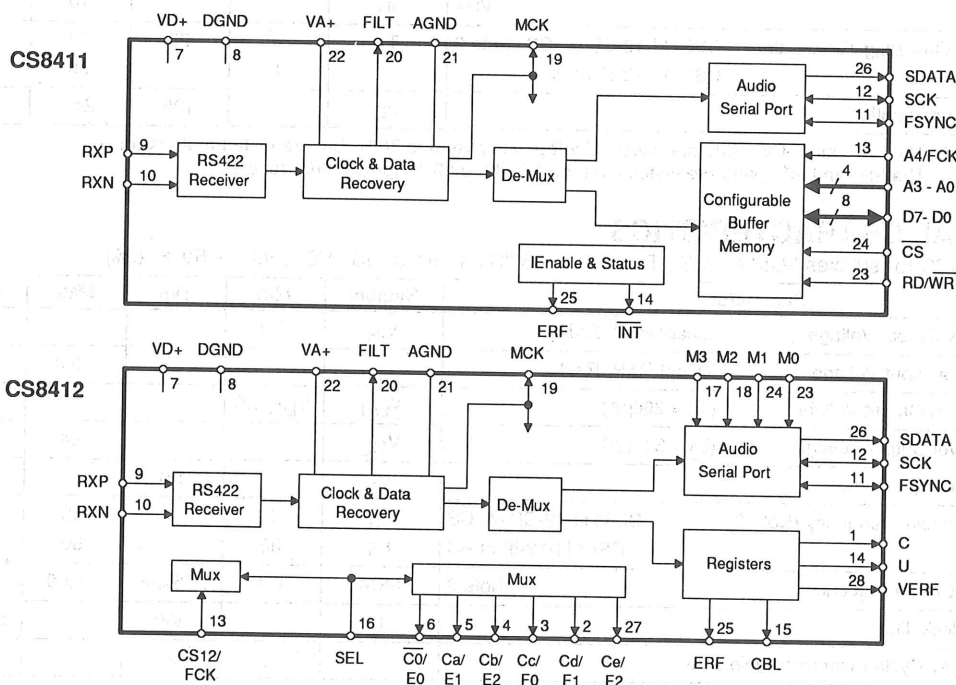
The CS8411 has a configurable internal buffer memory, read via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8412 de-multiplexes the channel, user, and validity data directly to serial output pins with dedicated output pins for the most important channel status bits.

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### Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation  
P.O. Box 17847, Austin, TX 78760  
(512) 445-7222 FAX: (512) 445-7581

MAR '92  
DS61PP3  
2-261

**ABSOLUTE MAXIMUM RATINGS** (GND = 0V, all voltages with respect to ground)

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	VD+, VA+		6.0	V
Input Current, Any Pin Except Supply <span style="float: right;">Note 1</span>	I <sub>in</sub>		±10	mA
Input Voltage, Any Pin except RXP, RXN	V <sub>IN</sub>	-0.3	VD+ + 0.3	V
Input Voltage, RXP and RXN	V <sub>IN</sub>	-12	12	V
Ambient Operating Temperature (power applied)	T <sub>A</sub>	-55	125	°C
Storage Temperature	T <sub>stg</sub>	-65	150	°C

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

**WARNING:** Operation beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS**

(GND = 0V; all voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	VD+, VA+	4.5	5.0	5.5	V
Supply Current <span style="float: right;">VA+ VD+</span>	I <sub>A</sub> I <sub>D</sub>		20 7	35 10	mA mA
Ambient Operating Temperature: CS8411/12-CP or -CS <span style="float: right;">Note 2</span>	T <sub>A</sub>	0 -40	25	70 85	°C °C
Power Consumption	P <sub>D</sub>		135	248	mW

Notes: 2. The '-CP' and '-CS' parts are specified to operate over 0 to 70 °C but are tested at 25 °C only.  
The '-IP' and '-IS' parts are tested over the full -40 to 85 °C temperature range.

**DIGITAL CHARACTERISTICS**

(T<sub>A</sub> = 25 °C for suffixes '-CP' & '-CS', T<sub>A</sub> = -40 to 85 °C for '-IP' & '-IS'; VD+, VA+ = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage <span style="float: right;">except RXP, RXN</span>	V <sub>IH</sub>	2.0			V
Low-Level Input Voltage <span style="float: right;">except RXP, RXN</span>	V <sub>IL</sub>			+0.8	V
High-Level Output Voltage (I <sub>O</sub> = 200µA)	V <sub>OH</sub>	V <sub>DD</sub> -1.0			V
Low-Level Output Voltage (I <sub>O</sub> = 3.2mA)	V <sub>OL</sub>			0.4	V
Input Leakage Current	I <sub>in</sub>		1.0	10	µA
Input Sample Frequency (Note 3) <span style="float: right;">CS8411/12-CP or -CS CS8411/12-IP or -IS</span>	F <sub>S</sub> F <sub>S</sub>	25 30		55 50	kHz kHz
Master Clock Frequency <span style="float: right;">Note 3</span>	MCK	6.4	256×F <sub>S</sub>	14.08	MHz
MCK Clock Jitter	t <sub>j</sub>		200		ps RMS
MCK Duty Cycle (high time/cycle time)			50		%

Notes: 3. F<sub>S</sub> is defined as the incoming audio sample frequency per channel.

Specifications are subject to change without notice.

## DIGITAL CHARACTERISTICS - RS422 RECEIVERS

(RXP, RXN pins only;  $V_{D+}$ ,  $V_{A+} = 5V \pm 10\%$ )

Parameter	Symbol	Min	Typ	Max	Units
Input Resistance $(-7V < V_{CM} < 7V)$ Note 4	$Z_{IN}$		10		$k\Omega$
Differential Input Voltage, RXP to RXN $(-7V < V_{CM} < 7V)$ Note 4,5	$V_{TH}$	200			mV
Input Hysteresis	$V_{HYST}$		50		mV

Notes: 4.  $V_{CM}$  - Input Common Mode Range

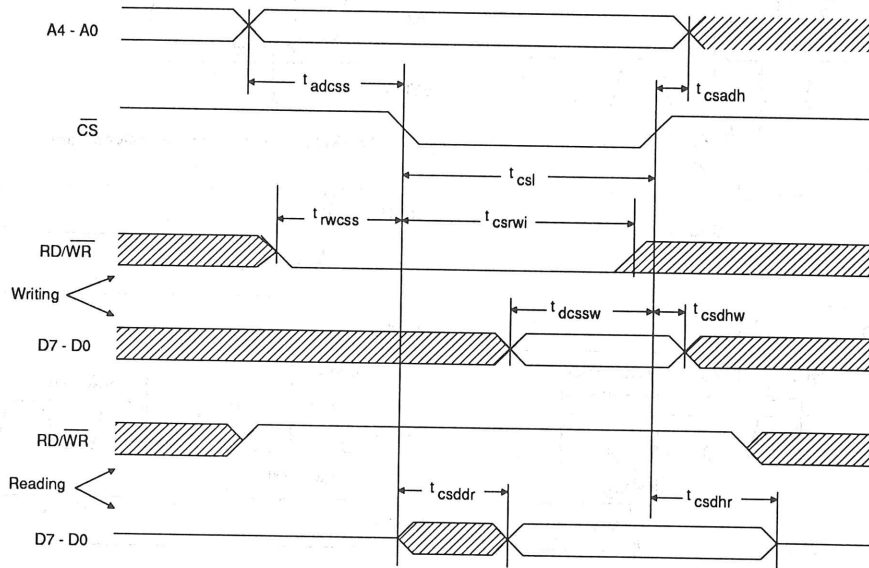
5. When the receiver inputs are configured for single ended operation (e.g. consumer configuration) the signal amplitude must exceed 400mVp-p for the differential voltage on RXP to RXN to exceed 200mV. This represents twice the minimum signal level of 200mVp-p specified in CP-340 and IEC-958 (which are not RS-422 compliant).

## SWITCHING CHARACTERISTICS - CS8411 PARALLEL PORT

( $T_A = 25^\circ C$  for suffixes '-CP' and '-CS';  $T_A = -40$  to  $85^\circ C$  for suffixes '-IP' and '-IS';

$V_{D+}$ ,  $V_{A+} = 5V \pm 10\%$ ; Inputs: Logic 0 = DGND, logic 1 =  $V_{D+}$ ;  $C_L = 20$  pF)

Parameter	Symbol	Min	Typ	Max	Units
ADDRESS valid to $\overline{CS}$ low	$t_{adcss}$	13.5			ns
$\overline{CS}$ high to ADDRESS invalid	$t_{csadh}$	0			ns
$RD/\overline{WR}$ valid to $\overline{CS}$ low	$t_{rwcss}$	10			ns
$\overline{CS}$ low to $RD/\overline{WR}$ invalid	$t_{csrwi}$	35			ns
$\overline{CS}$ low	$t_{csl}$	35			ns
DATA valid to $\overline{CS}$ rising $RD/\overline{WR}$ low (writing)	$t_{dcsw}$	32			ns
$\overline{CS}$ high to DATA invalid $RD/\overline{WR}$ low (writing)	$t_{csdhw}$	0			ns
$\overline{CS}$ falling to DATA valid $RD/\overline{WR}$ high (reading)	$t_{csddr}$			35	ns
$\overline{CS}$ rising to DATA Hi-Z $RD/\overline{WR}$ high (reading)	$t_{csdhr}$	5			ns



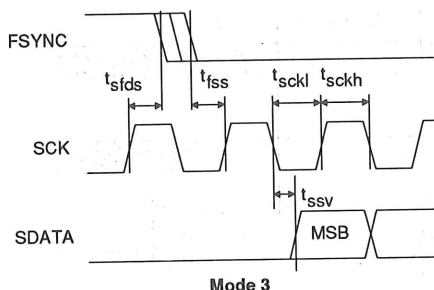
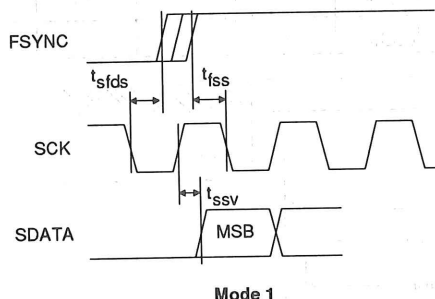
CS8411 Parallel Port Timing

## SWITCHING CHARACTERISTICS - SERIAL PORTS

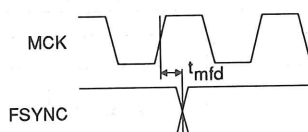
( $T_A = 25\text{ }^{\circ}\text{C}$  for suffixes '-CP' and '-CS';  $T_A = -40$  to  $85\text{ }^{\circ}\text{C}$  for suffixes '-IP' and '-IS';  
VD+, VA+ =  $5\text{V} \pm 10\%$ ; Inputs: Logic 0 = DGND, logic 1 = VD+;  $C_L = 20\text{ pF}$ )

Parameter			Symbol	Min	Typ	Max	Units
SCK Frequency	Master Mode	Notes 5,6	$f_{\text{sck}}$		OWRx32		Hz
	Slave Mode	Note 6			OWRx32	TBD	Hz
SCK falling to FSYNC delay	Master Mode	Notes 6,7	$t_{\text{sfdm}}$	-20		20	ns
SCK Pulse Width Low	Slave Mode	Note 6	$t_{\text{sckl}}$	40			ns
SCK Pulse Width High	Slave Mode	Note 6	$t_{\text{sckh}}$	40			ns
SCK rising to FSYNC edge delay	Slave Mode	Notes 6,7	$t_{\text{sfds}}$	20			ns
FSYNC edge to SCK rising setup	Slave Mode	Notes 6,7	$t_{\text{fss}}$	20			ns
SCK falling (rising) to SDATA valid		Note 7	$t_{\text{ssv}}$			20	ns
C, U, CBL valid to FSYNC edge	CS8412	Note 7	$t_{\text{cuvf}}$		$1/f_{\text{sck}}$		s
MCK to FSYNC edge delay	FSYNC from RXN/RXP		$t_{\text{mfd}}$		15		ns

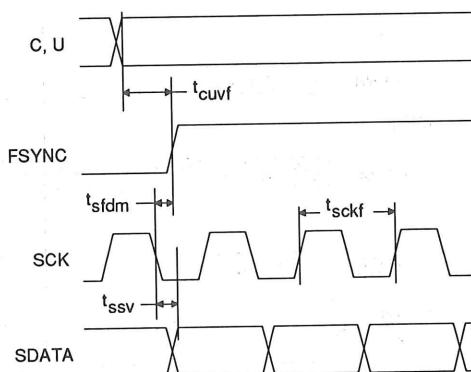
- Notes:
- The output word rate, OWR, refers to the frequency at which an audio sample is output from the part. (A stereo pair is two audio samples.) Therefore, in Master mode, there are always 32 SCK periods in one audio sample. In Slave mode 32 SCK periods must be provided in most serial port formats.
  - In master mode SCK and FSYNC are outputs. In Slave mode they are inputs. In the CS8411, control reg. 2 bit 1, MSTR, selects master. In the CS8412, formats 1 & 3 are slaves.
  - The table above assumes data is output on the falling edge and latched on the rising edge. With both parts the edge is selectable. The table is defined for the CS8411 with control reg. 2 bit 0, SCED, set to one, and for the CS8412 in formats 2, 3, 5 - 8. For the other formats, the table and figure edges must be reversed (ie. "rising" to "falling" and vice versa).



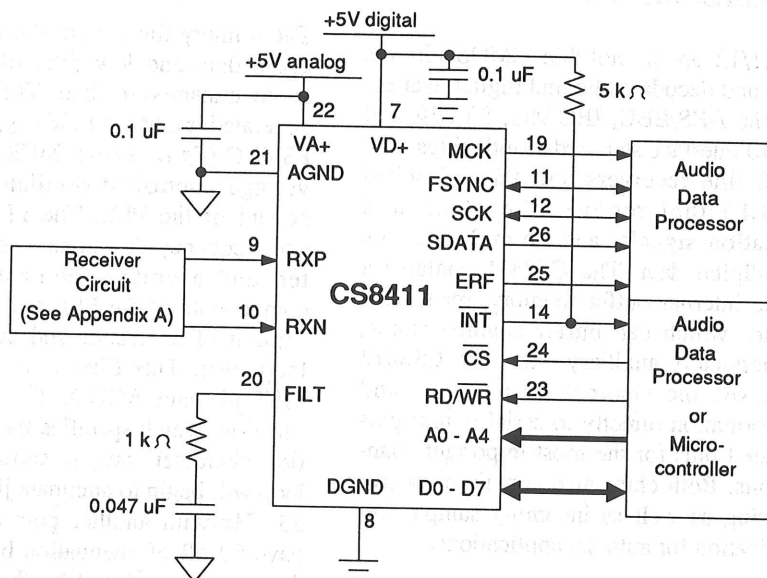
Serial Output Timing - Slave Mode



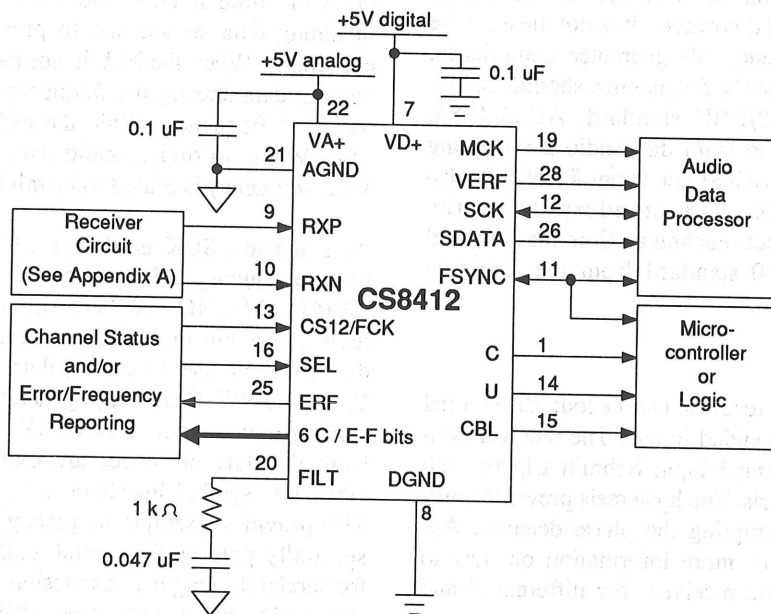
FSYNC Generated From Received Data



Serial Output Timing - Master Mode & C, U Port



**Figure 1. CS8411 Typical Connection Diagram**



**Figure 2. CS8412 Typical Connection Diagram**

## GENERAL DESCRIPTION

The CS8411/12 are monolithic CMOS circuits that receive and decode audio and digital data according to the AES/EBU, IEC 958, S/PDIF, and EIAJ CP-340 interface standards. Both chips contain RS422 line receivers and Phase-Locked Loops (PLL) that recover the clock and synchronization signals, and de-multiplex the audio and digital data. The CS8411 contains a configurable internal buffer memory, read via a parallel port, which can buffer channel status, user, and optionally auxiliary data. The CS8412 de-multiplexes the channel status, user, and validity information directly to serial output pins with dedicated pins for the most important channel status bits. Both chips also contain extensive error reporting as well as incoming sample frequency indication for auto-set applications.

Familiarity with the AES/EBU and IEC 958 specifications are assumed throughout this document. The CS8401/2 Digital Audio Transmitter data sheet contains an overview of the digital audio specification; however, it is not meant to be a complete reference. To guarantee compliance, the proper standards documents should be obtained. The AES/EBU standard, AES3-1985, should be obtained from the Audio Engineering Society or ANSI (ANSI document # ANSI S4.40-1985); the IEC 958 standard from the International Electrotechnical Commission; and the EIAJ CP-340 standard from the Japanese Electronics Bureau.

### *Line Receiver*

The RS422 line receiver can decode differential as well as single ended inputs. The receiver consists of a differential input Schmitt trigger with 50mV of hysteresis. The hysteresis prevents noisy signals from corrupting the phase detector. Appendix A contains more information on how to configure the line receivers for differential and single ended signals.

### *Clocks and Jitter Attenuation*

The primary function of these chips is to recover audio data and low jitter clocks from a digital audio transmission line. The clocks that can be generated are MCK ( $256 \times F_s$ ), SCK ( $64 \times F_s$ ), and FSYNC ( $F_s$  or  $2 \times F_s$ ). MCK is the output of the voltage controlled oscillator which is a component of the PLL. The PLL consists of phase and frequency detectors, a second-order loop filter, and a voltage controlled oscillator. All components of the PLL are on chip with the exception of a resistor and capacitor used in the loop filter. This filter is connected between the FILT pin and AGND. The closed-loop transfer function, which specifies the PLL's jitter attenuation characteristics, is shown in Figure 3. The loop will begin to attenuate jitter at approximately 25 kHz with another pole at 80 kHz, and will have 50 dB of attenuation by 1MHz. Since most data jitter introduced by the transmission line is high in frequency, it will be strongly attenuated.

Multiple frequency detectors are used to minimize the time it takes the PLL to lock to the incoming data stream and to prevent false lock conditions. When the PLL is not locked to the incoming data stream, the frequency detectors pull the VCO frequency within the lock range of the PLL. When no digital audio data is present, the VCO frequency is pulled to its minimum value.

As a master, SCK is always MCK divided by four, producing a frequency of  $64 \times F_s$ . In the CS8411, FSYNC can be programmed to be a divided version of MCK or it can be generated directly from the incoming data stream. In the CS8412, FSYNC is always generated from the incoming data stream. When FSYNC is generated from the data, its edges are extracted at times when intersymbol interference is at a minimum. This provides a sample frequency clock that is as spectrally pure as the digital audio source clock for moderate length transmission lines. For long transmission lines, the CS8411 can be



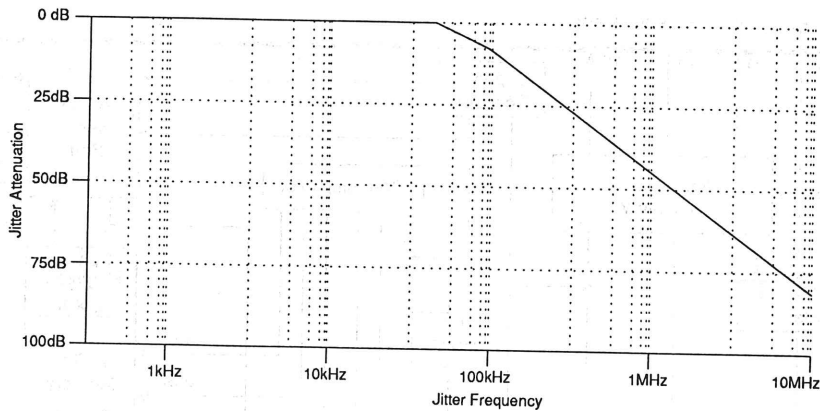


Figure 3. Jitter Attenuator Characteristics

programmed to generate FSYNC from MCK instead of from the incoming data.

## CS8411 DESCRIPTION

The CS8411 is more flexible than the CS8412 but requires a microcontroller or DSP to load internal registers. The CS8412 does not have internal registers so it may be used in a stand-alone mode where no microprocessor or DSP is available.

The CS8411 accepts data from a transmission line coded according to the digital audio interface standards. The I.C. recovers clock and data, and separates the audio data from control information. The audio data is output through a configurable serial port and the control information is stored in internal dual-port RAM. Extensive error reporting is available via internal registers with the option of repeating the last sample when an error occurs. A block diagram of the CS8411 is shown in Figure 4

### Parallel Port

The parallel port accesses two status registers, two interrupt enable registers, two control registers, and 28 bytes of dual-port buffer memory. The status registers and interrupt enable

registers occupy the same address space. A bit in control register 1 selects the two registers, either status or interrupt enable, that occupy addresses 0 and 1 in the memory map. The address bus and the RD/WR line should be valid when CS goes low. If RD/WR is low, the value on the data bus will be written into the buffer memory at the specified address. If RD/WR is high, the value in the buffer memory, at the specified address, is placed on the data bus. Detailed timing for the parallel port can be found in the *Switching Characteristics - Parallel Port* table.

The memory space on the CS8411 is allocated as shown in Figure 5. There are three defined buffer modes selectable by two bits in control register 1. Further information on the buffer modes can be found in the *Control Registers* section.

### Status and IEnable Registers

The status and interrupt enable registers occupy the same address space. The IER/SR bit in control register 1 selects whether the status registers (IER/SR = 0) or the IEnable registers (IER/SR = 1) occupy addresses 0 and 1. Upon power-up, the control and IEnable registers contain all zeros; therefore, the status registers are visible and all interrupts are disabled. The IER/SR bit must be set to make the IEnable registers visible.

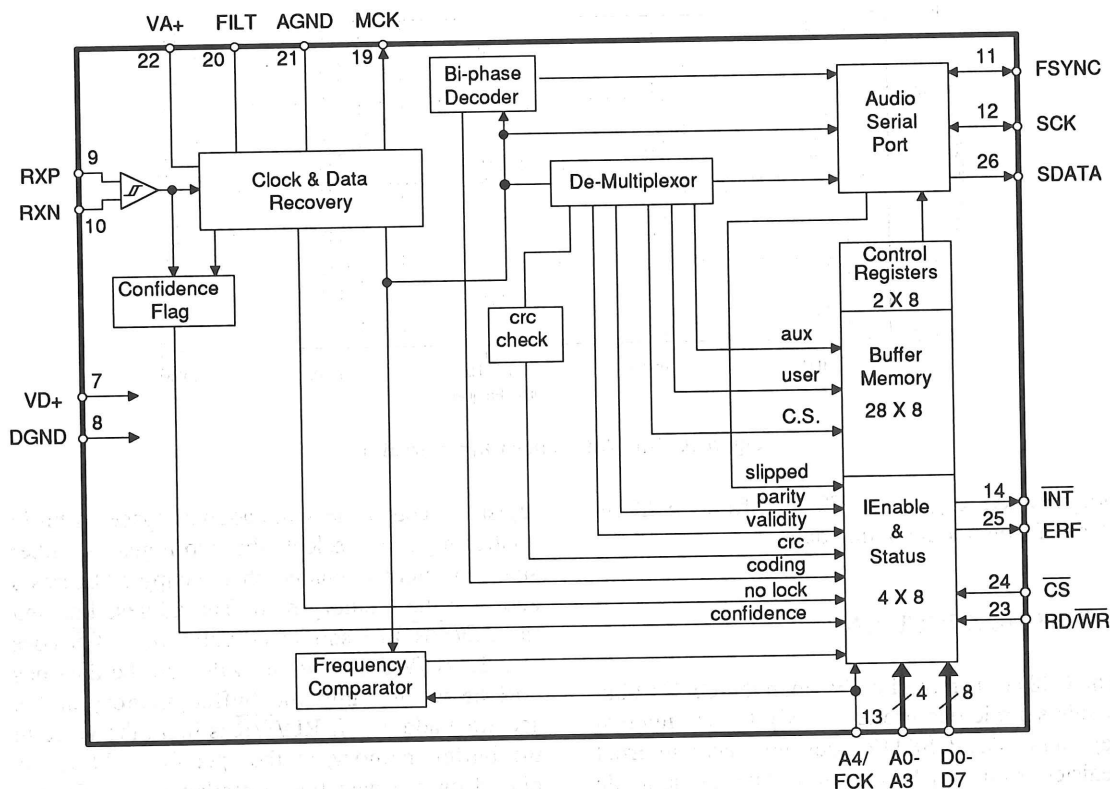


Figure 4. CS8411 Block Diagram

Status register 1 (SR1), shown in Figure 6, reports all the conditions that can generate a pulse on the interrupt pin (INT). The three least significant bits, FLAG2-FLAG0, are used to monitor the ram buffer. These bits continually change and indicate the position of the buffer pointer which points to the buffer memory location currently being written. Each flag has a corresponding interrupt enable bit in IEnable register 1 which, when set, allows a transition on the flag to generate a pulse on the interrupt pin. FLAG0 and FLAG1 cause interrupts on both edges whereas FLAG2 causes an interrupt on the rising edge only. Further information, including timing, on the flags can be found in the *Buffer Memory* section.

The next five bits; ERF, SLIP, CCHG, CRCE/CRC1, and CSDIF/CRC2, are latches which are set when their corresponding conditions occur, and are reset when SR1 is read. Interrupt pulses are generated the first time that condition occurs. If the status register is not read, further instances of that same condition will not generate another interrupt. ERF is the error flag bit and is set when the ERF pin goes high. It is an OR'ing of the errors listed in status register 2, bits 0 through 4, AND'ed with their associated interrupt enable bits in IEnable register 2.

SLIP is only valid when the audio port is in slave mode (FSYNC and SCK are inputs to the CS8411). This flag is set when an audio sample is dropped or reread because the audio data output from the part is at a different frequency than the

data received from the transmission line. CCHG is set when any bit in channel status bytes 0 through 3, stored in the buffer, changes from one block to the next. In buffer modes 0 and 1, only one channel of channel status data is buffered, so CCHG is only affected by that channel. (CS2/CS1 in CR1 selects which channel is buffered.) In buffer mode 2 both channels are buffered, so both channels affect CCHG. This bit is updated after each byte (0 to 3) is written to the buffer. The two most significant bits in SR1, CRCE/CRC1 and CSDIF/CRC2, are dual function flags. In buffer modes 0 and 1, they are CRCE and CSDIF, and in buffer mode 2, they are

CRC1 and CRC2. In buffer modes 0 and 1, the channel selected by the CS2/CS1 bit is stored in RAM and CRCE indicates that a CRC error occurred in that channel. CSDIF is set if there is any difference between the channel status bits of each channel. In buffer mode 2 channel status from both channels is buffered, with CRC1 indicating a CRC error in channel 1 and CRC2 indicating a CRC error in channel 2. CRCE, CRC1, and CRC2 are updated at the block boundary. Block boundary violations also cause CRC1,2 or CRCE to be set.

IEnable register 1, which occupies the same address space as status register 1, contains interrupt enable bits for all conditions in status register 1. A "1" in a bit location enables the same bit location in status register 1 to generate an interrupt pulse. A "0" masks that particular status bit from causing an interrupt.

Status register 2 (SR2) reports all the conditions that can affect the error flag bit in SR1 and the error pin (ERF), and can specify the received clock frequency. As previously mentioned, the first five bits of SR2 are AND'ed with their interrupt enable bits (in IER2) and then OR'ed to create ERF. The V, PARITY, CODE, LOCK, and

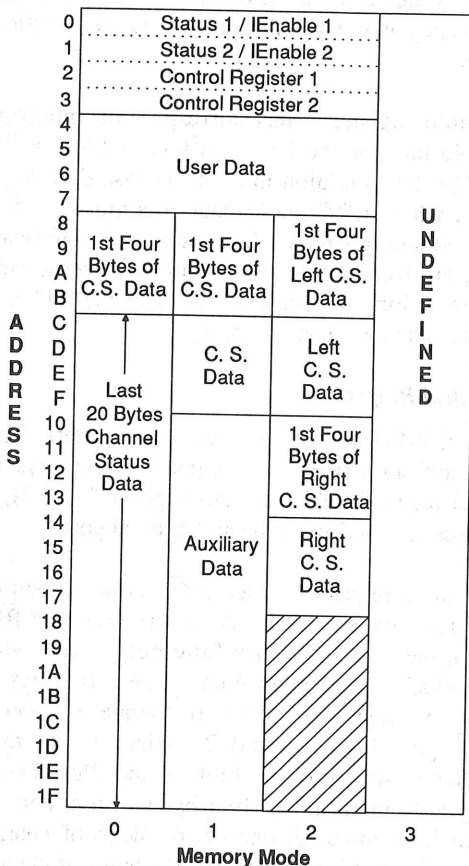
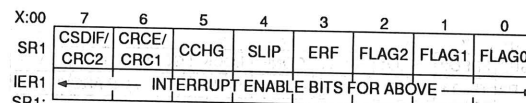


Figure 5. CS8411 Buffer Memory Map




- CSDIF: CS different between sub-frames. Buf. modes 0 & 1.
- CRC2: CRC Error - sub-frame 2. Buffer mode 2 only.
- CRCE: CRC Error - selected sub-frame. Buffer modes 0 & 1.
- CRC1: CRC Error - sub-frame 1. Buffer mode 2 only.
- CCHG: Channel Status changed
- SLIP: Slipped an audio sample
- ERF: Error Flag. ORing of all errors in SR2.
- FLAG2: High for first four bytes of channel status
- FLAG1: Memory mode dependent - See Figure 11
- FLAG0: High for last two bytes of user data.

IER1:  
Enables the corresponding bit in SR1.  
A "1" enables the interrupt. A "0" masks the interrupt.

Figure 6. Status/IEnable Register 1

CONF bits are latches which are set when their corresponding conditions occur, and are reset when SR2 is read. The ERF pin is asserted each time the error occurs assuming the interrupt enable bit in IER2 is set for that particular error. When the ERF pin is asserted, the ERF bit in SR1 is set. If the ERF bit was not set prior to the ERF pin assertion, an interrupt will be generated (assuming bit 3 in IER1 is set). Although the ERF pin is asserted for each occurrence of an enabled error condition, the ERF bit will only cause an interrupt once if SR1 is not read.

V is the validity status bit which is set any time the received validity bit is high. PARITY is set when a parity error is detected. CODE is set when a biphas coding error is detected. LOCK is asserted when the receiver PLL is not locked and occurs when there is no input on RXP/RXN, or if the received frequency is out of the receiver lock range (25 kHz to 55 kHz). Lock is achieved after receiving three frame preambles followed by one block preamble, and is lost after four consecutive frame preambles are not received. CONF is the confidence flag which is asserted when the received data eye opening is less than half a bit period. This indicates the transmission link is poor and does not meet specifications.

X:01	7	6	5	4	3	2	1	0
SR2	FREQ2	FREQ1	FREQ0	CONF	LOCK	CODE	PARITY	V
IER2	TEST1	TEST0		← INT. ENABLE BITS FOR ABOVE →				

### SR2:

FREQ2: The 3 FREQ bits indicate incoming sample freq.

FREQ1: (must have 6.144 MHz clock on FCK pin

FREQ0: and FCEN must be "1")

CONF: Confidence error

LOCK: Out-of-Lock error

CODE: Coding violation

PARITY: Parity error

V: Validity bit high

### IER2:

TEST1,0: (0 on power-up) Must stay at "0".

INT. ENABLES: Enables the corresponding bit in SR2.

A "1" enables the interrupt. A "0" masks the interrupt.

The upper three bits in SR2, FREQ2-FREQ0, can report the receiver frequency when the receiver is locked. These bits are only valid when FCEN in control register 1 is set, and a 6.144 MHz clock is applied to the FCK pin. When FCEN is set, the A4/FCK pin is used as FCK and A4 is internally set to zero; therefore, only the lower half of the buffer can be accessed. Table 2 lists the frequency ranges reported. The FREQ bits are updated three times per block and the clock on the FCK pin must be valid for two thirds of a block for the FREQ bits to be accurate. The vast majority of audio systems must meet the 400 ppm tolerance listed in the table. The 4% tolerance is provided for unique situations where the approximate frequency needs to be known, even though that frequency is outside the normal audio specifications.

IEnable register 2 has corresponding interrupt enable bits for the first five bits in SR2. A "1" enables the condition in SR2 to cause ERF to go high, while a "0" masks that condition. Bit 5 is unused and bits 6 and 7, the two most significant bits, are factory test bits and must be set to zero when writing to this register. The CS8411 sets these bits to zero on power-up.

## Control Registers

The CS8411 contains two control registers. Control register 1 (CR1), at address 2, selects system level features, while control register 2 (CR2), at address 3, configures the audio serial port.

In control register 1, when  $\overline{RST}$  is low, all outputs are reset except MCK. After the user sets  $\overline{RST}$  high, the CS8411 comes fully out of reset when the block boundary is found. The serial port, in master mode, will begin to operate as soon as  $\overline{RST}$  goes high. B0 and B1 select one of three buffer modes listed in Table 1 and illustrated in Figure 5. In all modes four bytes of user data are stored. In mode 0, one entire block of channel status is stored. In mode 1 eight bytes of channel status and sixteen bytes of auxiliary data are

Figure 7. Status/IEnable Register 2

stored. In mode 2, eight bytes of channel status from each sub-frame are stored. The buffer modes are discussed in more detail in the *Buffer Memory* section. The next bit, CS2/CS1, selects the particular sub-frame of channel status to buffer in modes 0 and 1, and has no effect in mode 2. When CS2/CS1 is low, sub-frame 1 is buffered, and when CS2/CS1 is high, sub-frame 2 is buffered. IER/SR selects which set of registers, either IEnable or status, occupy addresses 0 and 1. When IER/SR is low, the status registers occupy the first two addresses, and when IER/SR is high, the IEnable registers occupy those addresses. FCEN enables the internal frequency counter. A 6.144 MHz clock must be connected to the FCK pin as a reference. The value of the FREQ bits in SR2 are not valid until two thirds of a block of data is received. Since FCK and A4, the most significant address bit, occupy the same pin, A4 is internally set to zero when FCEN is high. Since A4 is forced to zero, the upper half of the buffer is not accessible while using the frequency compare feature. FPLL determines how FSYNC is derived. When FPLL is low, FSYNC is derived from the incoming data, and when

FPLL is high, it is derived from the internal phase-locked loop.

Control Register 2 configures the serial port which consists of three pins: SCK, SDATA, and FSYNC. SDATA is always an output, but SCK and FSYNC can be configured as inputs or outputs. FSYNC and SDATA can have a variety of shapes relative to each other, and the polarity of SCK can be controlled. The large variety of audio data formats provides an easy interface to most DSPs and other audio processors. SDATA is normally just audio data, but special modes are provided that output received biphasic data, or received NRZ data with zeros substituted for preamble. Another special mode allows an asynchronous SCK input to read audio data from the serial port without slipping samples. In this mode FSYNC and SDATA are outputs synchronized to the SCK input. Since SCK is asynchronous to the received clock, the number of SCK cycles between FSYNC edges will vary.

X:02	7	6	5	4	3	2	1	0
CR1	FPLL	FCEN	IER/SR	CS2/CS1	B1	B0	RST	

FPLL: 0 - FSYNC from RXP/RXN, 1 - FSYNC from PLL  
 FCEN: enables freq. comparator (FCK must be 6.144 MHz).  
 IER/SR: [X:00,01] 0 - status, 1 - interrupt enable registers.  
 CS2/CS1: ch. status to buffer; 0 - sub-frame 1, 1 - sub-frame 2.  
 B1: with B0, selects the buffer memory mode.  
 B0: with B1, selects the buffer memory mode.  
 RST: Resets internal counters. Set to "1" for normal operation.

Figure 8. Control Register 1

B1	B0	Mode	Buffer Memory Contents
0	0	0	Channel Status
0	1	1	Auxiliary Data
1	0	2	Independent Channel Status
1	1	3	Reserved

Table 1. Buffer Memory Modes

X:03	7	6	5	4	3	2	1	0
CR2	ROER	SDF2	SDF1	SDF0	FSF1	FSF0	MSTR	SCED

ROER: Repeat previous value on error (audio data)  
 SDF2: with SDF0 & SDF1, select serial data format.  
 SDF1: with SDF0 & SDF2, select serial data format.  
 SDF0: with SDF1 & SDF2, select serial data format.  
 FSF1: with FSF0, select FSYNC format.  
 FSF0: with FSF1, select FSYNC format.  
 MSTR: When set, SCK and FSYNC are outputs.  
 SCED: When set, falling edge of SCK outputs data.  
 When clear, rising edge of SCK outputs data.

Figure 9. Control Register 2

FREQ2	FREQ1	FREQ0	Sample Frequency
0	0	0	Out of Range
0	0	1	48kHz $\pm$ 4%
0	1	0	44.1 kHz $\pm$ 4%
0	1	1	32 kHz $\pm$ 4%
1	0	0	48 kHz $\pm$ 400 ppm
1	0	1	44.1 kHz $\pm$ 400 ppm
1	1	0	44.056 kHz $\pm$ 400 ppm
1	1	1	32 kHz $\pm$ 400 ppm

Table 2. Incoming Sample Frequency Bits

ROER, when set, causes the last audio sample to be reread if the error pin, ERF, is active. When out of lock, the CS8411 will output zeros if ROER is set and output random data if ROER is not set. The conditions that activate ERF are those reported in SR2 and enabled in IER2. Figure 10 illustrates the modes selectable by SDF2-SDF0 and FSF1-FSF0. MSTR, which in most applications will be set to one, determines whether FSYNC and SCK are outputs (MSTR =

1) or inputs (MSTR = 0). When FSYNC and SCK are inputs (slave mode) the audio data can be read twice or missed if the device controlling FSYNC and SCK is on a different time-base than the CS8411. If the audio data is read twice or missed, the SLIP bit in SR1 is set. SCED selects the SCK edge to output data on. SCED high causes data to be output on the falling edge, and SCED low causes data to be output on the rising edge.

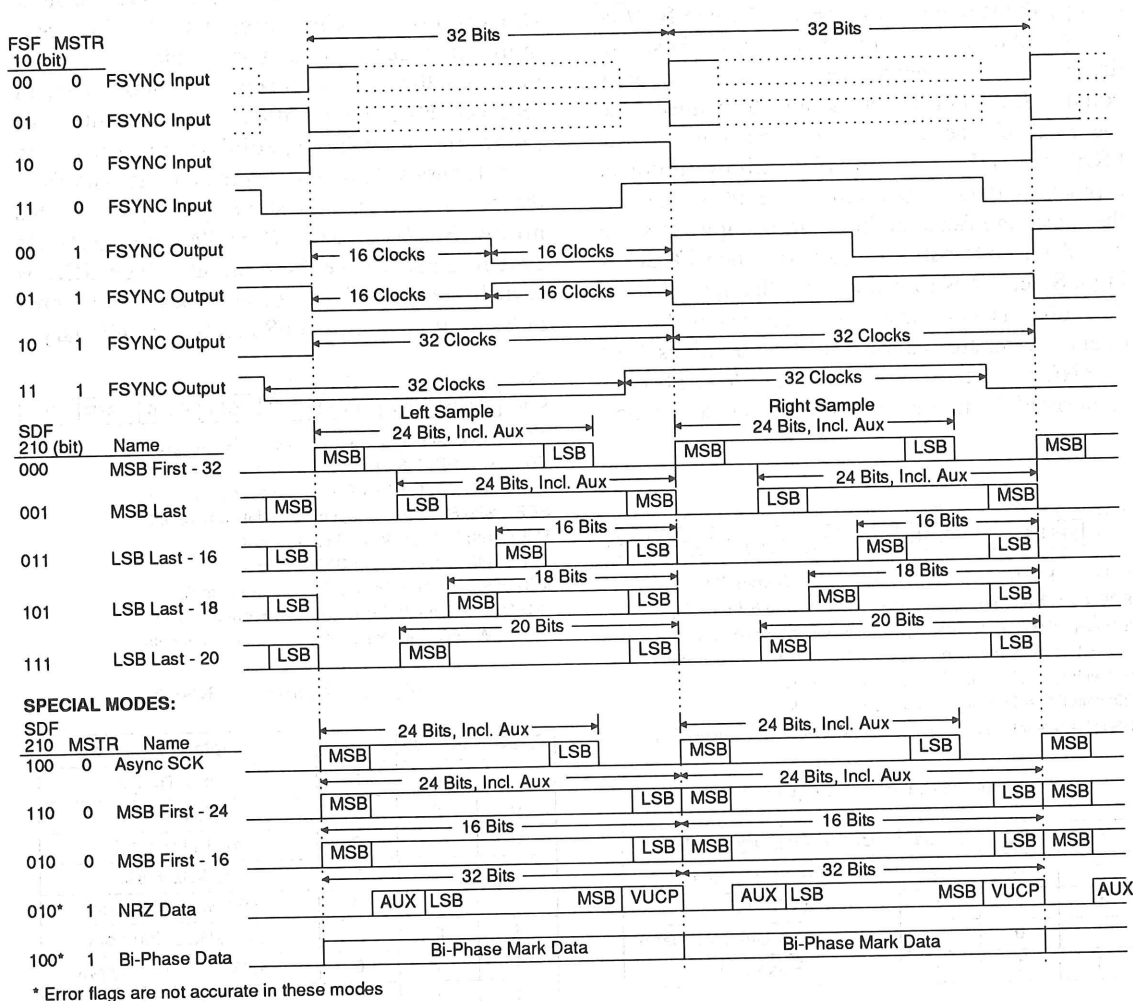


Figure 10. CS8411 Serial Port SDATA and FSYNC Timing



## Audio Serial Port

The audio serial port outputs the audio data portion from the received data and consists of three pins: SCK, SDATA, and FSYNC. SCK clocks the data out on the SDATA line. The edge that SCK uses to output data is programmable from CR2. FSYNC delineates the audio samples and may indicate the particular channel, left or right. Figure 10 illustrates the multitude of formats that SDATA and FSYNC can take.

### NORMAL MODES

SCK and FSYNC can be inputs ( $MSTR = 0$ ) or outputs ( $MSTR = 1$ ), and are usually programmed as outputs. As outputs, SCK contains 32 periods for each sample and FSYNC has four formats. The first two output formats of FSYNC (shown in Figure 10) delineate each word and the identification of the particular channel must be kept track of externally. This may be done using the rising edge of FLAG2 to indicate the next data word is left channel data. The last two output formats of FSYNC also delineate each channel with the polarity of FSYNC indicating the particular channel. The last format has FSYNC change one SCK cycle before the frame containing the data and may be used to generate an I<sup>2</sup>S compatible interface.

When SCK is programmed as an input, 32 SCK cycles per sample must be provided. (There are two formats in the *Special Modes* section where SCK can have 16 or 24 clocks per sample.) The four modes where FSYNC is an input are similar to the FSYNC output modes. The first two require a transition of FSYNC to start the sample frame, whereas the last two are identical to the corresponding FSYNC output modes. If the circuit generating SCK and FSYNC is not locked to the master clock of the CS8411, the serial port will eventually be reread or a sample will be missed. When this occurs, the SLIP bit in SR1 will be set.

SDATA can take on five formats in the normal serial port modes. The first format (see Figure 10), MSB First, has the MSB aligned with the start of a sample frame. Twenty-four audio bits are output including the auxiliary bits. This mode is compatible with many DSPs. If the auxiliary bits are used for something other than audio data, they must be masked off. The second format, MSB Last, outputs data LSB first with the MSB aligned to the end of the sample frame. This format is conducive to serial arithmetic. Both of the above formats output all audio bits from the received data. The last three formats are LSB Last formats that output the most significant 16, 18, and 20 bits respectively, with the LSB aligned to the end of the sample frame. These formats are used by many interpolation filters.

### SPECIAL MODES

Five special modes are included for unique applications. In these modes, the master bit, MSTR, must be defined as shown in Figure 10. In the first mode, Asynchronous SCK, FSYNC (which is an output in this mode) is aligned to the incoming SCK. This mode is useful when the SCK is locked to an external event and cannot be derived from MCK. Since SCK is asynchronous, the number of SCK cycles per sample frame will vary. The data output will be MSB first, 24 bits, and aligned to the beginning of a sample frame. The second and third special modes are unique in that they contain 24 and 16 SCK cycles respectively per sample frame, whereas all normal modes contain 32 SCK cycles. In these two modes, the data is MSB first and fills the entire frame. The fourth special mode outputs NRZ data including the V, U, C, and P bits and the preamble replaced with zeros. SCK is an output with 32 SCK cycles per sample frame. The fifth mode outputs the biphase data recovered from the transmission line with 64 SCK cycles output per sample frame, with data changing on the rising edge. The error codes are not accurate in the fourth and fifth special modes.



## Buffer Memory

In all buffer modes, the status, mask, and control registers are located at addresses 0-3, and the user data is buffered at locations 4 through 7. The parallel port can access any location in the user data buffer at any time; however, care should be taken not to read a location when that location is being updated internally. This internal writing is done through a second port of the buffer and is done in a cyclic manner. As data is received, the bits are assembled in an internal 8-bit shift register which, when full, is loaded into the buffer memory. The first bit received is stored in D0 and, after D7 is received, the byte is written into the proper buffer memory location.

The user data is received one bit per sub-frame. At the channel status block boundary, the internal pointer for writing user data is initialized to 04H (Hex). After receiving eight user bits, the byte is written to the address indicated by the user pointer which is then incremented to point to the next address. After receiving all four bytes of user data, 32 audio samples, the user pointer is set to 04H again and the cycle repeats. FLAG0, in SR1 can be used to monitor the user data buffer. When the last byte of the user buffer, location 07H, is written, FLAG0 is set low and when the second byte, location 05H, is written, FLAG0 is set high. If the corresponding bit in the interrupt enable register (IER1, bit 0) is set, a transition of FLAG0 will generate a low pulse on the interrupt pin. The level of FLAG0 indicates which two bytes the part will write next, thereby indicating which two bytes are free to be read.

FLAG1 is buffer mode dependent and is discussed in the individual buffer mode sections. A transition of FLAG1 will generate an interrupt if the appropriate interrupt enable bit is set.

FLAG2 is set high after channel status byte 23, the last byte of the block, is written and set low after channel status byte 3 is written to the buffer memory. FLAG2 is unique in that only the rising

edge can cause an interrupt if the appropriate interrupt enable bit in IER1 is set.

Figure 11 illustrates the flag timing for an entire channel status block which includes 24 bytes of channel status data per channel and 384 audio samples. The lower portion of Figure 11 expands the first byte of channel status showing eight pairs of data, with a pair defined as a frame. This is further expanded showing the first sub-frame (A0) to contain 32 bits defined as per the digital audio standards. When receiving stereo, channel A is left and channel B is right.

For all three buffer modes, the three most significant bits in SR1, shown in Figure 6, can be used to monitor the channel status data. In buffer mode 2, bits 7 and 6 change definition and are described in that section. Channel status data, as described in the standards, is independent for each channel. Each channel contains its own block of channel status data, and in most systems, both channels will contain the same channel status data. Buffer modes 0 and 1 operate on one block of channel status with the particular block selected by the CS2/CS1 bit in CR1. CSDIF, bit 7 in SR1, indicates when the channel status data for each channel is not the same even though only one channel is being buffered. CRCE, bit 6 in SR1, indicates a CRC error occurred in the buffered channel. CCHG, bit 5 in SR1, is set when any bit in the buffered channel status bytes 0 to 3, change from one block to the next.

## BUFFER MODE 0

The user data buffer previously described is identical for all modes. Buffer mode 0 allocates the rest of the buffer to channel status data. This mode stores an entire block of channel status in 24 memory locations from address 08H to 1FH. Channel status (CS) data is different from user data in that channel status data is independent for each channel. A block of CS data is defined as one bit per frame, not one bit per sub-frame; therefore, there are two blocks of channel status.

The CS2/CS1 bit in CR1 selects which channel is stored in the buffer. In a typical system sending stereo data, the channel status data for each channel would be identical.

FLAG1 in status register 1, SR1, can be used to monitor the channel status buffer. In mode 0, FLAG1 is set low after channel status byte 23 (the last byte) is written, and is set high when channel status byte 15, location 17H is written. If

the corresponding interrupt enable bit in IER1 is set, a transition of FLAG1 will generate a pulse on the interrupt pin. Figure 12 illustrates the memory write sequence for buffer mode 0 along with flag timing. The arrows on the flag timing indicate when an interrupt will occur if the appropriate interrupt enable bit is set. FLAG0 can cause an interrupt on either edge, which is only shown in the expanded portion of the figure for clarity.

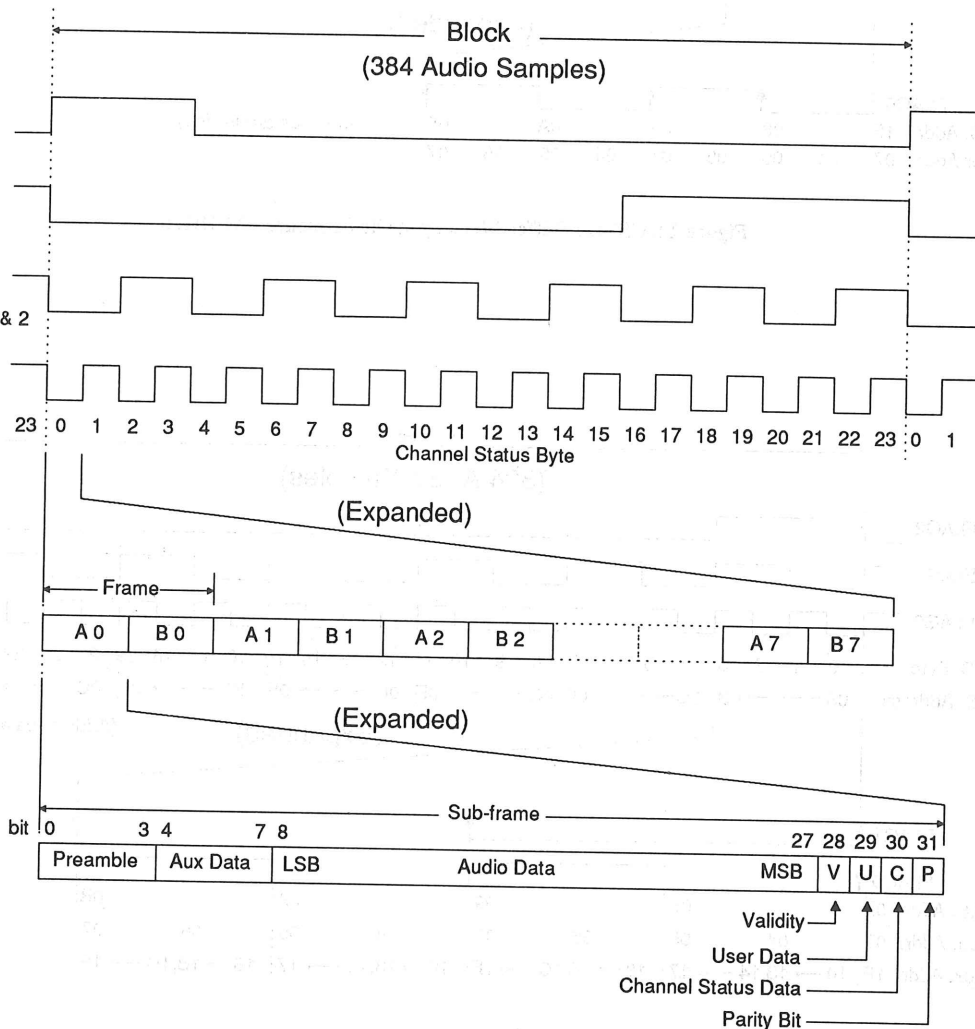


Figure 11. CS8411 Status Register Flag Timing

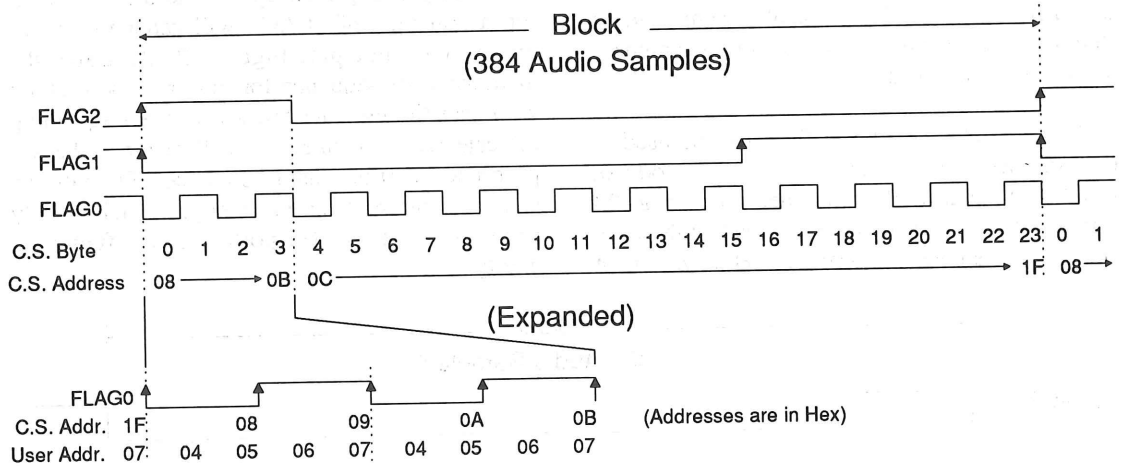


Figure 12. CS8411 Buffer Memory Write Sequence - MODE 0

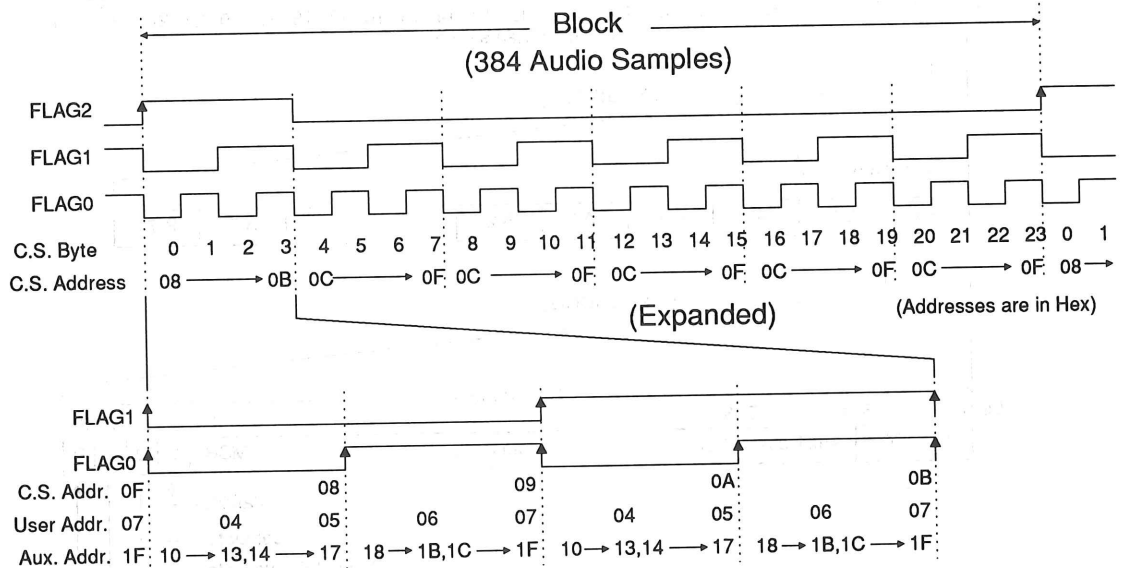


Figure 13. CS8411 Buffer Memory Write Sequence - MODE 1

### BUFFER MODE 1

In buffer mode 1, eight bytes are allocated for channel status data and sixteen bytes for auxiliary data as shown in Figure 5. The user data buffer is the same for all modes. The channel status buffer, locations 08H to 0FH, is divided into two sections. The first four locations always contain the first four bytes of channel status, identical to mode 0, and are written once per channel status block. The second four locations, addresses 0CH to 0FH, provide a cyclic buffer for the last 20 bytes of channel status data. The channel status buffer is divided in this fashion because the first four bytes are the most important ones; whereas, the last 20 bytes are often not used (except for byte 23, CRC).

FLAG1 and FLAG2 can be used to monitor this buffer as shown in Figure 13. FLAG1 is set high when CS byte 1, location 09H, is written and is toggled when every other byte is written. FLAG2 is set high after CS byte 23 is written and set low

after CS byte 3, location 0BH, is written. FLAG2 determines whether the channel status pointer is writing to the first four-byte section of the channel status buffer or the second four-byte section, while FLAG1 indicates which two bytes of the section are free to update.

The auxiliary data buffer, locations 10H to 1FH, is written to in a cyclic manner similar to the other buffers. Four auxiliary data bits are received per audio sample (sub-frame) and, since the auxiliary data is four times larger than the user data, the auxiliary data buffer on the CS8411 is four times larger allowing FLAG0 to be used to monitor both.

### BUFFER MODE 2

In buffer mode 2, two 8-byte buffers are available to independently buffer each channel of channel status data. Both buffers are identical to the channel status buffer in mode 1 and are written to simultaneously, with locations 08H to 0FH con-

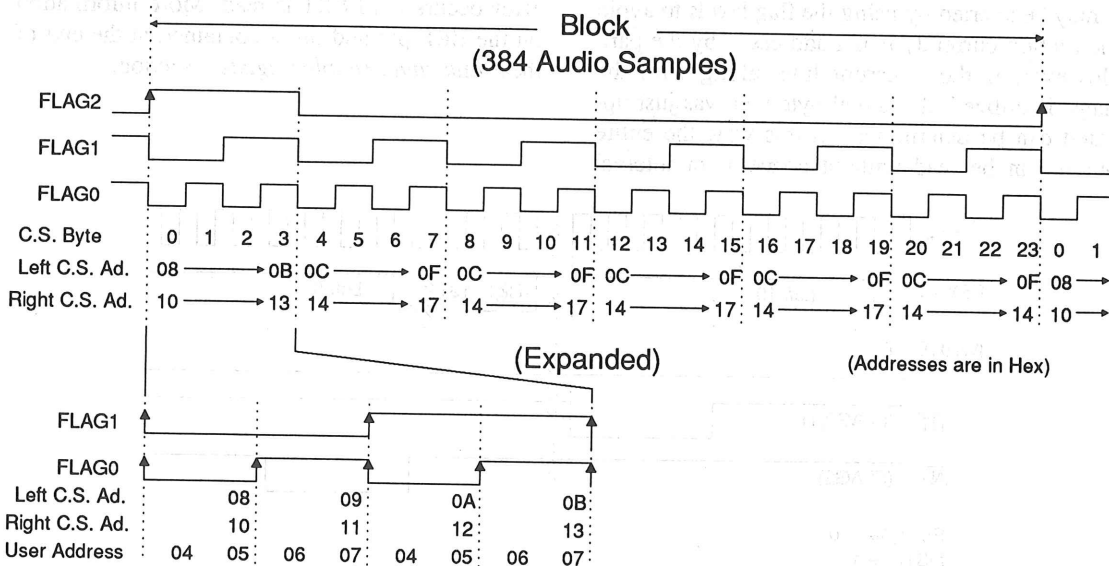


Figure 14. CS8411 Buffer Memory Write Sequence - MODE 2

taining CS data for channel A and locations 10H to 17H containing CS data for channel B. Both CS buffers can be monitored using FLAG1 and FLAG2 as described in the *BUFFER MODE 1* section.

The two most significant bits in SR1 change definition for buffer mode 2. These two bits, when set, indicate CRC errors for their respective channels. A CRC error occurs when the internal calculated CRC for channel status bytes 0 through 22 does not match channel status byte 23. CCHG, bit 5 in SR1, is set when any bit in the first four channel status bytes of either channel changes from one block to the next. Since channel status doesn't change very often, this bit may be monitored rather than checking all the bits in the first four bytes. These bits are illustrated in Figure 6.

### Buffer Updates and Interrupt Timing

As mentioned previously in the buffer mode sections, conflicts between externally reading the buffer RAM and the CS8411 internally writing to it may be averted by using the flag levels to avoid the section currently being addressed by the part. However, if the interrupt line, along with the flags, is utilized, the actual byte that was just updated can be determined. In this way, the entire buffer can be read without concern for internal

updates. Figure 15 shows the detailed timing for the interrupt line, flags, and the RAM write line. SCK is 64 times the incoming sample frequency, and is the same SCK output in master mode. The FSYNC shown is valid for all master modes except the I<sup>2</sup>S compatible mode. The interrupt pulse is shown to be 4 SCK periods wide and goes low 5 SCK periods after the RAM is written. Using the above information, the entire data buffer may be read starting with the next byte to be updated by the internal pointer.

### ERF Pin Timing

ERF signals that an error occurred while receiving the audio sample that is currently being read from the serial port. ERF changes with the active edge of FSYNC and is high during the errored sample. ERF is affected by the error conditions reported in SR2: CONF, LOCK, CODE, PARITY, and V. Any of these conditions may be masked off using the corresponding bits in IER2. The ERF pin will go high for each error that occurs. The ERF bit in SR1 is different from the ERF pin in that it only causes an interrupt the first time an error occurs until SR1 is read. More information on the ERF pin and bit is contained at the end of the *Status and IEnable Registers* section.

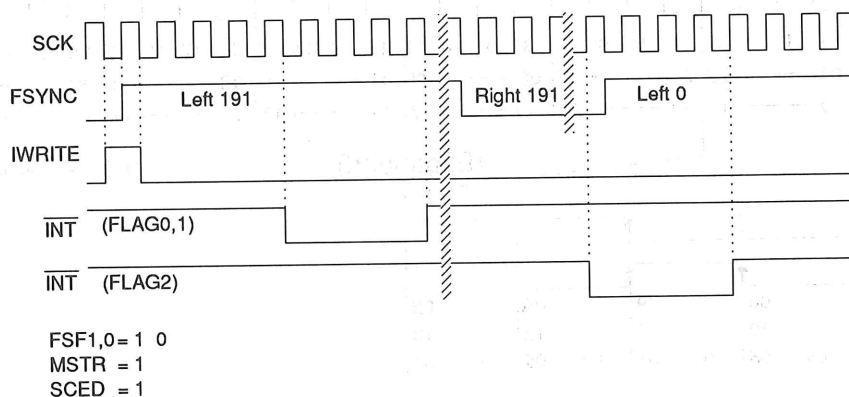


Figure 15. RAM/Buffer-Write and Interrupt Timing

### PIN DESCRIPTIONS:

#### CS8411

2

DATA BUS BIT 2	D2	1	28	D1	DATA BUS BIT 1
DATA BUS BIT 3	D3	2	27	D0	DATA BUS BIT 0
DATA BUS BIT 4	D4	3	26	SDATA	SERIAL OUTPUT DATA
DATA BUS BIT 5	D5	4	25	ERF	ERROR FLAG
DATA BUS BIT 6	D6	5	24	CS	CHIP SELECT
DATA BUS BIT 7	D7	6	23	RD/WR	READ/WRITE SELECT
DIGITAL POWER	VD+	7	22	VA+	ANALOG POWER
DIGITAL GROUND	DGND	8	21	AGND	ANALOG GROUND
RECEIVE POSITIVE	RXP	9	20	FILT	FILTER
RECEIVE NEGATIVE	RXN	10	19	MCK	MASTER CLOCK
FRAME SYNC	FSYNC	11	18	A0	ADDRESS BUS BIT 0
SERIAL DATA CLOCK	SCK	12	17	A1	ADDRESS BUS BIT 1
ADD BUS BIT 4 / FCLOCK	A4/FCK	13	16	A2	ADDRESS BUS BIT 2
INTERRUPT	INT	14	15	A3	ADDRESS BUS BIT 3

#### Power Supply Connections

##### VD+ - Positive Digital Power, PIN 7.

Positive supply for the digital section. Nominally +5 volts.

##### VA+ - Positive Analog Power, PIN 22.

Positive supply for the analog section. Nominally +5 volts. This supply should be as quiet as possible since noise on this pin will directly affect the jitter performance of the recovered clock.

##### DGND - Digital Ground, PIN 8.

Ground for the digital section. DGND should be connected to same ground as AGND.

##### AGND - Analog Ground, PIN 21.

Ground for the analog section. AGND should be connected to same ground as DGND.

#### Audio Output Interface

##### SCK - Serial Clock, PIN 12.

Serial clock for SDATA pin which can be configured (via control register 2) as an input or output, and can sample data on the rising or falling edge. As an input, SCK must contain 32 clocks for every audio sample in all normal audio serial port formats.

**FSYNC - Frame Sync, PIN 11.**

Delineates the serial data and may indicate the particular channel, left or right. Also, FSYNC may be configured as an input or output. The format is based on bits in control register 2.

**SDATA - Serial Data, PIN 26.**

Audio data serial output pin.

**ERF - Error Flag, PIN 25.**

Signals that an error has occurred while receiving the audio sample currently being read from the serial port. The errors that cause ERF to go high are enumerated in status register 2 and enabled by setting the corresponding bit in IEnable register 2.

**A4/FCK - Address Bus Bit 4/Frequency Clock, PIN 13.**

This pin has a dual function and is controlled by the FCEN bit in control register 1. A4 is the address bus pin as defined below. When used as FCK, an internal frequency comparator compares a 6.144 MHz clock input on this pin to the received clock frequency and stores the value in status register 1 as three FREQ bits. These bits indicate the incoming frequency as well as the tolerance. When defined as FCK, A4 is internally set to 0.

***Parallel Interface*** **$\overline{CS}$  - Chip Select, PIN 24.**

This input is active low and allows access to the 32 bytes of internal memory. The address bus and  $\overline{RD}/\overline{WR}$  must be valid while  $\overline{CS}$  is low.

 **$\overline{RD}/\overline{WR}$  - Read/Write, PIN 23.**

If  $\overline{RD}/\overline{WR}$  is low when  $\overline{CS}$  goes active (low), the data on the data bus is written to internal memory. If  $\overline{RD}/\overline{WR}$  is high when  $\overline{CS}$  goes active, the data in the internal memory is placed on the data bus.

**A4-A0 - Address Bus, PINS 13, 15-18.**

Parallel port address bus that selects the internal memory location to be read from or written to. Note that A4 is the dual function pin A4/FCK as described above.

**D0-D7 - Data Bus, PINS 27-28, 1-6.**

Parallel port data bus used to check status, read or write control words, or read internal buffer memory.



## **$\overline{\text{INT}}$ - Interrupt, PIN 14.**

Open drain output that can signal the state of the internal buffer memory as well as error information. A 5k $\Omega$  resistor to VD+ is typically used to support logic gates. All bits affecting  $\overline{\text{INT}}$  are maskable to allow total control over the interrupt mechanism.

2

## **Receiver Interface**

### **RXP, RXN - Differential Line Receivers, PINS 9, 10.**

RS422 compatible line receivers. Described in detail in Appendix A.

## **Phase Locked Loop**

### **MCK - Master Clock, PIN 19.**

Low jitter clock output of 256 times the received sample frequency.

### **FILT - Filter, PIN 20.**

An external 1k $\Omega$  resistor and 0.047 $\mu\text{F}$  capacitor are required from the FILT pin to analog ground.



## CS8412 DESCRIPTION

The CS8412 does not need a microprocessor to handle the non-audio data (although a micro may be used with the C and U serial ports). Instead, dedicated pins are available for the most important channel status bits. The CS8412 is a monolithic CMOS circuit that receives and decodes digital audio data which was encoded according to the digital audio interface standards. It contains an RS422 line receiver and clock and data recovery utilizing an on-chip phase-locked loop. The audio data is output through a configurable serial port that supports 14 formats. The channel status and user data have their own serial pins and the validity flag is OR'ed with the ERF flag to provide a single pin, VERF, indicating that

the audio output may not be valid. This pin may be used by interpolation filters that provide error correction. A block diagram of the CS8412 is illustrated in Figure 16.

The line receiver and jitter performance are described in the sections directly preceding the CS8411 sections in the beginning of this data sheet.

### Audio Serial Port

The audio serial port is used primarily to output audio data and consists of three pins: SCK, FSYNC, and SDATA. These pins are configured via four control pins: M0, M1, M2, and M3. M3 selects between eight normal serial formats (M3 = 0), and six special formats (M3 = 1).

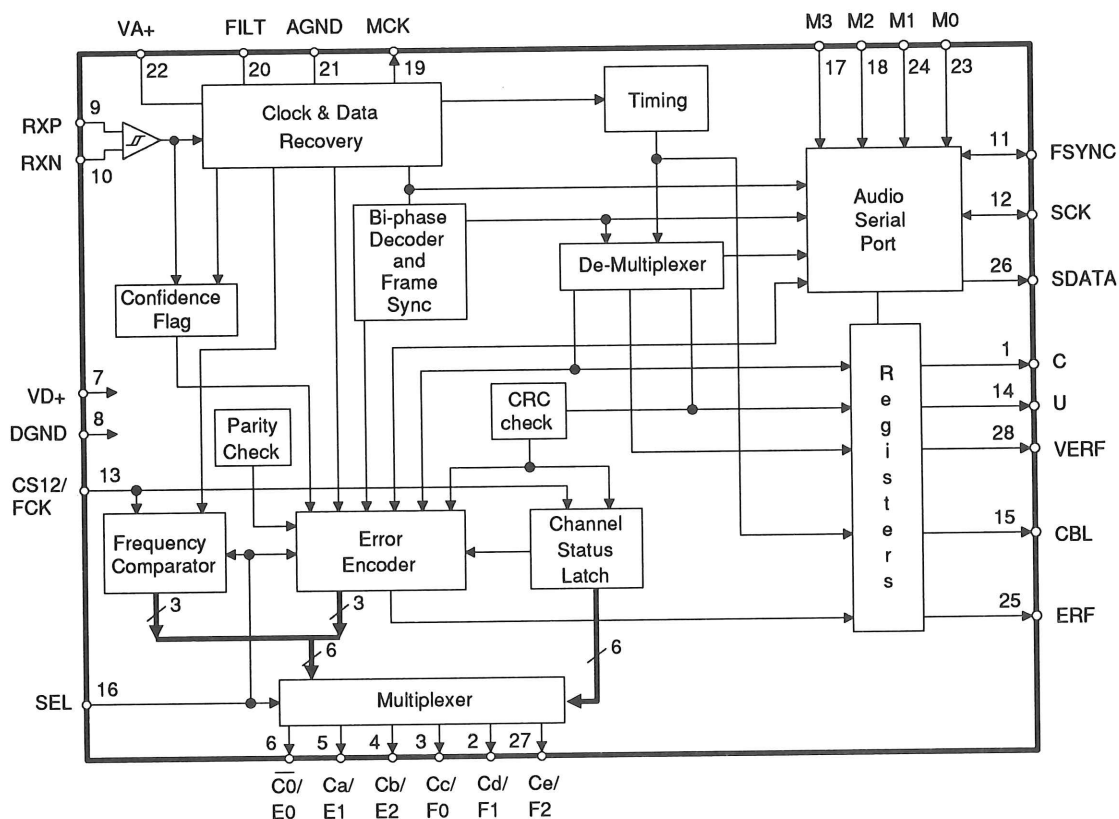


Figure 16. CS8412 Block Diagram

### NORMAL MODES ( $M3 = 0$ )

When  $M3$  is low, the normal serial port formats shown in Figure 17 are selected using  $M2$ ,  $M1$ , and  $M0$ . These formats are also listed in Table 3, wherein the first word past the format number (Out-In) indicates whether FSYNC and SCK are outputs from the CS8412 or are inputs. The next word (L/R-WSYNC) indicates whether FSYNC indicates the particular channel or just delineates each word. If an error occurs ( $ERF = 1$ ) while using one of these formats, the previous valid audio data for that channel will be output. As long as  $ERF$  is high, that same data word will be output. If the CS8412 is not locked, it will output all zeroes. In some modes FSYNC and SCK are outputs and in others they are inputs. In Table 3, LSBJ is short for *LSB justified* where the LSB is justified to the end of the audio frame and the MSB varies with word length. As outputs the CS8412 generates 32 SCK periods per audio sample (64 per stereo sample) and, as inputs, 32 SCK periods must be provided per audio sample. When FSYNC and SCK are inputs, one stereo sample is double buffered. For those modes which output 24 bits of audio data, the auxiliary bits will be included. If the auxiliary bits are not used for audio data, they must be masked off.

### SPECIAL MODES ( $M3 = 1$ )

When  $M3$  is high, the special audio modes described in Table 4 are selected via  $M2$ ,  $M1$ , and  $M0$ . In formats 8, 9, and 10, SCK, FSYNC, and

SDATA are the same as in formats 0, 1, and 2 respectively; however, the recovered data is output as is even if  $ERF$  is high, indicating an error. (In modes 0-2 the previous valid sample is output.) Similarly, when out of lock, the CS8412 will still output all the recovered data, which should be zeros if there is no input to the RXP, RXN pins. Format 11 is similar to format 0 except that SCK is an input and FSYNC is an output. In this mode FSYNC and SDATA are synchronized to the incoming SCK, and the number of SCK periods between FSYNC edges will vary since SCK is not synchronous to received data stream. This mode may be useful when writing data to storage. Format 12 is similar to format 7 except that SDATA is the entire data word received from the transmission line including the C, U, V, and P bits, with zeros in place of the preamble. In format 13 SDATA contains the entire biphase encoded data from the transmission line including the preamble, and SCK is twice the normal frequency. Figure 18 illustrates formats 12 and 13. Format 14 is reserved and not presently used, and format 15 causes the CS8412 to go into a reset state. While in reset all outputs will be inactive except MCK. The CS8412 comes out of reset at the first block boundary after leaving the reset state.

### C, U, V, ERF, and CBL Serial Outputs

The C and U bits and CBL are output one SCK period prior to the active edge of FSYNC in all serial port formats except 2 and 3 ( $I^2S$  modes). The active edge of FSYNC may be used to latch

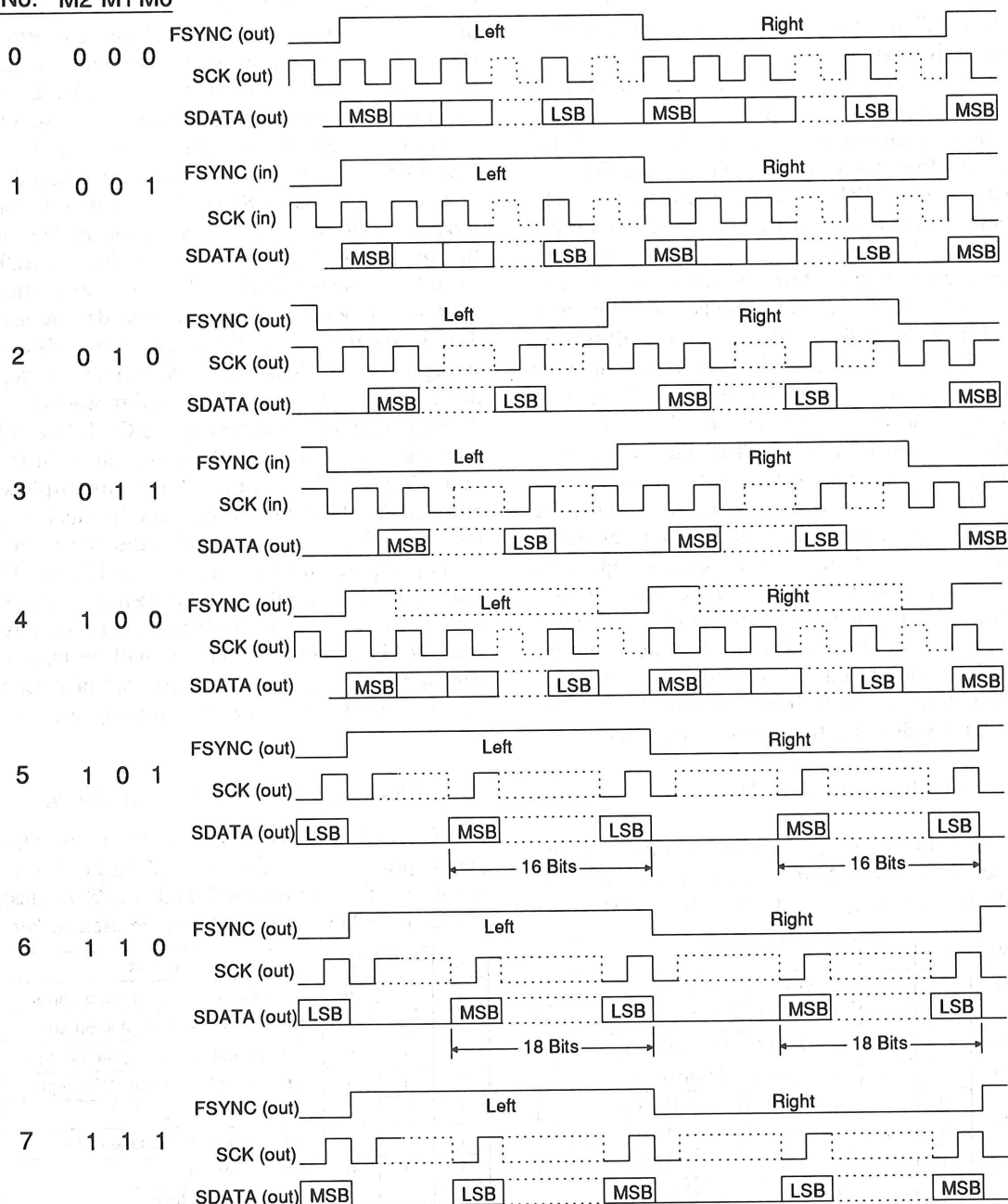
M2	M1	M0	Format
0	0	0	0 - Out, L/R, 16-24 Bits
0	0	1	1 - In, L/R, 16-24 Bits
0	1	0	2 - Out, L/R, $I^2S$ Compatible
0	1	1	3 - In, L/R, $I^2S$ Compatible
1	0	0	4 - Out, WSYNC, 16-24 Bits
1	0	1	5 - Out, L/R, 16 Bits LSBJ
1	1	0	6 - Out, L/R, 18 Bits LSBJ
1	1	1	7 - Out, L/R, MSB Last

Table 3. Normal Audio Port Modes ( $M3=0$ )

M2	M1	M0	Format
0	0	0	8 - Format 0 - No repeat on error
0	0	1	9 - Format 1 - No repeat on error
0	1	0	10 - Format 2 - No repeat on error
0	1	1	11 - Format 0 - Async. SCK input
1	0	0	12 - Received NRZ Data
1	0	1	13 - Received Bi-phase Data
1	1	0	14 - Reserved
1	1	1	15 - CS8412 Reset

Table 4. Special Audio Port Modes ( $M3=1$ )

FMT  
No. M2 M1 M0



**Figure 17. CS8412 Audio Serial Port Formats**

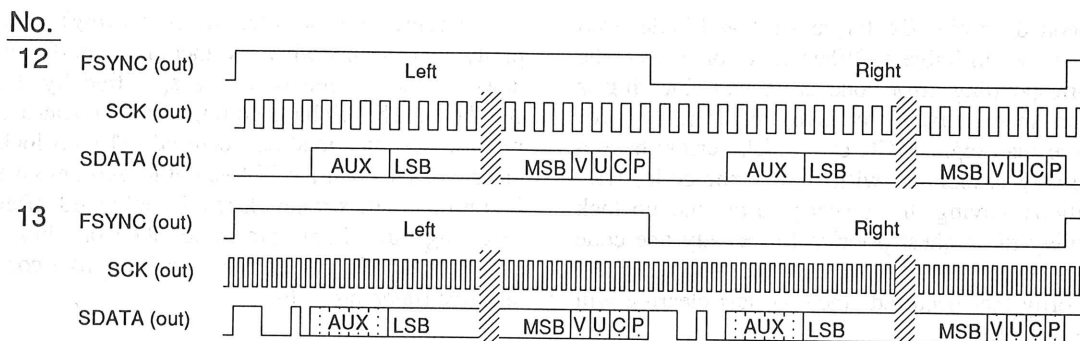


Figure 18. Special Audio Port Formats 12 and 13

C, U, and CBL externally. In formats 2 and 3, the C and U bits and CBL are updated with the active edge of FSYNC. The validity + error flag (VERF) and the error flag (ERF) are always updated at the active edge of FSYNC. This timing is illustrated in Figure 19.

The C output contains the channel status bits with CBL rising indicating the start of a new channel status block. CBL is high for the first four bytes of channel status (32 frames or 64 samples) and low for the last 20 bytes of channel status (160 frames or 320 samples). The U output contains the User Channel data. The V bit is OR'ed with the ERF flag and output on the VERF pin. This indicates that the audio sample may be in error and can be used by interpolation filters to

interpolate through the error. ERF being high indicates a serious error occurred on the transmission line. There are three errors that cause ERF to go high: a parity error or biphas coding violation during that sample, or an out of lock PLL receiver. Timing for the above pins is illustrated in Figure 19.

### Multifunction Pins

There are seven multifunction pins which contain either error and received frequency information, or channel status information, selectable by SEL.

### ERROR AND FREQUENCY REPORTING

When SEL is low, error and received frequency information are selected. The error information is

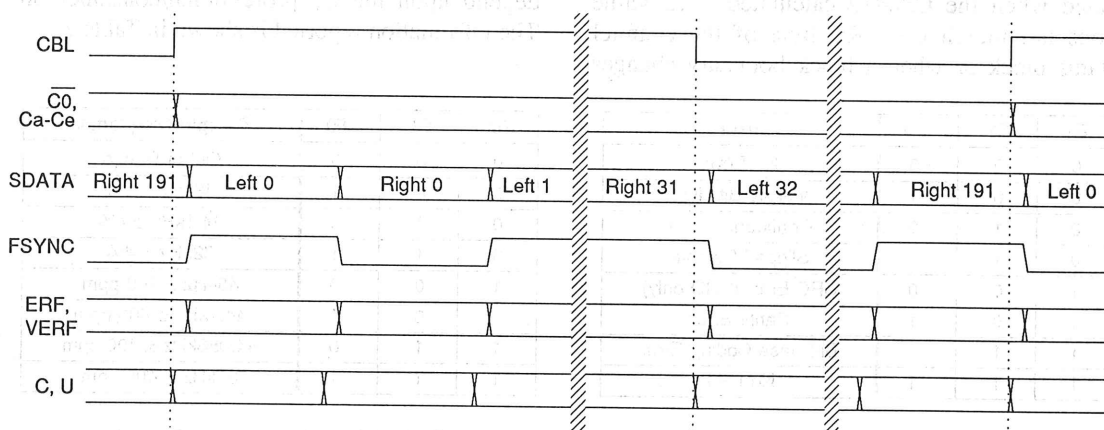


Figure 19. CBL Timing

encoded on pins E2, E1, and E0, and is decoded as shown in Table 5. When an error occurs, the corresponding error code is latched. Clearing is then accomplished by bringing SEL high for more than eight MCK cycles. The errors have a priority associated with their error code, with validity having the lowest priority and no lock having the highest priority. Since only one code can be displayed, the error with the highest priority that occurred since the last clearing will be selected.

The validity flag indicates that the validity bit for a previous sample was high since the last clearing of the error codes. The confidence flag occurs when the received data eye opening is less than half a bit period. This indicates that the quality of the transmission link is poor and does not meet the digital audio interface standards. The slipped sample error can only occur when FSYNC and SCK of the audio serial port are inputs. In this case, if FSYNC is asynchronous to the received data rate, periodically a stereo sample will be dropped or reread depending on whether the read rate is slower or faster than the received data rate. When this occurs, the slipped sample error code will appear on the 'E' pins. The CRC error is updated at the beginning of a channel status block, and is only valid when the professional format of channel status data is received. This error is indicated when the CS8412 calculated CRC value does not match the CRC byte of the channel status block or when a block boundary changes

(as in removing samples while editing). The parity error occurs when the incoming sub-frame does not have even parity as specified by the standards. The biphase coding error indicates a biphase coding violation occurred. The no lock error indicates that the PLL is not locked onto the incoming data stream. Lock is achieved after receiving three frame preambles then one block preamble, and is lost after not receiving four consecutive frame preambles.

The received frequency information is encoded on pins F2, F1, and F0, and is decoded as shown in Table 6. The on-chip frequency comparator compares the received clock frequency to an externally supplied 6.144 MHz clock which is input on the FCK pin. The 'F' pins are updated three times during a channel status block including prior to the rising edge of CBL. CBL may be used to externally latch the 'F' pins. The clock on FCK must be valid for two thirds of a block for the 'F' pins to be accurate.

#### CHANNEL STATUS REPORTING

When SEL is high, channel status is displayed on C0, and Ca-Ce for the channel selected by CS12. If CS12 is low, channel status for sub-frame 1 is displayed, and if CS12 is high, channel status for sub-frame 2 is displayed. The contents of Ca-Ce depend upon the C0 professional/consumer bit. The information reported is shown in Table 7.

E2	E1	E0	Error
0	0	0	No Error
0	0	1	Validity Bit High
0	1	0	Confidence Flag
0	1	1	Slipped Sample
1	0	0	CRC Error (PRO only)
1	0	1	Parity Error
1	1	0	Bi-Phase Coding Error
1	1	1	No Lock

Table 5. Error Decoding

F2	F1	F0	Sample Frequency
0	0	0	Out of Range
0	0	1	48kHz $\pm$ 4%
0	1	0	44.1kHz $\pm$ 4%
0	1	1	32kHz $\pm$ 4%
1	0	0	48kHz $\pm$ 400 ppm
1	0	1	44.1kHz $\pm$ 400 ppm
1	1	0	44.056kHz $\pm$ 400 ppm
1	1	1	32kHz $\pm$ 400 ppm

Table 6. Sample Frequency Decoding

## Professional Channel Status ( $\overline{C0} = 0$ )

When  $\overline{C0}$  is low, the received channel status block is encoded according to the professional/broadcast format. The Ca through Ce pins are defined for some of the more important professional bits. As listed in Table 7, Ca is the inverse of channel status bit 1. Therefore, if the incoming channel status bit 1 is 1, Ca, defined as  $\overline{C1}$ , will be 0.  $\overline{C1}$  indicates whether audio ( $\overline{C1} = 1$ ) or non-audio ( $\overline{C1} = 0$ ) data is being received. Cb and Cc, defined as EM0 and EM1 respectively, indicate emphasis and are encoded versions of channel status bits 2, 3, and 4. The decoding is listed in Table 8. Cd, defined as  $\overline{C9}$ , is the inverse of channel status bit 9, which gives some indication of channel mode. (Bit 9 is also defined as bit 1 of byte 1.) When Ce, defined as  $\overline{CRCE}$ , is low, the CS8412 calculated CRC value does not match the received CRC value. This signal may be used to qualify Ca through Cd. If Ca through Ce are being displayed, Ce going low can indicate not to update the display.

## Consumer Channel Status ( $\overline{C0} = 1$ )

When  $\overline{C0}$  is high, the received channel status block is encoded according to the consumer format. In this case Ca through Ce are defined differently as shown in Table 7. Ca is the inverse of channel status bit 1,  $\overline{C1}$ , indicating audio ( $\overline{C1} = 1$ ) or non-audio ( $\overline{C1} = 0$ ). Cb is defined as the inverse of channel status bit 2,  $\overline{C2}$ , which indicates copy inhibit/copyright information. Cc, defined as  $\overline{C3}$ , is the emphasis bit of channel status, with  $\overline{C3}$  low indicating the data has had pre-emphasis added.

Pin	Professional	Consumer
$\overline{C0}$	0 (low)	1 (high)
Ca	$\overline{C1}$	$\overline{C1}$
Cb	EM0	$\overline{C2}$
Cc	EM1	$\overline{C3}$
Cd	$\overline{C9}$	ORIG
Ce	$\overline{CRCE}$	IGCAT

Table 7. Channel Status Pins

The audio standards, in consumer mode, describe bit 15, L, as the generation status which indicates whether the audio data is an original work or a copy (1st generation or higher). The definition of the L bit is reversed for three category codes: two broadcast codes, and laser-optical (CD's). Therefore, to interpret the L bit properly, the category code must be decoded. The CS8412 does this decoding internally and provides the ORIG signal that, when high, indicates that the audio data is original over all category codes.

## SCMS

The consumer audio standards also mention a serial copy management system, SCMS, for dealing with copy protection of copyrighted works. SCMS is designed to allow unlimited duplication of the original work, but no duplication of any copies of the original. This system utilizes the channel status bit 2, Copy, and channel status bit 15, L or generation status, along with the category codes. If the Copy bit is 0, copyright protection is asserted over the material. Then, the L bit is used to determine if the material is an original or a duplication. (As mentioned in the previous paragraph, the definition of the L bit can be reversed based on the category codes.) There are two category codes that get special attention: general and A/D converters without C or L bit information. For these two categories the SCMS standard requires that equipment interfacing to these categories set the C bit to 0 (copyright protection asserted) and the L bit to 1 (original). To support this feature, Ce, in the consumer mode, is defined as IGCAT (ignorant category) which is high for the "general" (0000000) and "A/D converter without copyright information" (01100xx) categories.

EM1	EM0	C2	C3	C4
0	0	1	1	1
0	1	1	1	0
1	0	1	0	0
1	1	0	0	0

Table 8. Emphasis Encoding



## PIN DESCRIPTIONS:

### CS8412

CHANNEL STATUS OUTPUT	<b>C</b>	1	28	<b>VERF</b>	VALIDITY + ERROR FLAG
CS d / FREQ REPORT 1	<b>Cd/F1</b>	2	27	<b>Ce/F2</b>	CS e / FREQ REPORT 2
CS c / FREQ REPORT 0	<b>Cc/F0</b>	3	26	<b>SDATA</b>	SERIAL OUTPUT DATA
CS b / ERROR CONDITION 2	<b>Cb/E2</b>	4	25	<b>ERF</b>	ERROR FLAG
CS a / ERROR CONDITION 1	<b>Ca/E1</b>	5	24	<b>M1</b>	SERIAL PORT MODE SELECT 1
CS 0 / ERROR CONDITION 0	<b>C0/E0</b>	6	23	<b>M0</b>	SERIAL PORT MODE SELECT 2
DIGITAL POWER	<b>VD+</b>	7	22	<b>VA+</b>	ANALOG POWER
DIGITAL GROUND	<b>DGND</b>	8	21	<b>AGND</b>	ANALOG GROUND
RECEIVE POSITIVE	<b>RXP</b>	9	20	<b>FILT</b>	FILTER
RECEIVE NEGATIVE	<b>RXN</b>	10	19	<b>MCK</b>	MASTER CLOCK
FRAME SYNC	<b>FSYNC</b>	11	18	<b>M2</b>	SERIAL PORT MODE SELECT 2
SERIAL DATA CLOCK	<b>SCK</b>	12	17	<b>M3</b>	SERIAL PORT MODE SELECT 3
CHANNEL SELECT / FCLOCK	<b>CS12/FCK</b>	13	16	<b>SEL</b>	FREQ/CS SELECT
USER DATA OUTPUT	<b>U</b>	14	15	<b>CBL</b>	CS BLOCK START

### Power Supply Connections

#### VD+ - Positive Digital Power, PIN 7.

Positive supply for the digital section. Nominally +5 volts.

#### VA+ - Positive Analog Power, PIN 22.

Positive supply for the analog section. Nominally +5 volts.

#### DGND - Digital Ground, PIN 8.

Ground for the digital section. DGND should be connected to same ground as AGND.

#### AGND - Analog Ground, PIN 21.

Ground for the analog section. AGND should be connected to same ground as DGND.

### Audio Output Interface

#### SCK - Serial Clock, PIN 12.

Serial clock for SDATA pin which can be configured (via the M0, M1, M2, and M3 pins) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will generate 32 clocks for every audio sample. As an input, 32 SCK periods per audio sample must be provided in all normal modes.

#### FSYNC - Frame Sync, PIN 11.

Delineates the serial data and may indicate the particular channel, left or right, and may be an input or output. The format is based on M0, M1, M2, and M3 pins.

**SDATA - Serial Data, PIN 26.**

Audio data serial output pin.

**M0, M1, M2, M3 - Serial Port Mode Select, PINS 23, 24, 18, 17.**

Selects the format of FSYNC and the sample edge of SCK with respect to SDATA. M3 selects between eight normal modes (M3 = 0), and six special modes (M3 = 1).

**Control Pins****VERF - Validity + Error Flag, PIN 28.**

A logical OR'ing of the validity bit from the received data and the error flag. May be used by interpolation filters to interpolate through errors.

**U - User Bit, PIN 14.**

Received user bit serial output port. FSYNC may be used to latch this bit externally.

**C - Channel Status Output, PIN 1.**

Received channel status bit serial output port. FSYNC may be used to latch this bit externally.

**CBL - Channel Status Block Start, PIN 15.**

The channel status block output is high for the first four bytes of channel status and low for the last 16 bytes.

**SEL - Select, PIN 16.**

Control pin that selects either channel status information or error and frequency information to be displayed on six of the following pins.

 **$\overline{C0}$ , Ca, Cb, Cc, Cd, Ce - Channel Status Output Bits, PINS 2-6, 27.**

These pins are dual function with the 'C' bits selected by bring SEL high. Channel status information is displayed for the channel selected by CS12.  $\overline{C0}$ , which is channel status bit 0, defines professional ( $\overline{C0} = 0$ ) or consumer ( $\overline{C0} = 1$ ) mode and further controls the definition of the Ca-Ce pins. These pins are updated with the rising edge of CBL.

**CS12 - Channel Select, PIN 13.**

This pin is also dual function and is selected by bringing SEL high. CS12 selects sub-frame 1 (when low) or sub-frame 2 (when high) to be displayed by channel status pins  $\overline{C0}$  and Ca through Ce.

**FCK - Frequency Clock, PIN 13.**

Frequency Clock input that is enabled by bringing SEL low. FCK is compared to the received clock frequency with the value displayed on F2 through F0. Nominal input value is 6.144 MHz.

**E0, E1, E2 - Error Condition, PINS 4-6.**

Encoded error information that is enabled by bringing SEL low. The error codes are prioritized and latched so that the error code displayed is the highest level of error since the last clearing of the error pins. Clearing is accomplished by bring SEL high for more than 8 MCK cycles.

**F0, F1, F2 - Frequency Reporting Bits, PINS 2-3, 27.**

Encoded sample frequency information that is enabled by bringing SEL low. Must have proper clock on FCK for at least one full channel status block for these pins to be valid. They are updated three times per block.

**ERF - Error Flag, PIN 25.**

Signals that an error has occurred while receiving the audio sample currently being read from the serial port. Three errors cause ERF to go high: a parity or biphase coding violation during the current sample, or an out of lock PLL receiver.

***Receiver Interface*****RXP, RXN - Differential Line Receivers, PINS 9, 10.**

RS422 compatible line receivers.

***Phase Locked Loop*****MCK - Master Clock, PIN 19.**

Low jitter clock output of 256 times the received sample frequency.

**FILT - Filter, PIN 20.**

An external 1k $\Omega$  resistor and 0.05 $\mu$ F capacitor is required from FILT pin to analog ground.

### APPENDIX A: RS422 Receiver Information

The RS422 receivers on the CS8411 and CS8412 are designed to receive both the professional and consumer interfaces, and meet all specifications listed in the digital audio standards. Figure A1 illustrates the internal schematic of the receiver portion of both chips. The receiver has a differential input. A Schmitt trigger is incorporated to add hysteresis which prevents noisy signals from corrupting the phase detector.

#### Professional Interface

The digital audio specifications for professional use call for a balanced receiver, using XLR connectors, with  $110\Omega \pm 20\%$  impedance. (The XLR connector on the receiver should have female pins with a male shell.) Since the receiver has a very high impedance, a  $110\Omega$  resistor should be placed across the receiver terminals to match the line impedance, as shown in Figure A2, and, since the part has internal biasing, no external biasing network is needed. If some isolation is desired without the use of transformers, a  $0.01\mu\text{F}$  capacitor should be placed on the input of each pin (RXP and RXN) as shown in Figure A3. However, if transformers are not used, high frequency energy could be coupled between transmitter and receiver causing degradation in analog performance. Although transformers are not required by AES they are strongly recommended. The EBU requires transformers. Figures A2 and A3 show an optional DC blocking capacitor on the transmission line. A  $0.1$  to  $0.47\mu\text{F}$  ceramic capacitor may be used to block any DC voltage that is accidentally connected to the digital audio receiver. The use of this capacitor is an issue of robustness as the digital audio transmission line does not have a DC voltage component.

#### Consumer Interface

In the case of the consumer interface, the standards call for an unbalanced circuit having a

receiver impedance of  $75\Omega \pm 5\%$ . The connector for the consumer interface is an RCA phono plug (fixed socket described in Table IV of IEC 268-11). The receiver circuit for the consumer interface is shown in Figure A4.

#### TTL/CMOS Levels

The circuit shown in Figure A5 may be used when external RS422 receivers or TTL/CMOS logic drive the CS8411/12 receiver section.

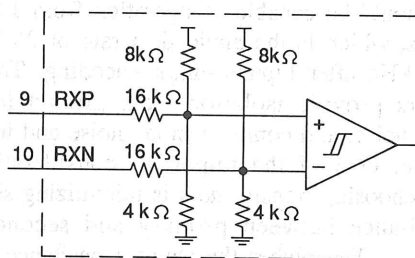


Figure A1. RS422 Receiver Internal Circuit

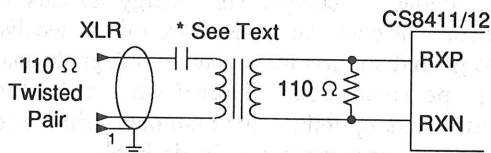


Figure A2. Professional Input Circuit

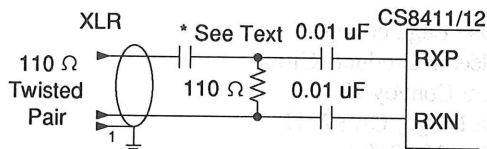


Figure A3. Transformerless Professional Circuit

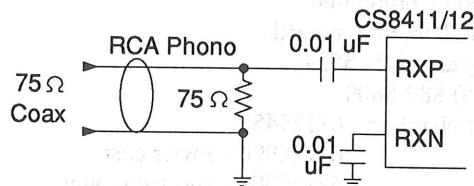
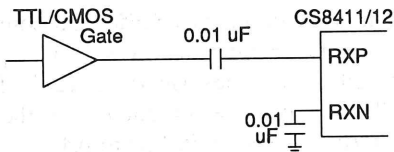


Figure A4. Consumer Input Circuit



**Figure A5. TTL/CMOS Interface**

Scientific Conversions Inc.

2800 Third Street

San Francisco, CA 94107

(415) 821-6464

Part Number: SC916-01 - single shield.

### **Transformers**

The transformer used in the professional interface should be capable of operation from 1.5 to 7 MHz, which is the audio data rate of 25 kHz to 55 kHz after biphasemark encoding. Transformers provide isolation from ground loop, 60 Hz noise, and common mode noise and interference. One of the important considerations when choosing transformers is minimizing shunt capacitance between primary and secondary windings. The higher the shunt capacitance, the lower the isolation between primary and secondary and the more coupling that can occur for high frequency energy. This energy appears in the form of common mode noise on the receive side ground and has the potential to degrade analog performance. Therefore, shielded transformers optimized for minimum primary to secondary capacitance may be desirable.

The following are a few typical transformers:

Pulse Engineering  
Telecom Products Group  
7250 Convoy Ct.  
San Diego, CA 92111  
(619) 268-2400  
Part Number: PE65612

Schott Corporation  
1000 Parkers Lane Rd.  
Wayzata, MN 55391  
(615) 889-8800  
Part Number: 67125450  
67128990 - lower cost  
67129000 - surface mount  
67129600 - single shield

## ORDERING GUIDE

Model	Temperature Range	Package
CS8411-CP	0 to 70 °C*	28-Pin Plastic .6" DIP
CS8411-IP	-40 to 85 °C	28-Pin Plastic .6" DIP
CS8411-CS	0 to 70 °C*	28-Pin Plastic SOIC
CS8411-IS	-40 to 85 °C	28-Pin Plastic SOIC
CS8412-CP	0 to 70 °C*	28-Pin Plastic .6" DIP
CS8412-IP	-40 to 85 °C	28-Pin Plastic .6" DIP
CS8412-CS	0 to 70 °C*	28-Pin Plastic SOIC
CS8412-IS	-40 to 85 °C	28-Pin Plastic SOIC

\* Although the '-CP' and '-CS' suffixed parts are guaranteed to operate over 0 to 70 °C, they are tested at 25 °C only. If testing over temperature is desired, the '-IP' and '-IS' suffixed parts are tested over their specified temperature range.

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## A-LAN - Audio Local Area Network Transceiver

### Features

- Monolithic Digital Audio Transceiver
- Supports S/PDIF Format
- System Messages are Communicated via User Channel
- Configurable Interface Port Supports I<sup>2</sup>C Bus, Parallel Interface, or the CS8425 Operates as Stand Alone Unit
- Up to Eight Nodes per Network
- Also Applicable as General Purpose Transceiver
- Unlimited Number of Nodes per Network

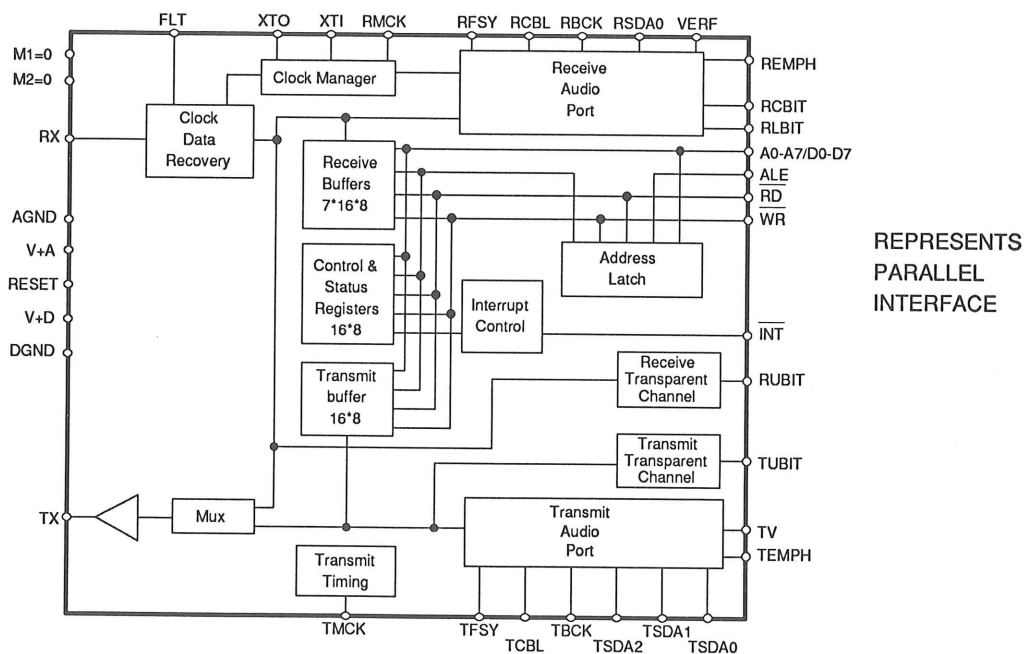
### General Description

The A-LAN chip is a monolithic CMOS circuit that implements the physical layer of an Audio Local Area Network. Nodes in the network can include CD players, digital equalizers, digitized cassette decks, tuners, amplifiers, etc. Intranetwork information is passed via the user channel.

Audio data is transmitted using the Sony/Phillips Digital Interface Format (S/PDIF), and can be generated by any one of multiple nodes on the A-LAN. The A-LAN is configured in a ring topology. External drivers and receivers are required for interface to the transmission media.

### ORDERING INFORMATION

Contact Crystal Semiconductor



### Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation  
P.O. Box 17847, Austin, TX 78760  
(512) 445 7222 Fax: (512) 445 7581

APR '92  
DS93PP1  
2-295

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## INTRODUCTION

Using SMART Analog technology, Crystal Semiconductor has created a family of CMOS A/D Converters which feature patented on-chip, self-calibrating architectures to maintain accuracy and linearity over their full temperature range and device lifetime. Each of our A/D Converters features an on-chip sample and hold, and is manufactured in low-power CMOS. Most devices include a power-down sleep mode.

### **CS5012A, CS5014, CS5016 SAR Family**

The CS5012A, CS5014 and CS5016 converters have 12, 14 & 16 bits of resolution respectively, with conversion times of 7  $\mu$ s to 16  $\mu$ s. The converters are tested for static and dynamic performance, at full rated conversion speed. On-chip self-calibration ensures that linearity, offset and full-scale errors remain with specification, with no missing codes. Specifications are maintained over the full temperature range.

### **CS5030, CS5031, CS5032**

Crystal's new family of 400 kHz, 12-bit ADC's offer on-chip sample/hold and on-chip reference. Superb initial accuracy, along with good temperature stability, eases error budgets. These low cost ADC's are ideal for 12-bit resolution applications.

### **CS5101A, CS5126 16-bit 100 kHz ADC**

The CS5101A is a 16-bit ADC capable of converting in 8  $\mu$ s, yielding sample rates of 100 kHz. A 2-channel analog input mux is included. Output data is available serially, with 4 interface modes. An on-chip crystal oscillator is provided, along with a power-down control. The CS5126 is a low-cost version of the CS5101A, intended for audio signal processing applications.

### **CS5102A 16-bit 20 kHz Low Power ADC**

The CS5102A is a low power version of the CS5101A. Requiring only 44 mW from  $\pm 5$  V supplies, along with a 1 mW power down mode, the

CS5102A is ideal for battery powered applications.

### **CS5412 12-bit, 1 MHz ADC**

Using a 2-step flash approach, the CS5412 achieves 12-bit performance at 1 MHz sample rate. Self calibration insures accuracy over time and the military temperature range. Available in both DIP and J-lead LCC packages, with on-chip S/H, the IC offers a very compact ADC solution.

### **CS5501, CS5503 16/20-bit DC Measurement ADC**

The CS5501 and CS5503 feature an on-chip, 6-pole, low-pass filter, with adjustable corner frequencies from 0.1 Hz to 10 Hz. The ADC's achieve linearity errors of 0.0007%, with no missing codes. A highly flexible serial interface, along with 25 mW power consumption, all in a 20 pin package, make the parts ideal for weigh scale and process control applications. The CS5503 is the 20-bit version of the CS5501, offering increased dynamic range, often removing the need for external gain scaling.

### **CS5505/6/7/8 4-channel, 16/20-bit DC Measurement ADC**

Very low power consumption of 1.5 mW, along with a 4-channel input mux, make this part ideal for process control and hand held meter applications. These ADC's are available in 16 or 20 bit

versions, with single channel or 4 channel inputs and DIP or surface mount packages.

### CS5516, CS5520 16/20-bit Bridge Transducer ADC

The CS5516 and CS5520 are complete solutions for digitizing low level signals from strain gauges, load cells and pressure transducers. Any family of mV output transducers, including those needing bridge excitation, can be directly interfaced to the CS5516 or CS5520. The devices offer an on-chip software programmable instrumentation amplifier, choice of AC or DC bridge excitation, software selectable reference and signal demodulation.

### CS5322, CS5323, CS5324, 24-bit Variable Bandwidth ADC

The CS5323 modulator, combined with the CS5322 digital filter, offers >120 dB dynamic range in the DC to 1500 Hz frequency band. Seven different filter corner frequencies and output update rates are offered, allowing the ADC to be optimized for different types of seismic measurements. The CS5324 includes a modulator and the first stage of digital filtering, allowing users to implement their own final filter stage.

3

Specifications	CS5012A CS5014 CS5016	CS5030 CS5031 CS5032	CS5101A CS5102A CS5126	CS5317	CS5322 CS5323 CS5324	CS5412	CS5501 CS5503	CS5505 CS5506 CS5507 CS5508	CS5516 CS5520
Application	GP	GP	GP	Modem	Seismic	GP Fast	DC Measurement		
Resolution (bits)	12/14/16	12	16	16	24	12	16/20	16/20	16/20
Conversion Time (us)	7/14/16	3	8/40	-	-	1.25	-	-	-
Throughput (kHz)	100/56/50	400	100/20	20	-	1 MHz	4	60/100Hz	60Hz
Number of Inputs	1	1	2	1	1	1	1	1/4	1
Input Bandwidth	-	-	-	10 kHz	1500 Hz	4 MHz	10Hz	10 Hz	12Hz
Integral Non-Linearity(%)	.006/.002/.001	.001	.0015	-	-	.01	.0007	.0015	.0007
Differential (± LSB) Non-Linearity	0.25/0.25/NMC	±0.5	NMC	NMC	NMC	0.9	0.125/NMC	0.125	0.5
No Missing Codes	12/14/16	12	16	16	20	12	16/20	16/18	16/20
Total Harmonic Distortion (%)	.008/.003/.001	.001	.001	.007	.0003	.02	-	-	-
Signal-to-Noise plus Distortion (dB)	73/83/92	72	92	80	-	70	-	-	-
Dynamic Range (dB)	73/83/92	72	92	84	120	70	-	-	-
Power Needed (mW)	120	40	280/44	220	150	750	25	3	30
Conversion Method	Succ. Approx.	Succ. Approx.	Succ. Approx.	Delta Sigma	Delta Sigma	2-Step Flash	Delta Sigma	Delta Sigma	Delta Sigma
Power Down Mode			✓		✓		✓	✓	✓
On-Chip Sample and Hold	✓	✓	✓	✓	✓	✓	✓	✓	✓
On-Chip V. Ref		✓		✓				✓	✓
On-Chip Filtering				✓	✓		✓	✓	✓
Statically Tested	✓	✓	✓			✓	✓	✓	✓
Dynamically Tested	✓	✓	✓	✓	✓	✓			
Temperature Range	Com Ind Mil	Com Ind Mil	Com Ind Mil	Com Ind Mil	Com Ind	Com Ind Mil	Com Ind Mil	Ind Mil	Ind Mil
Number of Pins (DIP)	40	24	28	18	28	40	20	20/24	24
Packages	DIP PLCC LCC	DIP	DIP PLCC LCC	DIP SOIC	PLCC	DIP JLCC	DIP SOIC	DIP SOIC	DIP SOIC

NMC=No Missing Codes

GP=General Purpose

**CS5317 16-bit Voice Band ADC**

The CS5317 is well suited for a wide range of voiceband applications, from speech recognition to passive sonar. An on-chip PLL/Clock generator makes the part perfect for high-performance modems. The device features a 20 kHz word rate, a 10 kHz bandwidth, 84 dB dynamic range and 80 dB THD

**CS5336 Audio Bandwidth ADC's**

Selected members of our audio ADC family are now available in industrial or military versions (See the Digital Audio Section, page 2-159).

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## 16, 14 & 12-Bit, Self-Calibrating A/D Converters

### Features

- Monolithic CMOS A/D Converters  
Microprocessor Compatible  
Parallel and Serial Output  
Inherent Track/Hold Input
- True 12, 14 and 16-Bit Precision
- Conversion Times:  
CS5016 16.25  $\mu$ s  
CS5014 14.25  $\mu$ s  
CS5012A 7.2  $\mu$ s
- Self Calibration Maintains Accuracy  
Over Time and Temperature
- Low Power Dissipation: 150 mW
- Low Distortion

### General Description

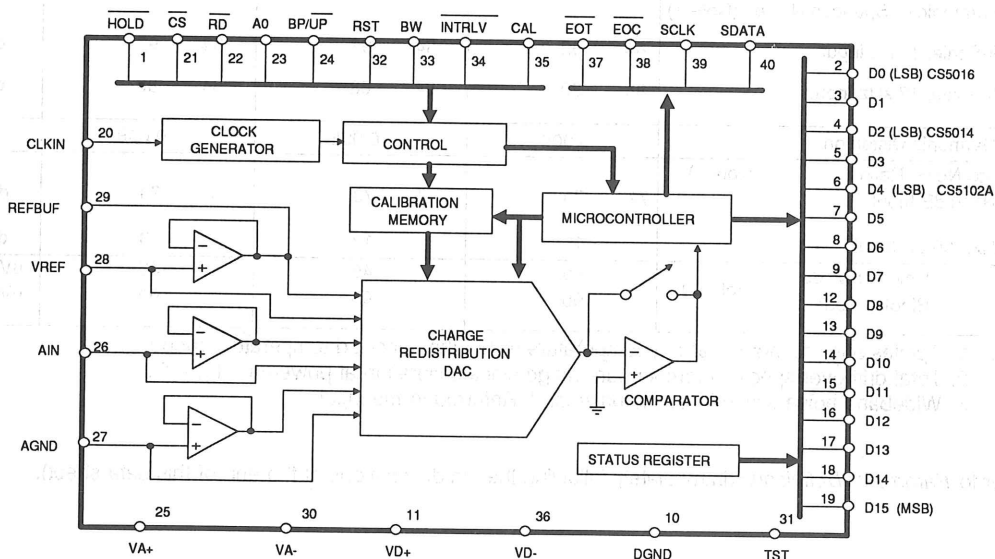
The CS5012A/14/16 are 12, 14 and 16-bit monolithic analog to digital converters with conversion times of 7.2 $\mu$ s, 14.25 $\mu$ s and 16.25 $\mu$ s. Unique self-calibration circuitry insures excellent linearity and differential non-linearity, with no missing codes. Offset and full scale errors are kept within 1/2 LSB (CS5012A/14) and 1 LSB (CS5016), eliminating the need for calibration. Unipolar and bipolar input ranges are digitally selectable.

The pin compatible CS5012A/14/16 consist of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the devices' sampling architecture, acquires the input signal after each conversion using a fast slewing on-chip buffer amplifier. This allows throughput rates up to 100 kHz (CS5012A), 56 kHz (CS5014) and 50 kHz (CS5016).

An evaluation board (CDB5012/14/16) is available which allows fast evaluation of ADC performance.

**ORDERING INFORMATION:** Pages 3-45 & 3-46

3





**CS5012A ANALOG CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}$ ,  $V_{D+} = 5V$ ;  
 $V_{A-}$ ,  $V_{D-} = -5V$ ;  $V_{REF} = 2.5V$  to  $4.5V$ ;  $f_{CLK} = 6.4$  MHz for  $-7$ , 4 MHz for  $-12$ , 2 MHz for  $-24$ ;  
 Analog Source Impedance = 200  $\Omega$ )

Parameter *		CS5012-K CS5012A-K			CS5012-B CS5012A-B			CS5012-T CS5012A-T			Units
		min	typ	max	min	typ	max	min	typ	max	
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125			°C
Accuracy											
Linearity Error	(Note 1)	± 1/4 ± 1/2			± 1/4 ± 1/2			± 1/4 ± 1/2			LSB <sub>12</sub>
Drift	(Note 2)	± 1/8			± 1/8			± 1/8			ΔLSB <sub>12</sub>
Differential Linearity	(Note 1)	± 1/4 ± 1/2			± 1/4 ± 1/2			± 1/4 ± 1/2			LSB <sub>12</sub>
Drift	(Note 2)	± 1/32			± 1/32			± 1/32			ΔLSB <sub>12</sub>
Full Scale Error	(Note 1)	± 1/4 ± 1/2			± 1/4 ± 1/2			± 1/4 ± 1/2			LSB <sub>12</sub>
Drift	(Note 2)	± 1/16			± 1/16			± 1/8			ΔLSB <sub>12</sub>
Unipolar Offset	(Note 1)	± 1/4 ± 1/2			± 1/4 ± 1/2			± 1/4 ± 1/2			LSB <sub>12</sub>
Drift	(Note 2)	± 1/16			± 1/16			± 1/16			ΔLSB <sub>12</sub>
Bipolar Offset	(Note 1)	± 1/4 ± 1/2			± 1/4 ± 1/2			± 1/4 ± 1/2			LSB <sub>12</sub>
Drift	(Note 2)	± 1/16			± 1/16			± 1/16			ΔLSB <sub>12</sub>
Bipolar Negative Full-Scale Error	(Note 1)	± 1/4 ± 1/2			± 1/4 ± 1/2			± 1/4 ± 1/2			LSB <sub>12</sub>
Drift	(Note 2)	± 1/16			± 1/16			± 1/16			ΔLSB <sub>12</sub>
Total Unadjusted Error	(Note 1)	± 1/4			± 1/4			± 1/4			LSB <sub>12</sub>
Drift	(Note 2)	± 1/4			± 1/4			± 1/4			ΔLSB <sub>12</sub>
Dynamic Performance (Bipolar Mode)											
Peak Harmonic or Spurious Noise (Note 1)											
Full-Scale, 1 kHz Input		84	92		84	92		84	92		dB
Full-Scale, 12 kHz Input		84	88		84	88		84	88		dB
Total Harmonic Distortion		0.008			0.008			0.008			%
Signal-to-Noise Ratio (Note 1)											
1 kHz, 0 dB Input		72	73		72	73		72	73		dB
1 kHz, -60 dB Input		13			13			13			dB
Noise	Unipolar Mode	45			45			45			μV <sub>rms</sub>
	Bipolar Mode (Note 3 )	90			90			90			μV <sub>rms</sub>

Notes: 1. Applies after calibration at any temperature within the specified temperature range.  
 2. Total drift over specified temperature range since calibration at power-up at 25 °C.  
 3. Wideband noise aliased into the baseband. Referred to the input.

\* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

### CS5012A ANALOG CHARACTERISTICS (continued)

Parameter *		CS5012-K CS5012A-K		CS5012-B CS5012A-B		CS5012-T CS5012A-T		Units
		min	typ	max	min	typ	max	
Specified Temperature Range		0 to +70		-40 to +85		-55 to +125		° C
Analog Input								
Aperture Time		25		25		25		ns
Aperture Jitter		100		100		100		ps
Input Capacitance	(Note 4)							
Unipolar Mode	CS5012	275	375	275	375	275	375	pF
	CS5012A	103	137	103	137	103	137	pF
Bipolar Mode	CS5012	165	220	165	220	165	220	pF
	CS5012A	72	96	72	96	72	96	pF
Conversion & Throughput								
Conversion Time	-7	7.2		7.2		7.2		us
(Notes 5, 6)	-12	12.25		12.25		12.25		us
	-24	24.5		24.5		24.5		us
Acquisition Time	-7	2.5	2.8	2.5	2.8	2.5	2.8	us
(Note 6)	-12	3.0	3.75	3.0	3.75	3.0	3.75	us
	-24	4.5	5.25	4.5	5.25	4.5	5.25	us
Throughput	-7	100		100		100		kHz
(Note 6)	-12	62.5		62.5		62.5		kHz
	-24	33.6		33.6		33.6		kHz
Power Supplies								
DC Power Supply Currents (Note 7)								
	I <sub>A+</sub>	12	19	12	19	12	19	mA
	I <sub>A-</sub>	-12	-19	-12	-19	-12	-19	mA
	I <sub>D+</sub>	3	6	3	6	3	6	mA
	I <sub>D-</sub>	-3	-6	-3	-6	-3	-6	mA
Power Dissipation	(Note 7)	150	250	150	250	150	250	mW
Power Supply Rejection	(Note 8)							
Positive Supplies		84		84		84		dB
Negative Supplies		84		84		84		dB

- Notes:
4. Applies only in track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
  5. Measured from falling transition on HOLD to falling transition on EOC.
  6. Conversion, acquisition, and throughput times depend on CLKIN, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5012A/14/16's conversion clock, interleave calibrate is disabled, and operation is from the full-rated, external clock. Refer to the section *Conversion Time/Throughput* for a detailed discussion of conversion timing.
  7. All outputs unloaded. All inputs CMOS levels.
  8. With 300 mV p-p, 1 kHz ripple applied to each analog supply separately in bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 13 shows a plot of typical power supply rejection versus frequency.

**CS5014 ANALOG CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}$ ,  $V_{D+} = 5V$ ;  
 $V_{A-}$ ,  $V_{D-} = -5V$ ;  $V_{REF} = 4.5V$ ;  $CLKIN = 4\text{ MHz}$  for  $-14$ ,  $2\text{ MHz}$  for  $-28$ ; Analog Source Impedance =  $200\ \Omega$ )

Parameter *		CS5014-K		CS5014-B		CS5014-S,T		Units
		min	typ max	min	typ max	min	typ max	
Specified Temperature Range		0 to +70		-40 to +85		-55 to +125		°C
Accuracy								
Linearity Error	(Note 1) K,B,T S	± 1/4 ± 1/2		± 1/4 ± 1/2		± 1/4 ± 1/2 ± 1/2 ± 1.5		LSB <sub>14</sub> LSB <sub>14</sub> ΔLSB <sub>14</sub>
Drift	(Note 2)	± 1/8		± 1/8		± 1/8		
Differential Linearity	(Note 1)	± 1/4 ± 1/2		± 1/4 ± 1/2		± 1/4 ± 1/2		LSB <sub>14</sub>
Drift	(Note 2)	± 1/32		± 1/32		± 1/32		ΔLSB <sub>14</sub>
Full Scale Error	(Note 1)	± 1/2 ± 1		± 1/2 ± 1		± 1/2 ± 1		LSB <sub>14</sub>
Drift	(Note 2)	± 1/4		± 1/4		± 1/2		ΔLSB <sub>14</sub>
Unipolar Offset	(Note 1) K,B,T S	± 1/4 ± 3/4		± 1/4 ± 3/4		± 1/4 ± 3/4 ± 1		LSB <sub>14</sub> LSB <sub>14</sub> ΔLSB <sub>14</sub>
Drift	(Note 2)	± 1/4		± 1/4		± 1/2		
Bipolar Offset	(Note 1) K,B,T S	± 1/4 ± 3/4		± 1/4 ± 3/4		± 1/4 ± 3/4 ± 1		LSB <sub>14</sub> LSB <sub>14</sub> ΔLSB <sub>14</sub>
Drift	(Note 2)	± 1/4		± 1/2		± 1/2		
Bipolar Negative Full-Scale Error	(Note 1) K,B,T S	± 1/2 ± 1		± 1/2 ± 1		± 1/2 ± 1 ± 1.5		LSB <sub>14</sub> LSB <sub>14</sub> ΔLSB <sub>14</sub>
Drift	(Note 2)	± 1/4		± 1/4		± 1/2		
Total Unadjusted Error	(Note 1)	± 1		± 1		± 1		LSB <sub>14</sub>
Drift	(Note 2)	± 1/2		± 1		± 1		ΔLSB <sub>14</sub>
Dynamic Performance (Bipolar Mode)								
Peak Harmonic or Spurious Noise (Note 1)								
Full-Scale, 1 kHz Input	K,B,T S	94	98	94	98	94	98	dB
						85		dB
Full-Scale, 12 kHz Input	K,B,T S	84	87	84	87	84	87	dB
						80		dB
Total Harmonic Distortion		0.003		0.003		0.003		%
Signal-to-Noise Ratio (Note 1, 9)								
1 kHz, 0 dB Input	K,B,T S	82	84	82	84	82	84	dB
						80		dB
1 kHz, -60 dB Input		23		23		23		dB
Noise	Unipolar Mode	45		45		45		μV <sub>rms</sub>
	Bipolar Mode (Note 3)	90		90		90		μV <sub>rms</sub>

Notes: 9. A detailed plot of  $S/(N+D)$  vs. input amplitude appears in Figure 26 for the CS5014 and Figure 28 for the CS5016.

\* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

### CS5014 ANALOG CHARACTERISTICS (continued)

Parameter *	CS5014-K			CS5014-B			CS5014-S,T			Units
	min	typ	max	min	typ	max	min	typ	max	
Specified Temperature Range	0 to +70			-40 to +85			-55 to +125			°C
<b>Analog Input</b>										
Aperture Time	25			25			25			ns
Aperture Jitter	100			100			100			ps
Input Capacitance (Note 4)										
Unipolar Mode	275	375		275	375		275	375		pF
Bipolar Mode	165	220		165	220		165	220		pF
<b>Conversion &amp; Throughput</b>										
Conversion Time	-14	14.25		-14	14.25		-14	14.25		us
-28 (Notes 5, 6)		28.5			28.5			28.5		us
Acquisition Time	-14	3.0	3.75	-14	3.0	3.75	-14	3.0	3.75	us
-28 (Note 6)		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput	-14	55.6		-14	55.6		-14	55.6		kHz
-28 (Note 6)		27.7			27.7			27.7		kHz
<b>Power Supplies</b>										
DC Power Supply Currents (Note 7)										
I <sub>A+</sub>	9	19		9	19		9	19		mA
I <sub>A-</sub>	-9	-19		-9	-19		-9	-19		mA
I <sub>D+</sub>	3	6		3	6		3	6		mA
I <sub>D-</sub>	-3	-6		-3	-6		-3	-6		mA
Power Dissipation (Note 7)	120	250		120	250		120	250		mW
Power Supply Rejection (Note 8)										
Positive Supplies	84			84			84			dB
Negative Supplies	84			84			84			dB

**CS5016 ANALOG CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}$ ,  $V_{D+} = 5V$ ;  
 $V_{A-}$ ,  $V_{D-} = -5V$ ;  $V_{REF} = 4.5V$ ;  $CLKIN = 4\text{ MHz}$  for  $-16$ ,  $2\text{ MHz}$  for  $-32$ ; Analog Source Impedance =  $200\ \Omega$ ;  
Synchronous Sampling.)

Parameter *		CS5016 -J,K min typ max		CS5016 -A,B min typ max		CS5016 -S,T min typ max		Units	
Specified Temperature Range		0 to +70		-40 to +85		-55 to +125		°C	
Accuracy									
Linearity Error	(Note 1)	-J,A,S	0.002	0.003	0.002	0.003	0.002	0.0076	% FS
		-K,B,T	0.001	0.0015	0.001	0.0015	0.001	0.0015	% FS
	(Note 2)	Drift	± 1/4		± 1/4		± 1/4		ΔLSB <sub>16</sub>
Differential Linearity		(Note 10)	16		16		16		Bits
Full Scale Error	(Note 1)	-J,A,S	± 2	± 3	± 2	± 3	± 2	± 4	LSB <sub>16</sub>
		-K,B,T	± 2	± 3	± 2	± 3	± 2	± 3	LSB <sub>16</sub>
	(Note 2)	Drift	± 1		± 1		± 2		ΔLSB <sub>16</sub>
Unipolar Offset	(Note 1)	-J,A,S	± 1	± 2	± 1	± 3	± 1	± 4	LSB <sub>16</sub>
		-K,B,T	± 1	± 3/2	± 1	± 3	± 1	± 3	LSB <sub>16</sub>
	(Note 2)	Drift	± 1		± 1		± 2		ΔLSB <sub>16</sub>
Bipolar Offset	(Note 1)	-J,A,S	± 1	± 2	± 1	± 2	± 1	± 4	LSB <sub>16</sub>
		-K,B,T	± 1	± 3/2	± 1	± 2	± 1	± 2	LSB <sub>16</sub>
	(Note 2)	Drift	± 1		± 2		± 2		ΔLSB <sub>16</sub>
Bipolar Negative Full-Scale Error	(Note 1)	-J,A,S	± 2	± 3	± 2	± 3	± 2	± 5	LSB <sub>16</sub>
		-K,B,T	± 2	± 3	± 2	± 3	± 2	± 3	LSB <sub>16</sub>
	(Note 2)	Drift	± 1		± 2		± 2		ΔLSB <sub>16</sub>
Dynamic Performance (Bipolar Mode)									
Peak Harmonic or Spurious Noise									
Full-Scale, 1kHz Input		-J,A,S	96	100	96	100	92	100	dB
		-K,B,T	100	104	100	104	100	104	dB
	(Note 1)	-J,A,S	85	88	85	88	82	88	dB
Full-Scale, 12kHz Input		-K,B,T	85	91	85	91	85	91	dB
Total Harmonic Distortion									
Full-Scale, 1kHz Input		-J,A,S	0.002		0.002		0.002		%
		-K,B,T	0.001		0.001		0.001		%
Signal-to-Noise Ratio									
1kHz, 0dB Input		-J,A,S	87	90	87	90	84	90	dB
		-K,B,T	90	92	90	92	90	92	dB
(Note 1, 9)		-J,A,S		30		30		30	dB
		-K,B,T		32		32		32	dB
Noise	Unipolar Mode		35		35		35		uV <sub>rms</sub>
	(Note 3) Bipolar Mode		70		70		70		uV <sub>rms</sub>

Notes: 10. Minimum resolution for which no missing codes is guaranteed

\* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

**CS5016 ANALOG CHARACTERISTICS** (continued)

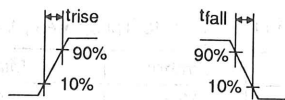
CS5016 -J,K (continued)									
Parameter *		CS5016 -J,K min typ max		CS5016 -A,B min typ max		CS5016 -S,T min typ max		Units	
Specified Temperature Range		0 to +70		-40 to +85		-55 to +125		°C	
Analog Input									
Aperture Time		25		25		25		ns	
Aperture Jitter		100		100		100		ps	
Input Capacitance (Note 4)									
Unipolar Mode		275 375		275 375		275 375		pF	
Bipolar Mode		165 220		165 220		165 220		pF	
Conversion & Throughput									
Conversion Time (Notes 5, 6)		-16 -32		16.25 32.5		16.25 32.5		16.25 32.5 us us	
Acquisition Time (Note 6)		-16 -32		3.0 3.75 4.5 5.25		3.0 3.75 4.5 5.25		3.0 3.75 4.5 5.25 us us	
Throughput (Note 6)		-16 -32		50 26.5		50 26.5		50 26.5 kHz kHz	
Power Supplies									
Power Supply Currents (Note 8)									
I <sub>A+</sub>		9 19		9 19		9 19		mA	
I <sub>A-</sub>		-9 -19		-9 -19		-9 -19		mA	
I <sub>D+</sub>		3 6		3 6		3 6		mA	
I <sub>D-</sub>		-3 -6		-3 -6		-3 -6		mA	
Power Dissipation (Note 8)		120 250		120 250		120 250		mW	
Power Supply Rejection (Note 8)									
Positive Supplies		84		84		84		dB	
Negative Supplies		84		84		84		dB	

**SWITCHING CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}, V_{D+} = 5V \pm 10\%$ ;  $V_{A-}, V_{D-} = -5V \pm 10\%$ ; Inputs: Logic 0 = 0V, Logic 1 =  $V_{D+}$ ;  $C_L = 50$  pF,  $BW = V_{D+}$ )

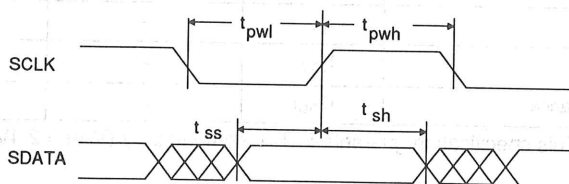
Parameter	Symbol	Min	Typ	Max	Units
CS5012A CLKIN Frequency: Internally Generated: K, B, -7, -12 T, -7, -12 -24 Externally Supplied: -7 -12 -24	$f_{CLK}$	2 1.75 1 100 kHz 100 kHz 100 kHz	- - - - - -	- - - 6.4 4.0 2.0	MHz
CS5014/16 CLKIN Frequency: Internally Generated: A, B, J, K, 14, -16 S, T, -14, -16 -28, -32 Externally Supplied: -14, -16 -28, -32	$f_{CLK}$	2 1.75 1 100 kHz 100 kHz	- - - - -	- - - 4 2	MHz
CLKIN Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input Any Digital Output	$t_{rise}$	- -	- 20	1.0 -	$\mu s$ ns
Fall Times: Any Digital Input Any Digital Output	$t_{fall}$	- -	- 20	1.0 -	$\mu s$ ns
HOLD Pulse Width	$t_{hpw}$	$1/f_{CLK} + 50$	-	$t_c$	ns
Conversion Time: CS5012A CS5014 CS5016	$t_c$	$49/f_{CLK} + 50$ $57/f_{CLK}$ $65/f_{CLK}$	- - -	$53/f_{CLK} + 235$ $61/f_{CLK} + 235$ $69/f_{CLK} + 235$	ns
Data Delay Time	$t_{dd}$	-	40	100	ns
EOC Pulse Width (Note 11)	$t_{epw}$	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: $\overline{CS}$ , $\overline{INTRLV}$ to $\overline{CS}$ Low A0 to $\overline{CS}$ and $\overline{RD}$ Low	$t_{cs}$ $t_{as}$	20 20	10 10	- -	ns
Hold Times: $\overline{CS}$ or $\overline{RD}$ High to A0 Invalid $\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	$t_{ah}$ $t_{ch}$	50 50	30 30	- -	ns
Access Times: $\overline{CS}$ Low to Data Valid - A, B, J, K - S, T $\overline{RD}$ Low to Data Valid - A, B, J, K - S, T	$t_{ca}$ $t_{ra}$	- -	90 115 90 115	120 150 120 150	ns
Output Float Delay: -K, B CS or RD High to Output Hi-Z -T	$t_{fd}$	-	90 90	110 140	ns
Serial Clock Pulse Width Low Pulse Width High	$t_{pwl}$ $t_{pwh}$	- -	$2/f_{CLK}$ $2/f_{CLK}$	- -	ns
Set Up Times: SDATA to SCLK Rising	$t_{ss}$	$2/f_{CLK} - 50$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	$t_{sh}$	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

Note: 11.  $\overline{EOC}$  remains low 4 CLKIN cycles if  $\overline{CS}$  and  $\overline{RD}$  are held low. Otherwise, it returns high within 4 CLKIN cycles from the start of a data read operation or a conversion cycle.

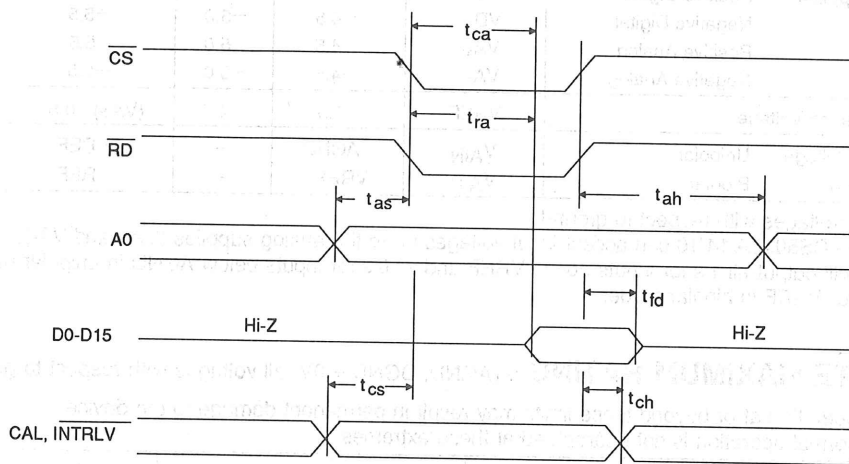




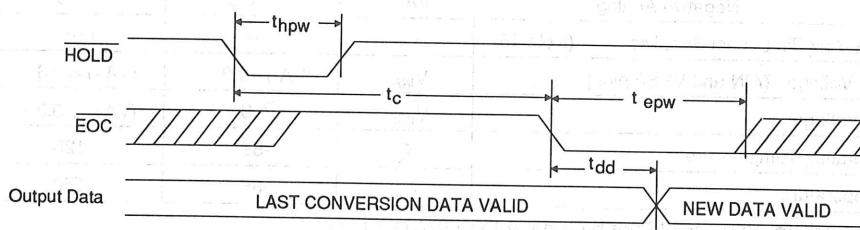
**Rise and Fall Times**



**Serial Output Timing**



**Read and Calibration Control Timing**



**Conversion Timing**

**DIGITAL CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}$ ,  $V_{D+} = 5V \pm 10\%$ ;  $V_{A-}$ ,  $V_{D-} = -5V \pm 10\%$ )

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	$V_{IH}$	2.0	—	—	V
Low-Level Input Voltage	$V_{IL}$	—	—	0.8	V
High-Level Output Voltage (Note 12)	$V_{OH}$	$(V_{D+}) - 1.0V$	—	—	V
Low-Level Output Voltage $I_{out}=1.6mA$	$V_{OL}$	—	—	0.4	V
Input Leakage Current	$I_{in}$	—	—	10	$\mu A$
3-State Leakage Current	$I_{OZ}$	—	—	$\pm 10$	$\mu A$
Digital Output Pin Capacitance	$C_{out}$	—	9	—	pF

Note: 12.  $I_{out} = -100 \mu A$ . This specification guarantees TTL compatibility ( $V_{OH} = 2.4V$  @  $I_{out} = -40 \mu A$ ).

**RECOMMENDED OPERATING CONDITIONS** (AGND, DGND = 0V, see Note 14.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	$V_{D+}$	4.5	5.0	$V_{A+}$
	Negative Digital	$V_{D-}$	-4.5	-5.0	-5.5
	Positive Analog	$V_{A+}$	4.5	5.0	5.5
	Negative Analog	$V_{A-}$	-4.5	-5.0	-5.5
Analog Reference Voltage	$V_{REF}$	2.5	4.5	$(V_{A+}) - 0.5$	V
Analog Input Voltage: (Note 14)	Unipolar	$V_{AIN}$	AGND	—	$V_{REF}$
	Bipolar	$V_{AIN}$	-VREF	—	$V_{REF}$

Notes: 13. All voltages with respect to ground.

14. The CS5012A/14/16 can accept input voltages up to the analog supplies ( $V_{A+}$  and  $V_{A-}$ ).

It will output all 1's for inputs above  $V_{REF}$  and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

**ABSOLUTE MAXIMUM RATINGS** (AGND, DGND = 0V, all voltages with respect to ground.)

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

Parameter	Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital (Note 15)	$V_{D+}$	-0.3	6.0
	Negative Digital	$V_{D-}$	0.3	-6.0
	Positive Analog	$V_{A+}$	-0.3	6.0
	Negative Analog	$V_{A-}$	0.3	-6.0
Input Current, Any Pin Except Supplies (Note 16)	$I_{in}$	—	$\pm 10$	mA
Analog Input Voltage ( $A_{IN}$ and $V_{REF}$ pins)	$V_{INA}$	$(V_{A-}) - 0.3$	$(V_{A+}) + 0.3$	V
Digital Input Voltage	$V_{IND}$	-0.3	$(V_{A+}) + 0.3$	V
Ambient Operating Temperature	$T_A$	-55	125	$^{\circ}C$
Storage Temperature	$T_{stg}$	-65	150	$^{\circ}C$

Note: 15. In addition,  $V_{D+}$  should not be greater than  $(V_{A+}) + 0.3V$ .

16. Transient currents of up to 100 mA will not cause SCR latch-up.

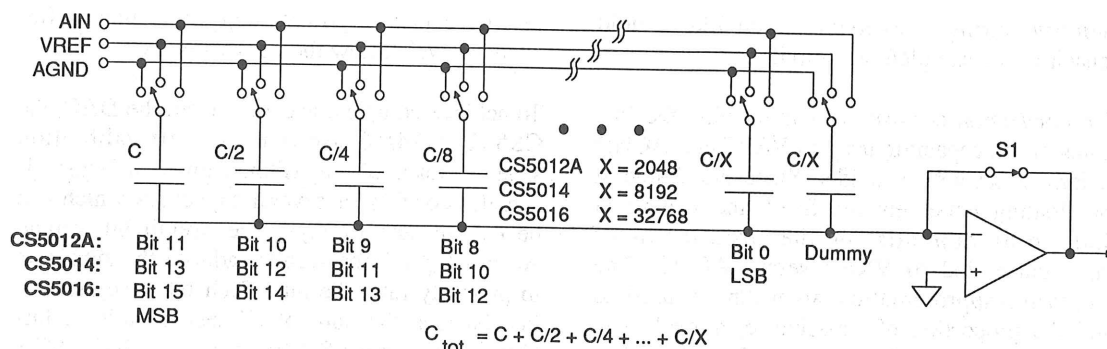


Figure 1. Charge Redistribution DAC

## THEORY OF OPERATION

The CS5012A/14/16 family utilize a successive approximation conversion technique. The analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

A unique charge redistribution architecture is used to implement the successive approximation

algorithm. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all capacitors are tied to AIN forming  $C_{tot}$ . Switch S1 is closed and the charge on the array,  $Q_{in}$ , tracks the input signal  $V_{in}$  (Figure 2a).

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge  $Q_{in}$  on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog

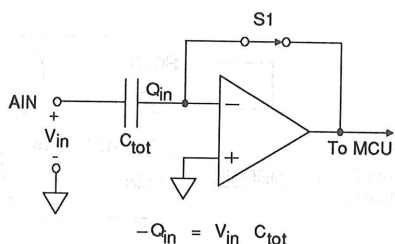


Figure 2a. Tracking Mode

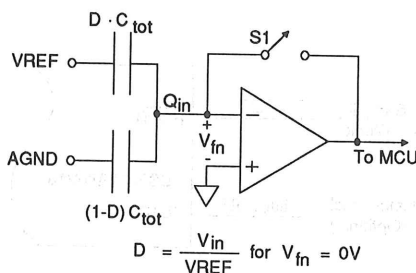


Figure 2b. Convert Mode

memory during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which when connected to the reference will drive the voltage at the floating node ( $V_{fn}$ ) to zero. That binary fraction of capacitance represents the converter's digital output.

This charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range is doubled and is offset half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

### Calibration

The ability of the CS5012A/14/16 to convert accurately clearly depends on the accuracy of their comparator and DAC. The CS5012A/14/16 utilize an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-

zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve complete accuracy from the DAC, the CS5012A/14/16 use a novel self-calibration scheme. Each bit capacitor, shown in Figure 1, actually consists of several capacitors which can be manipulated to adjust the overall bit weight. An on-chip microcontroller adjusts the subarrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example,  $16C = 8C + 4C + 2C + C + C$ ). Calibration resolution for the array is a small fraction of an LSB resulting in nearly ideal differential and integral linearity.

### DIGITAL CIRCUIT CONNECTIONS

The CS5012A/14/16 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the devices' conversion time and throughput. The devices also feature on-chip 3-state output buffers and a complete interface for connecting to 8-bit and 16-bit digital systems. Output data is also available in serial format.

### Master Clock

The CS5012A/14/16 operate from a master clock (CLKIN) which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the CS5012A/14/16 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

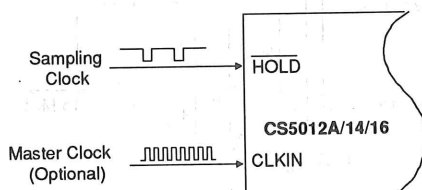


Figure 3a. Asynchronous Sampling

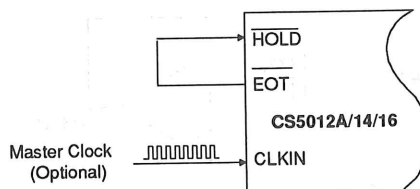


Figure 3b. Synchronous Sampling

All calibration, conversion, and throughput times directly scale to CLKIN frequency. Thus, throughput can be precisely controlled and/or maximized using an external CLKIN signal. In contrast, the CS5012A/14/16's internal oscillator will vary from unit-to-unit and over temperature. The CS5012A/14/16 can typically convert with CLKIN as low as 10 kHz at room temperature.

### Initiating Conversions

A falling transition on the  $\overline{\text{HOLD}}$  pin places the input in the hold mode and initiates a conversion cycle. Upon completion of the conversion cycle, the CS5012A/14/16 automatically return to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the  $\overline{\text{HOLD}}$  input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one CLKIN cycle plus 50 ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

### Microprocessor-Controlled Operation

Sampling and conversion can be placed under microprocessor control (Figure 4) by simply gating the devices' decoded address with the write strobe for the  $\overline{\text{HOLD}}$  input. Thus, a write cycle to the CS5012A/14/16's base address will initiate a conversion. However, the write cycle

must be to the odd address (A0 high) to avoid initiating a software controlled reset (see *Reset* below).

The calibration control inputs, CAL, and  $\overline{\text{INTRLV}}$  are inputs to a set of transparent latches. These signals are internally latched by  $\overline{\text{CS}}$  returning high. They must be in the appropriate state whenever the chip is selected during a read or write cycle. Address lines A1 and A2 are shown connected to CAL and  $\overline{\text{INTRLV}}$  in Figure 4 placing calibration under microprocessor control as well. Thus, any read or write cycle to the CS5012A/14/16's base address will initiate or terminate calibration. Alternatively, A0,  $\overline{\text{INTRLV}}$ , and CAL may be connected to the microprocessor data bus.

### Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CS5012A/14/16 require time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six CLKIN cycles plus 2.25  $\mu\text{s}$  (1.32  $\mu\text{s}$  for the CS5012A -7 version only). This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CS5012A/14/16, in turn, depends on the sampling, calibration, and CLKIN conditions.

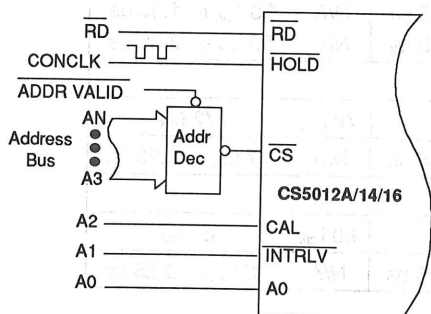


Figure 4a. Conversions Asynchronous to CLKIN

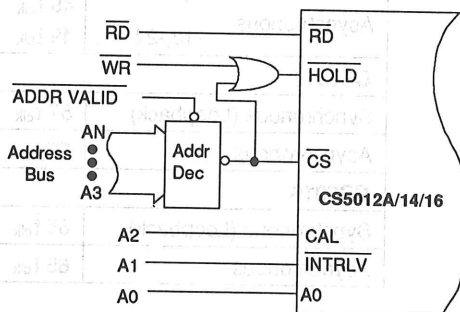
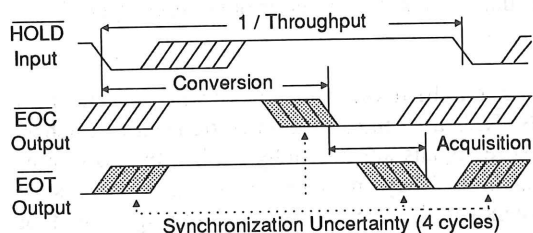


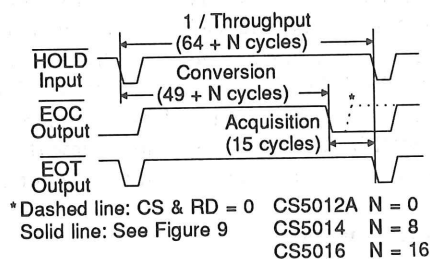
Figure 4b. Conversions under Microprocessor Control



**Figure 5a. Asynchronous Sampling (External Clock)**

### Asynchronous Sampling

The CS5012A/14/16 internally operate from a clock which is delayed and divided down from CLKIN ( $f_{CLK}/4$ ). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after HOLD goes low *even though the charge is trapped immediately*. In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 49, 57 and 65 clock cycles (for the CS5012A/14/16 respectively) to define the maximum conversion time (see Figure 5a and Table 1).



**Figure 5b. Synchronous (Loopback Mode)**

### Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track (EOT) output to HOLD (Figure 3b). The EOT output falls 15 CLKIN cycles after EOC indicating the analog input has been acquired to the CS5012A/14/16's specified accuracy. The EOT output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at  $[1/64]f_{CLK}$  for the CS5012A,  $[1/72]f_{CLK}$  for CS5014 and  $[1/80]f_{CLK}$  for CS5016 where  $f_{CLK}$  is the CLKIN frequency (see Figure 5b and Table 1).

Sampling Mode	Conversion Time		Throughput Time	
	Min	Max	Min	Max
<b>CS5012A</b>				
Synchronous (Loopback)	49 $t_{clk}$	49 $t_{clk}$	64 $t_{clk}$	64 $t_{clk}$
Asynchronous	49 $t_{clk}$	53 $t_{clk} + 235$ ns	N/A	59 $t_{clk} + 1.32$ $\mu$ s
	49 $t_{clk}$	53 $t_{clk} + 235$ ns	N/A	59 $t_{clk} + 2.25$ $\mu$ s
<b>CS5014</b>				
Synchronous (Loopback)	57 $t_{clk}$	57 $t_{clk}$	72 $t_{clk}$	72 $t_{clk}$
Asynchronous	57 $t_{clk}$	61 $t_{clk} + 235$ ns	N/A	67 $t_{clk} + 2.25$ $\mu$ s
<b>CS5016</b>				
Synchronous (Loopback)	65 $t_{clk}$	65 $t_{clk}$	80 $t_{clk}$	80 $t_{clk}$
Asynchronous	65 $t_{clk}$	69 $t_{clk} + 235$ ns	N/A	75 $t_{clk} + 2.25$ $\mu$ s

**Table 1. Conversion and Throughput Times ( $t_{clk}$  = Master Clock Period)**

Also, the CS5012A/14/16's internal RC oscillator exhibits jitter (typically  $\pm 0.05\%$  of its period), which is high compared to crystal oscillators. If the CS5012A/14/16 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity. The user can obtain best sampling purity while synchronously sampling by using an external crystal-based clock.

### Reset

Upon power up, the CS5012A/14/16 must be reset to guarantee a consistent starting condition and initially calibrate the devices. Due to the CS5012A/14/16's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 5%, 1% or 0.25% of its final value, for the CS5012/14/16 respectively, before RST falls to guarantee an accurate calibration. Later, the CS5012A/14/16 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5012A/14/16 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Resets can be initiated in hardware or software. The simplest method of resetting the CS5012A/14/16 involves strobing the RST pin high for at least 100 ns. When RST is brought high all internal logic clears. When it returns low, a full calibration begins which takes 58,280 CLKIN cycles for the CS5012A (approximately 9.1 ms with a 6.4 MHz clock) and 1,441,020 CLKIN cycles for the CS5016, CS5014 and CS5012 (approximately 360 ms with a 4 MHz CLKIN). A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmitt-trigger inverter to prevent oscillation (see Figure 6). The CS5012A/14/16 can also be reset in software when under microprocessor control. The CS5012A/14/16 will reset whenever  $\overline{CS}$ , A0, and  $\overline{HOLD}$  are taken low simultaneously. See the *Microprocessor Interface* section (below) to

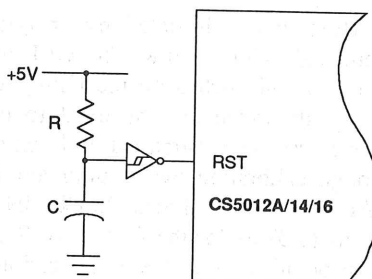


Figure 6. Power-on Reset Circuit

eliminate the possibility of inadvertent software reset. The  $\overline{EOC}$  output remains high throughout the calibration operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CS5012A/14/16 is ready for operation. While calibrating, the  $\overline{HOLD}$  input is ignored until  $\overline{EOC}$  falls. After  $\overline{EOC}$  falls, six CLKIN cycles plus 2.25  $\mu s$  (1.32  $\mu s$  for the CS5012A -7 version only) must be allowed for signal acquisition before  $\overline{HOLD}$  is activated. Under microprocessor-independent operation ( $\overline{CS}$ ,  $\overline{RD}$  low; A0 high) the CS5014's and CS5016's  $\overline{EOC}$  output will not fall at the completion of the calibration cycle, but  $\overline{EOT}$  will fall 15 CLKIN cycles later.

### Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CS5012A/14/16's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is normally only required once, after power-up.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal



fashion. Burst cal is initiated by bringing the CAL input high with  $\overline{CS}$  low. The CAL input is level-triggered and latches on the rising edge of  $\overline{CS}$ , so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 CLKIN cycles plus 2.25  $\mu$ s (1.32  $\mu$ s for the CS5012A -7 version only) must be allowed before a conversion is initiated to ensure the CS5012A/14/16 has completed its calibration experiment and has acquired the analog input. The  $\overline{EOC}$  output indicates the completion of the final calibration experiment. (See the *Addendum* which appends this data sheet.)

The CS5012A/14/16 feature a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CS5012A/14/16 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 2,014 conversions in the CS5012A and one calibration per 72,051 conversions in the CS5012, CS5014 and CS5016). Initiated by bringing both the  $\overline{INTRLV}$  input and  $\overline{CS}$  low (or hard-wiring  $\overline{INTRLV}$  low), interleave extends the CS5012A/14/16's effective conversion time by 20 CLKIN cycles. Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CS5012A/14/16 see free time. Interleave is subordinate to burst calibrations, so  $\overline{INTRLV}$  could still be externally tied low. If used, interleave should be left active continuously.

The fact that the CS5012A/14/16 offer several calibration modes is not to imply that the devices need to be recalibrated often. The devices are very stable in the presence of large temperature

changes. Tests have indicated that after using a single reset calibration at 25 °C most devices exhibit very little change in offset or gain when exposed to temperatures from -55 to +125 °C. The data indicated 30 ppm as the typical worst case total change in offset or gain over this temperature range. Differential linearity remained virtually unchanged. System error sources outside of the A/D converter, whether due to changes in temperature or to long-term aging, will generally dominate total system error.

### Microprocessor Interface

The CS5012A/14/16 feature an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8-bit or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both  $\overline{CS}$  and  $\overline{RD}$  low enables the CS5012A/14/16's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 4b thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ( $\overline{CS}$  and  $\overline{RD}$  strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while  $\overline{HOLD}$  is low, or a software reset will result (see Reset above).*

Alternatively, the End-of-Convert ( $\overline{EOC}$ ) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The  $\overline{EOC}$  pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four CLKIN cycles of the first subsequent data read operation or after the start of a new conversion cycle.

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	END OF CONVERSION	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/HIGH BYTE	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	END OF TRACK	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the input.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Pin Definitions

To interface with a 16-bit data bus, the BW input to the CS5012A/14/16 should be held high and all data bits (12, 14 and 16 for the CS5012A, CS5014 and CS5016 respectively) read in parallel on pins D4-D15 (CS5012A), D2-D15 (CS5014), or D0-D15 (CS5016). With an 8-bit bus, the converter's result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the remaining LSB's (4, 6 or 8 for the CS5012A/14/16 respectively) with 4, 2 or 0 trailing zeros. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next con-

version finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The CS5012A/14/16 internally buffer their output data, so data can be read while the devices are tracking or converting the next sample. Therefore, retrieving the converters' digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CS5012A/14/16 is converting will not introduce conversion errors. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	8- or 16-Bit Data Bus
Status (A0=0)		X	X	X	X	X	X	X	X	S7	S6	S5	S4	S3	S2	S1	S0	
Data (A0=1)	CS5012A	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0	16-Bit Bus (BW=1)
	CS5014	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	
	CS5016	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
	CS5012A	X	X	X	X	X	X	X	X	B11	B10	B9	B8	B7	B6	B5	B4	8-Bit Bus (BW=0)
	CS5014	X	X	X	X	X	X	X	X	B3	B2	B1	B0	0	0	0	0	
	CS5016	X	X	X	X	X	X	X	X	B13	B12	B11	B10	B9	B8	B7	B6	
										B5	B4	B3	B2	B1	B0	0	0	
										B15	B14	B13	B12	B11	B10	B9	B8	
										B7	B6	B5	B4	B3	B2	B1	B0	

"X" Denotes High Impedance Output

Figure 7. CS5012A/14/16 Data Format

### Microprocessor Independent Operation

The CS5012A/14/16 can be operated in a stand-alone mode independent of intelligent control. In this mode,  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  are hard-wired low. This permanently enables the 3-state output buffers and allows transparent latch inputs (CAL and  $\overline{\text{INTRLV}}$ ) to be active. A free-running condition is established when BW is tied high, CAL is tied low, and  $\overline{\text{HOLD}}$  is continually strobed low or tied to  $\overline{\text{EOT}}$ . The CS5012A/14/16's  $\overline{\text{EOC}}$  output can be used to externally latch the output data if desired. With  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  hard-wired low,  $\overline{\text{EOC}}$  will strobe low for four CLKIN cycles after each conversion. Data will be unstable up to 100 ns after  $\overline{\text{EOC}}$  falls, so it should be latched on the rising edge of  $\overline{\text{EOC}}$ .

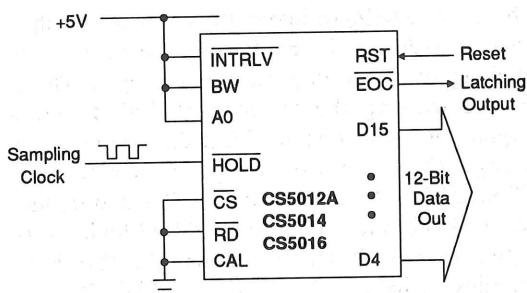


Figure 8. Microprocessor-Independent Connections

### Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CS5012A/14/16 present each bit to the SDATA pin four CLKIN cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CS5012A/14/16 (See Figure 9).

### ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5012A/14/16 internally buffer all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

### Reference Considerations

An application note titled "Voltage References for the CS501X Series of A/D Converters" is available for the CS5012A/14/16. In addition to working through a reference circuit design example, it offers several built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5012A/14/16 include an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CS5012A/14/16 sequence through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the inter-

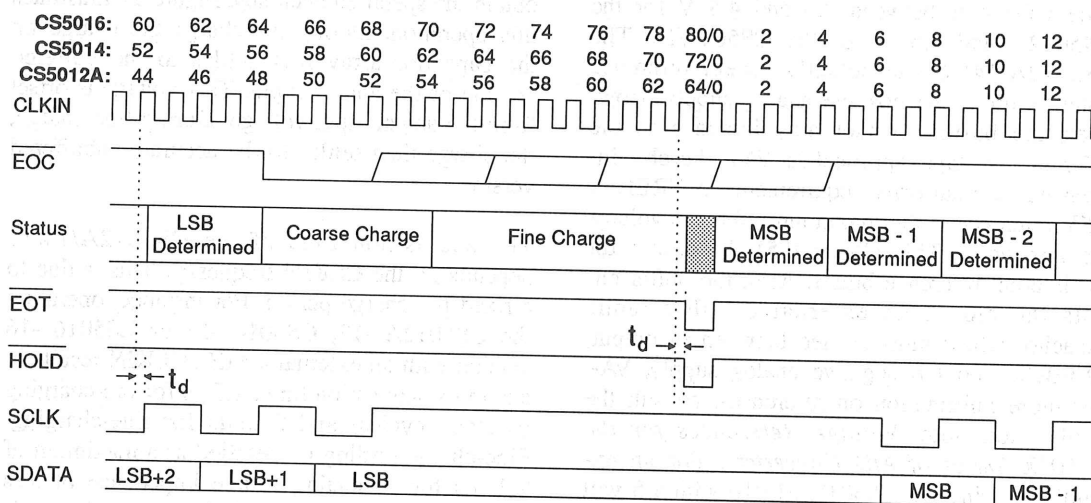
nal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc.

The magnitude of the current load on the external reference circuitry will scale to the CLKIN frequency. At full speed, the reference must supply a maximum load current of 10  $\mu$ A peak-to-peak (1  $\mu$ A typical). For the CS5012A an output im-

pedance of 15  $\Omega$  will therefore yield a maximum error of 150 mV. With a 2.5V reference and LSB size of 600 mV, this would insure better than 1/4 LSB accuracy. A 1  $\mu$ F capacitor exhibits an impedance of less than 15  $\Omega$  at frequencies greater than 10 kHz. Similarly, for the CS5014 with a 4.5V reference (275  $\mu$ V/LSB), better than 1/4 LSB accuracy can be insured with an output impedance of 4  $\Omega$  or less (maximum error of 40  $\mu$ V). A 2.2  $\mu$ F capacitor exhibits an impedance of less than 4  $\Omega$  at frequencies greater than 5 kHz. For the CS5016 with a 4.5V reference (69  $\mu$ V/LSB), better than 1/4 LSB accuracy can be insured with an output impedance of less than 2  $\Omega$  (maximum error of 20  $\mu$ V). A 20  $\mu$ F capacitor exhibits an impedance of less than 2  $\Omega$  at frequencies greater than 16 kHz. A high-

3



- Notes: 1. Synchronous (loopback) mode is illustrated. After  $\overline{EOC}$  falls the converter goes into coarse charge mode for 6 CLKIN cycles, then to fine charge mode for 9 cycles, then  $\overline{EOT}$  falls. In loopback mode,  $\overline{EOT}$  trips  $\overline{HOLD}$  which captures the analog sample. Conversion begins on the next rising edge of CLKIN. If operated asynchronously,  $\overline{EOT}$  will remain low until after  $\overline{HOLD}$  is taken low. When  $\overline{HOLD}$  occurs the analog sample is captured immediately, but conversion may not begin until four CLKIN cycles later.  $\overline{EOT}$  will return high when conversion begins.
2. Timing delay  $t_d$  (relative to CLKIN) can vary between 135 ns to 235 ns over the military temperature range and over  $\pm 10\%$  supply variation
3.  $\overline{EOC}$  returns high in 4 CLKIN cycles if  $A0 = 1$  and  $\overline{CS} = \overline{RD} = 0$  (Microprocessor Independent Mode); within 4 CLKIN cycles after a data read (Microprocessor Mode); or 4 CLKIN cycles after  $\overline{HOLD} = 0$  is recognized on a rising edge of CLKIN/4.

Figure 9. Serial Output Timing

quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f<sub>peak</sub>" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CS5012A/14/16 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is between 2.5 and 4.5 V for the CS5012A and 4.5 V for the CS5014/16. The CS5012A/14/16 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1 μF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult the application note: *Voltage References for the CS501X Series of A/D Converters*. For an example of using the CS5012A/14/16 with a 5 volt reference, see the application note: *A Collection of Application Hints for the CS501X Series of A/D Converters*.

### Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six CLKIN cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is

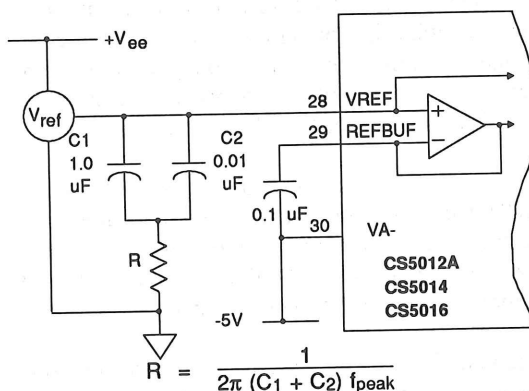


Figure 10. Reference Connections

required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 illustrates this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

The acquisition time of the CS5012A/14/16 depends on the CLKIN frequency. This is due to a fixed pre-charge period. For instance, operating the CS5012A -12, CS5014 -14 or CS5016 -16 version with an external 4 MHz CLKIN results in a 3.75 μs acquisition time: 1.5 μs for pre-charging (6 clock cycles) and 2.25 μs for fine-charging. Fine-charge settling is specified as a maximum of 2.25 μs for an analog source impedance of less than 200 Ω. (For the CS5012A -7 version it is specified as 1.32 μs.) In addition, the comparator requires a source impedance of less than 400 Ω around 2 MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200 pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more

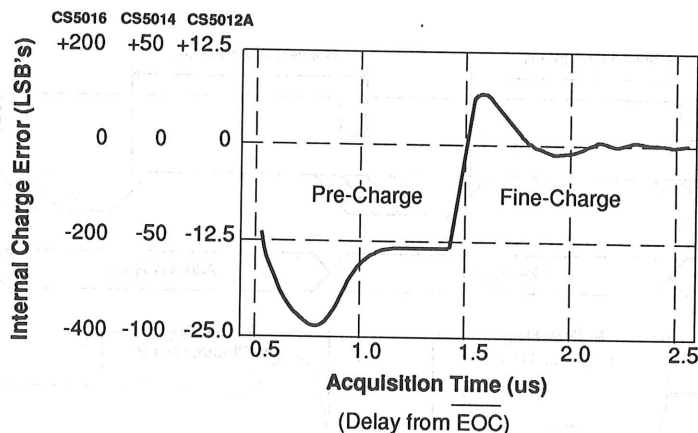


Figure 11. Internal Acquisition Time

information on input applications, consult the application note: *Input Buffer Amplifiers for the CS501X Family of A/D Converters*.

During the first six clock cycles following a conversion (pre-charge) in unipolar mode, the CS5012A is capable of slewing at 20V/ $\mu$ s and the CS5014/16 can slew at 5V/ $\mu$ s. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5012A can slew at 40V/ $\mu$ s, and the CS5014/16 can slew at 10V/ $\mu$ s. After the first six CLKIN cycles, the CS5012A will slew at 1.25V/ $\mu$ s in unipolar mode and 3.0V/ $\mu$ s in bipolar mode, and the CS5014/16 will slew at 0.25V/ $\mu$ s in unipolar mode and 0.5V/ $\mu$ s in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CS5012A/14/16 is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the CS5012A/14/16 can convert at full speed.

### Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/ $\overline{UP}$  low), the first code transition occurs

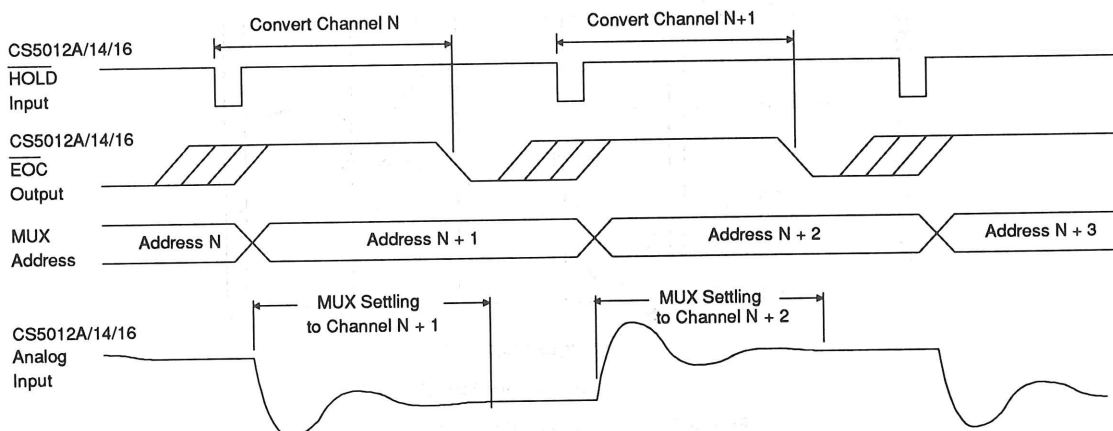
0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/ $\overline{UP}$  high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of all ones, and negative full scale gives a digital output of all zeros.

The BP/ $\overline{UP}$  mode pin may be switched after calibration without having to recalibrate the converter. However, the BP/ $\overline{UP}$  mode should be changed during the previous conversion cycle, that is, between  $\overline{HOLD}$  falling and  $\overline{EOC}$  falling. If BP/ $\overline{UP}$  is changed at any other time, one dummy conversion cycle must be allowed for proper acquisition of the input.

### Grounding and Power Supply Decoupling

The CS5012A/14/16 use the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used





**Figure 12. Pipelined MUX Input Channels**

as the entire system's analog ground reference point.

The digital and analog supplies to the CS5012A/14/16 are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1  $\mu$ F ceramic capacitors. If significant low-frequency noise is present on the supplies, 1  $\mu$ F tantalum capacitors are recommended in parallel with the 0.1  $\mu$ F capacitors.

*The positive digital power supply of the CS5012A/14/16 must never exceed the positive analog supply by more than a diode drop or the device could experience permanent damage.* If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram in Figure 36 shows a decoupling scheme which allows the CS5012A/14/16 to be powered from a single set of  $\pm 5$ V rails.

As with any high-precision A/D converter, the CS5012A/14/16 require careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to proper-

ly apply the device. The CDB5012/14/16 evaluation board is available for the CS5012A/14/16, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5012A/14/16, and can be quickly reconfigured to simulate any combination of sampling, calibration, CLKIN, and analog input range conditions.



### Power Supply Rejection

The CS5012A/14/16's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5012A/14/16's accuracy. This is because the CS5012A/14/16 adjust their offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 13 shows power supply rejection of the CS5012A/14/16 in the bipolar mode with the analog input grounded and a 300 mVp-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode.

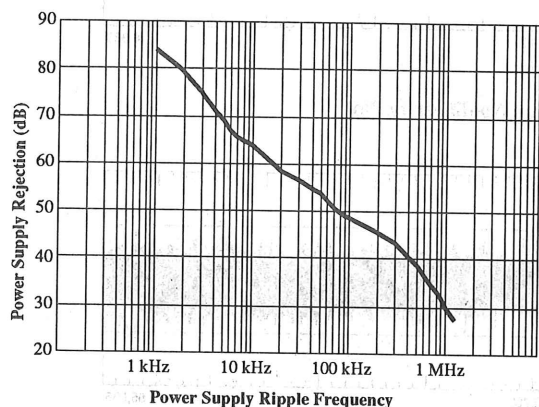


Figure 13. Power Supply Rejection

### CS5012A/14/16 PERFORMANCE

#### Differential Nonlinearity

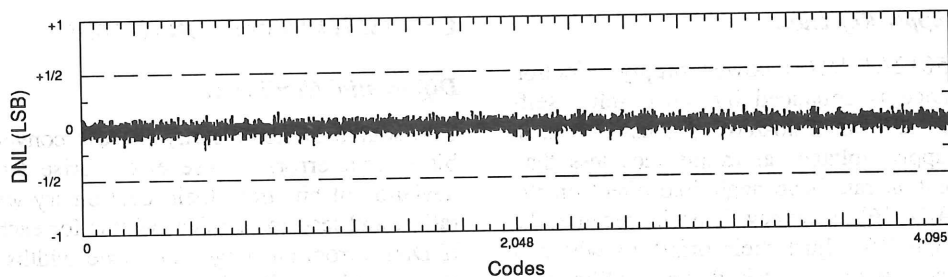
One source of nonlinearity in A/D converters is bit weight errors. These errors arise from the deviation of bits from their ideal binary-weighted ratios, and lead to nonideal widths for each code. If DNL errors are large, and code widths shrink to zero, it is possible for one or more codes to be entirely missing. The CS5012A/14/16 calibrate all bits in the capacitor array to a small fraction of an LSB resulting in nearly ideal DNL. Histogram plots of typical DNL of the CS5012A/14/16 can be seen in Figures 14, 16, 17. Figure 15 illustrates the DNL of the CS5012 for comparison with the CS5012A (Figure 14).

A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

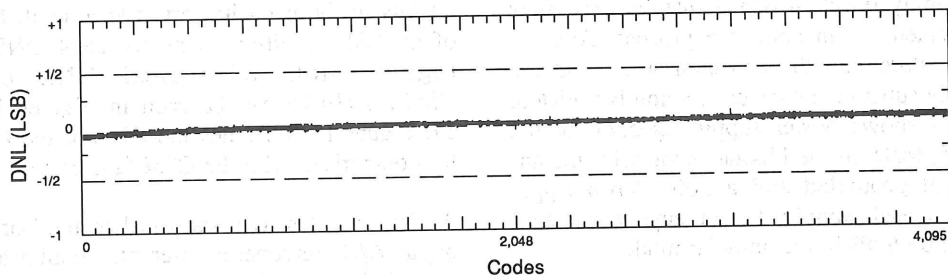
#### Integral Nonlinearity

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows in the transfer curve generate harmonic distortion. The worst-case condition of bit-weight errors (DNL) has traditionally also defined the point of maximum INL.

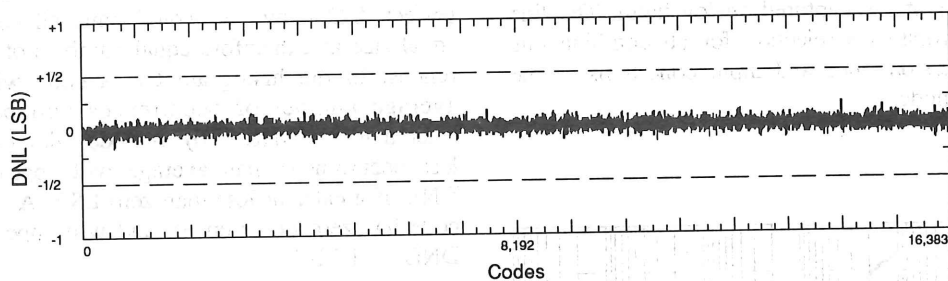
Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the



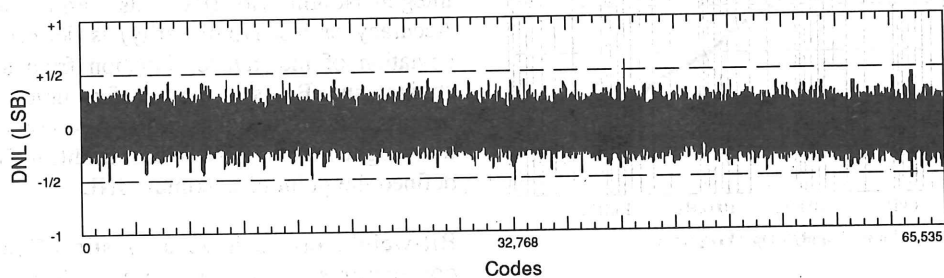
**Figure 14. CS5012A Differential Nonlinearity Plot**



**Figure 15. CS5012 Differential Nonlinearity Plot**



**Figure 16. CS5014 Differential Nonlinearity Plot**



**Figure 17. CS5016 Differential Nonlinearity Plot**

input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

The CS5012A/14/16 achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The CS5012A calibrates its bit weight errors to a small fraction of an LSB at 12-bits yielding peak distortion below the noise floor (see Figure 19). The CS5014 calibrates its bit weights to within  $\pm 1/16$  LSB at 14-bits ( $\pm 0.004\%$  FS) yielding peak distortion as low as -105 dB (see Figure 22). The CS5016 calibrates its bit weights to within  $\pm 1/4$  LSB at 16-bits ( $\pm 0.004\%$  FS) yielding peak distortion as low as -105 dB (see Figure 24). Unlike traditional ADC's, the linearity of the CS5012A/14/16 are not limited by bit-weight errors; their performance is therefore extremely repeatable and independent of input signal conditions.

### Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is  $\pm 1/2$  LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to  $\pm 1/2$  LSB, but any value within this range has equal probability of occurrence. Such a probability distribution leads to an error "signal" with an rms value of  $1 \text{ LSB}/\sqrt{12}$ . Using an rms signal value of  $\text{FS}/\sqrt{8}$  (amplitude =  $\text{FS}/2$ ), this relates to ideal 12, 14 and 16-bit signal-to-noise ratios of 74, 86 and 98 dB respectively.

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out, and improved system performance can be attained.

### FFT Tests and Windowing

In the factory, the CS5012A/14/16 are tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CS5012A/14/16, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5012A/14/16.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

Figure 18 shows an FFT computed from an ideal 12-bit sinewave. The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CS5014 and CS5016 has a maximum side-lobe level of -92 dB.

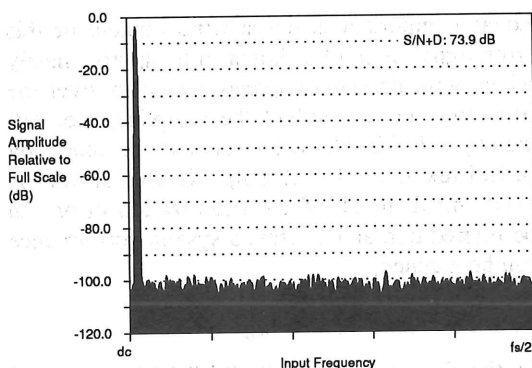


Figure 18. Plot of Ideal 12-bit ADC

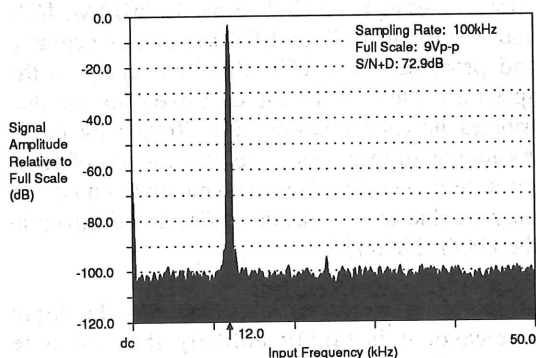


Figure 20. FFT Plot of CS5012A with 12 kHz Full-Scale Input

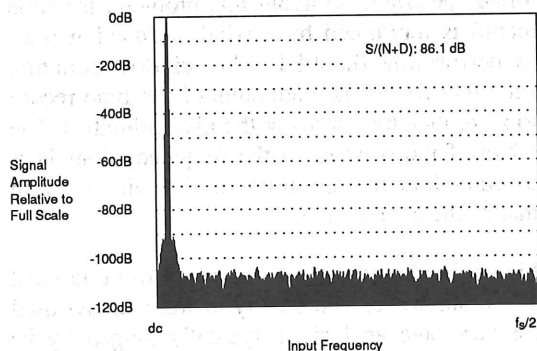


Figure 21. Plot of Ideal 14-bit ADC

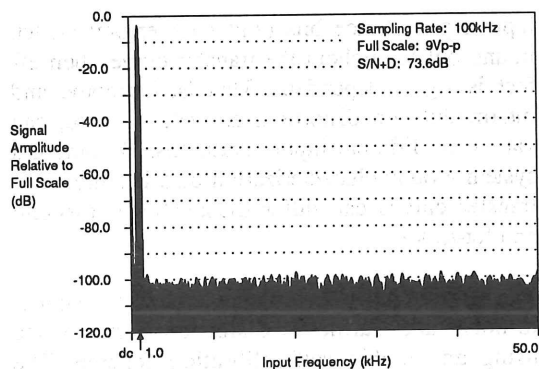


Figure 19. Plot of CS5012A with 1 kHz Full Scale Input

Figures 21 and 23 show FFT plots computed from an ideal 14 and 16-bit sine wave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten 1024 point time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics which exist above the noise floor and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic

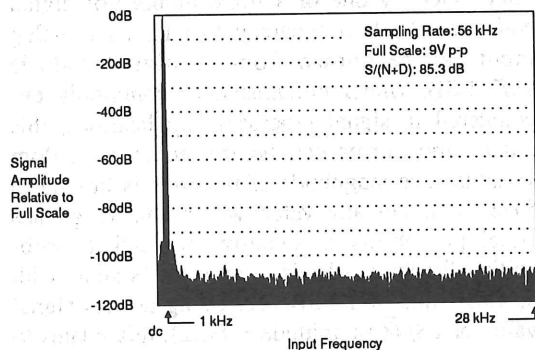


Figure 22. CS5014 FFT plot with 1 kHz Full Scale Input

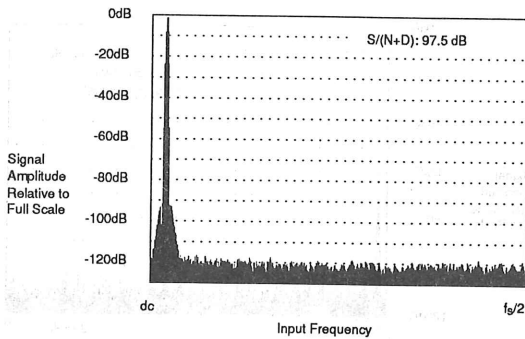


Figure 23. Plot of Ideal 16-bit ADC

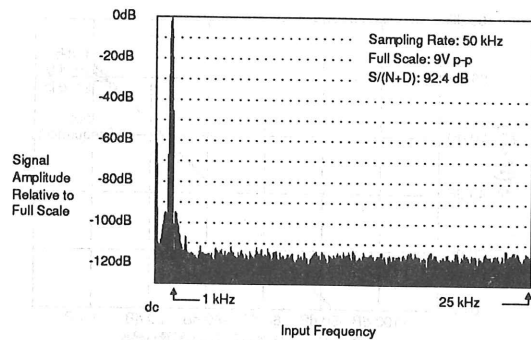


Figure 24. CS5016 FFT plot with 1 kHz Full Scale Input

analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Crystal Semiconductor.

Figures 19, 22, and 24 show the performance of the CS5012A/14/16 with 1kHz full scale inputs. Figure 20 shows CS5012A performance with 12kHz full scale inputs. Notice that the performance CS5012A/14/16 closely approaches that of the corresponding ideal ADC.

### CS5012A High Frequency Performance

The CS5012A performs very well over a wide range of input frequencies as shown in Figure 25. The figure depicts the CS5012A-KP7 tested under four different conditions. The conditions include tests with the voltage reference set at 4.5 and at 2.5 volts with input signals at 0.5 dB down from full scale and 6.0 dB down from full scale. The sample rate is at 100 kHz for all cases. The plots indicate that the part performs very well even with input frequencies above the Nyquist rate. Best performance at the higher frequencies is achieved with a 2.5 volt reference.

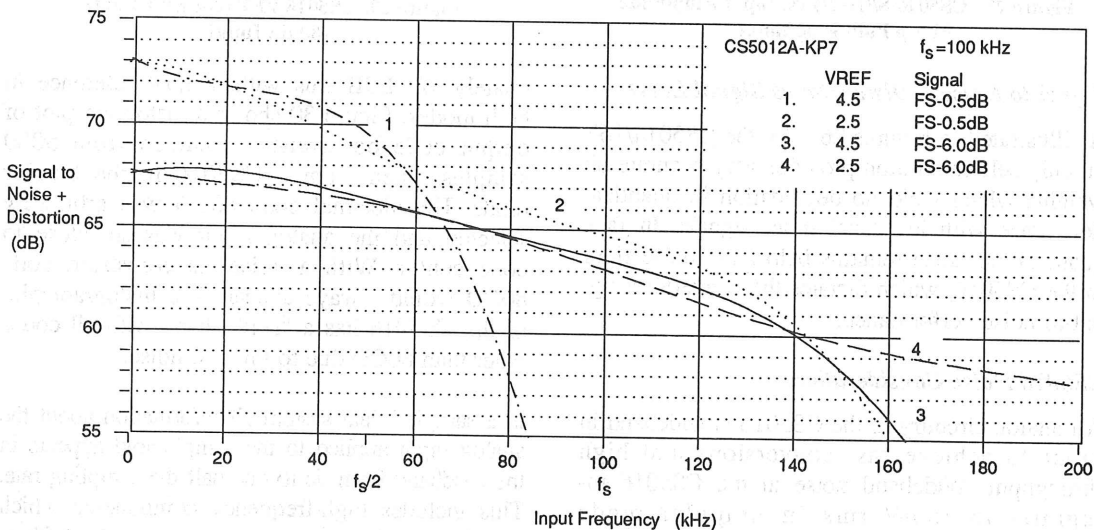


Figure 25. CS5012A High Frequency Input Performance

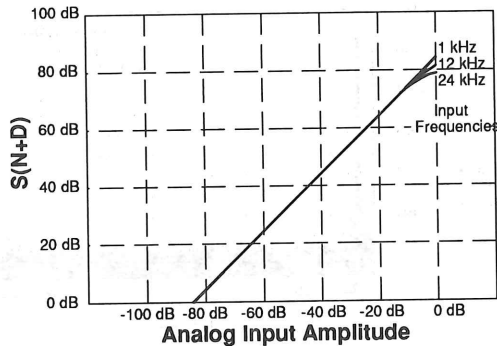


Figure 26. CS5014 S/(N+D) vs. Input Amplitude (9Vp-p Full-Scale Input)

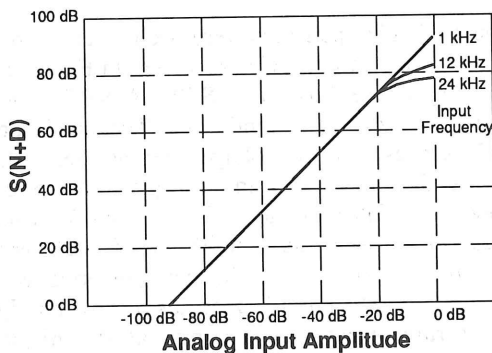


Figure 28. CS5016 S/(N+D) vs. Input Amplitude (9Vp-p Full-Scale Input)

## Signal to Noise + Distortion vs Signal Level

As illustrated in Figures 26 - 29, the CS5014/16's on-chip self-calibration provides very accurate bit weights which yield no degradation in quantization noise with low-level input signals. In fact, quantization noise remains below the noise floor in the CS5016, which dictates the converter's signal-to-noise performance.

## CS5016 Noise Considerations

All analog circuitry in the CS5016 is wideband in order to achieve fast conversions and high throughput. Wideband noise in the CS5016 integrates to 35 mV rms in unipolar mode (70 mV rms in bipolar mode). This is approx-

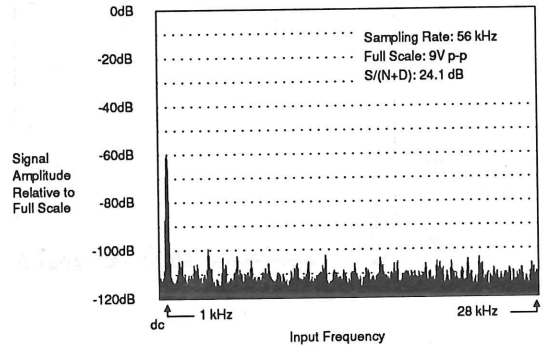


Figure 27. CS5014 FFT plot with 1 kHz -60 dB Input

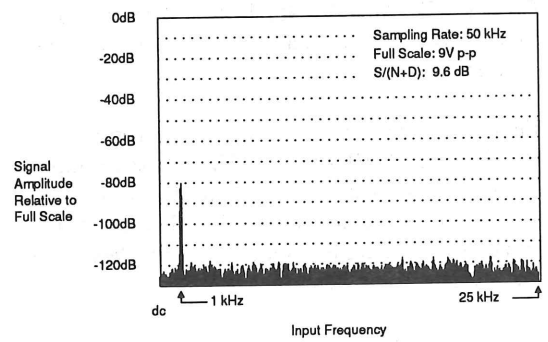
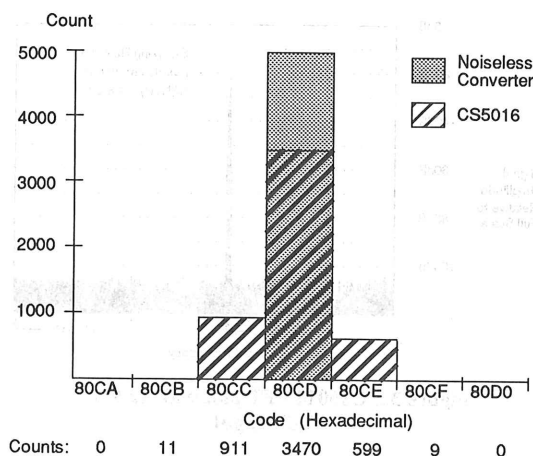


Figure 29. CS5016 FFT plot with 1 kHz -80 dB Input

imately 1/2 LSB rms with a 4.5V reference in both modes. Figure 30 shows a histogram plot of output code occurrences obtained from 5000 samples taken from a CS5016 in the bipolar mode. Hexadecimal code 80CD was arbitrarily selected and the analog input was set close to code center. With a noiseless converter, code 80CD would always appear. The histogram plot of the CS5016 has a "bell" shape with all codes other than 80CD due to internal noise.

In a sampled data system all information about the analog input applied to the sample/hold appears in the baseband from dc to one-half the sampling rate. This includes high-frequency components which alias into the baseband. Low-pass (anti-alias) filters





**Figure 30. Histogram Plot of 5000 Conversion Inputs from the CS5016**

are therefore used to remove frequency components in the input signal which are above one-half the sample rate. However, all wideband noise introduced by the CS5016 still aliases into the baseband. This "white" noise is evenly spread from dc to one-half the sampling rate and integrates to 35 mV rms in unipolar mode.

Noise can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the CS5016's noise over a wider band (for lower noise density), and averaging applies a low-pass response which filters noise above the desired signal bandwidth. In general, the CS5016's noise performance can be maximized in any application by always sampling at the maximum specified rate of 50 kHz (for lowest noise density) and digitally filtering to the desired signal bandwidth.

### CS5014 and CS5016 Sampling Distortion

The ultimate limitation on the CS5014/16's linearity (and distortion) arises from nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually

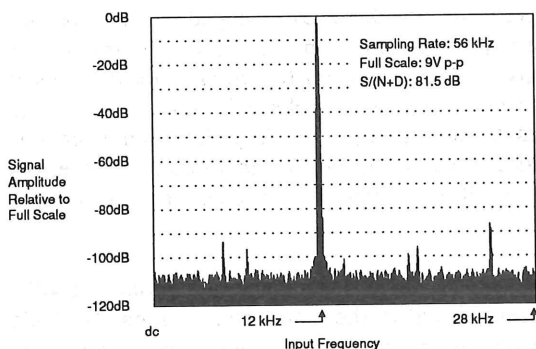
performed on the charge trapped on the capacitor array at the moment the  $\overline{\text{HOLD}}$  command is given. The charge on the array is ideally related to the analog input voltage by  $Q_{in} = -V_{in} \times C_{tot}$  as shown in Figure 2. Any deviation from this ideal relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between charge  $Q_{in}$  and the analog input voltage  $V_{in}$  and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figures 22 and 24).

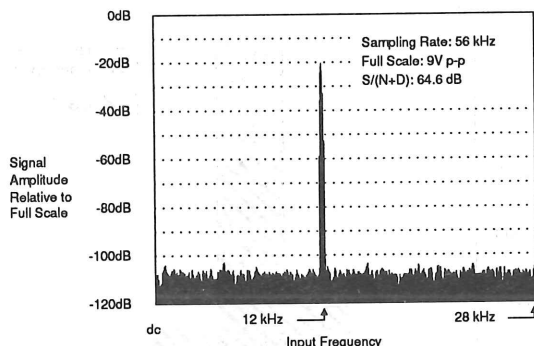
The ideal relationship between  $Q_{in}$  and  $V_{in}$  can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency as shown in Figures 26 and 28 since the magnitude of the steady state current increases. First noticeable at 1 kHz, this distortion assumes a linear relationship with input frequency. With signals 20 dB or more below full-scale, it no longer dominates the converter's overall S/(N+D) performance (Figures 31-34).

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the CS5014/16 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's  $\overline{\text{HOLD}}$  input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

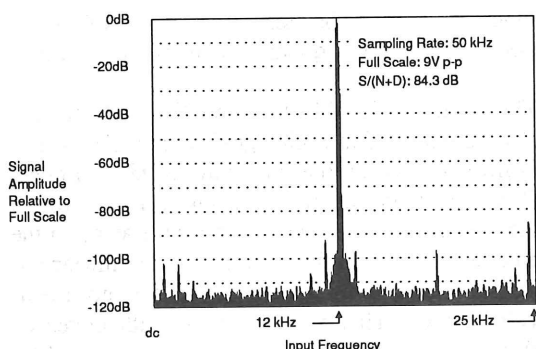




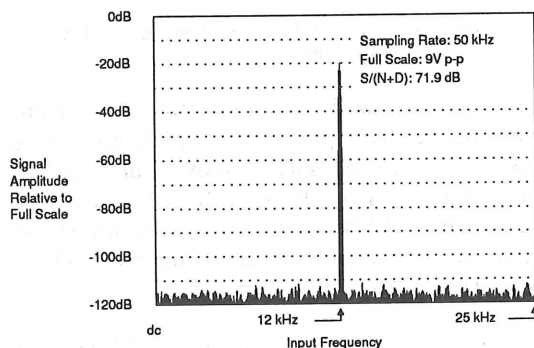
**Figure 31. CS5014 FFT plot with 12 kHz Full Scale Input**



**Figure 32. CS5014 FFT plot with 12 kHz -20 dB Input**



**Figure 33. CS5016 FFT plot with 12 kHz Full Scale Input**



**Figure 34. CS5016 FFT plot with 12 kHz -20 dB Input**

### Clock Feedthrough in the CS5014 and CS5016

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CS5014/16 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CS5014/16's analog input and master clock.

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the HOLD input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CS5014/16's output. The offset could theoretically reach the peak coupling magnitude

Master Clock In/Ext	Freq	Analog Input Source Impedance	Clock Feedthrough	
			RMS	Peak-to-Peak
Internal	2MHz	50 $\Omega$	15uV	70uV
External	2MHz	50 $\Omega$	25uV	110uV
External	4MHz	50 $\Omega$	40uV	150uV
External	4MHz	25 $\Omega$	25uV	110uV
External	4MHz	200 $\Omega$	80uV	325uV

**Figure 35. Examples of Measured Clock Feedthrough**

(Figure 35), but the probability of this occurring is small since the peaks are spikes of short duration.

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an

ac error at the CS5014/16's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{\text{tone}} = (N f_s - f_{\text{clk}})$$

where  $N = f_{\text{clk}}/f_s$  rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CS5014/16's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 35, a typical CS5014/16 operating with their internal oscillator at 2 MHz and 50  $\Omega$  of analog input source impedance will exhibit only 15  $\mu\text{V}$  rms of clock feedthrough. However, if a 2 MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25  $\mu\text{V}$  rms. Feedthrough also increases with clock frequency; a 4 MHz clock yields 40  $\mu\text{V}$  rms.

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 35, reducing source impedance from 50  $\Omega$  to 25  $\Omega$  yields a 15  $\mu\text{V}$  rms reduction in feedthrough. Therefore, when operating the CS5014/16 with high-frequency external master clocks, it is important to minimize source impedance applied to the CS5014/16's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CS5014/16 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

### Differences between the CS5012A and the CS5012

The differences between the CS5012A and the CS5012 are tabulated in Table 3. The CS5012 is a short-cycled version of the CS5016 A/D converter and includes the same 18-bit calibration circuitry. This calibration circuitry sets the calibration resolution of the CS5012 at 1/64th of an LSB and achieves the near perfect differential linearity performance illustrated by the CS5012 DNL plot in Figure 15. The CS5012A calibration circuitry was modified to provide calibration to 15-bit resolution therefore achieving calibration to 1/8 of an LSB. This reduction in calibration resolution for the CS5012A reduces the time required to calibrate the device (see Table 3) and reduces the size of the total array capacitance. The reduced array capacitance improves the high frequency performance by allowing higher slew rate in the input circuitry.

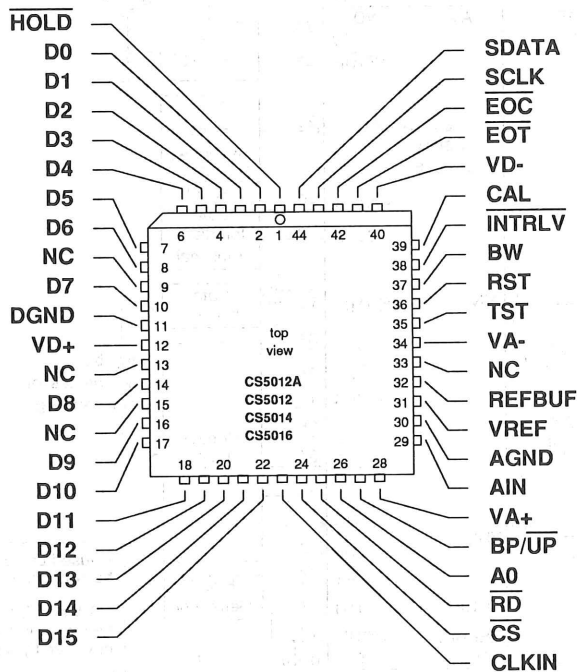
Table 3 documents some other improvements included in the CS5012A. The burst mode calibration, while not generally needed, was made functional. The device was also modified so the  $\overline{\text{EOC}}$  signal goes low at the end of a reset calibration in either microprocessor or microprocessor-independent mode. The CS5012A was modified to maintain a throughput rate of 64 CLKIN cycles in loopback mode for all frequencies of CLKIN.

	<b>CS5012A</b>	<b>CS5012</b>
Calibration resolution	15 bits. Results in DNL calibration to 1/8 LSB at 12 bits.	18 bits. Results in DNL calibration to 1/64 LSB at 12 bits.
Calibration time reset: interleave: burst:	58,280 CLKIN cycles 2,014 conversions fully functional	1,441,020 CLKIN cycles 72,051 conversions not functional
End of calibration indicator	EOC falls in either microprocessor or microprocessor-independent mode at the completion of a RESET calibration cycle.	EOC falls at the completion of a RESET calibration cycle in microprocessor mode only. In microprocessor-independent mode EOT must be used. EOT falls 15 CLKIN cycles after completion of a RESET calibration.
Throughput rate in loopback mode	The device acquires and converts a sample in 64 CLKIN cycles for all CLKIN frequencies when in loopback.	The device acquires and converts in 64 CLKIN cycles for CLKIN=4MHz, but will require 68 CLKIN cycles at 100kHz throughput. This is due to excess delay on EOT.
Input capacitance in fine-charge mode	103pF typical, unipolar mode 72pF typical, bipolar mode	275pF typical, unipolar mode 165pF typical, bipolar mode
Slew Rate Unipolar Coarse charge Fine charge Bipolar Coarse charge Fine charge	20V/us 1.5V/us  40V/us 3.0V/us	5V/us 0.25V/us  10V/us 0.5V/us

**Table 3. Differences Between the CS5012A and CS5012**



	HOLD	1	40	SDATA	SERIAL OUTPUT
CS5016 (LSB) DATA BUS BIT 0	D0	2	39	SCLK	SERIAL CLOCK
DATA BUS BIT 1	D1	3	38	EOC	END OF CONVERSION
CS5014 (LSB) DATA BUS BIT 2	D2	4	37	EOT	END OF TRACK
DATA BUS BIT 3	D3	5	36	VD-	NEGATIVE DIGITAL POWER
CS5012 (LSB) DATA BUS BIT 4	D4	6	35	CAL	CALIBRATE
DATA BUS BIT 5	D5	7	34	INTRLV	INTERLEAVE
DATA BUS BIT 6	D6	8	33	BW	BUS WIDTH SELECT
DATA BUS BIT 7	D7	9	32	RST	RESET
DIGITAL GROUND	DGND	10	31	TST	TEST
POSITIVE DIGITAL POWER	VD+	11	30	VA-	NEGATIVE ANALOG POWER
DATA BUS BIT 8	D8	12	29	REFBUF	REFERENCE BUFFER OUTPUT
DATA BUS BIT 9	D9	13	28	VREF	VOLTAGE REFERENCE
DATA BUS BIT 10	D10	14	27	AGND	ANALOG GROUND
DATA BUS BIT 11	D11	15	26	AIN	ANALOG INPUT
DATA BUS BIT 12	D12	16	25	VA+	POSITIVE ANALOG POWER
DATA BUS BIT 13	D13	17	24	BP/UP	BIPOLAR/UNIPOLAR SELECT
DATA BUS BIT 14	D14	18	23	A0	READ ADDRESS
(MSB) DATA BUS BIT 15	D15	19	22	RD	READ
CLOCK INPUT	CLKIN	20	21	CS	CHIP SELECT



NOTE: All pin references in this data sheet refer to the 40-pin DIP package numbering. Use this figure to determine pin numbers for 44-pin package.

**PIN DESCRIPTIONS****Power Supply Connections****VD+ – Positive Digital Power, PIN 11.**

Positive digital power supply. Nominally +5 volts.

**VD- – Negative Digital Power, PIN 36.**

Negative digital power supply. Nominally -5 volts.

**DGND – Digital Ground, PIN 10.**

Digital ground.

**VA+ – Positive Analog Power, PIN 25.**

Positive analog power supply. Nominally +5 volts.

**VA- – Negative Analog Power, PIN 30.**

Negative analog power supply. Nominally -5 volts.

**AGND – Analog Ground, PIN 27.**

Analog ground.

**Oscillator****CLKIN – Clock Input, PIN 20.**

All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

**Digital Inputs****HOLD – Hold, PIN 1.**

A falling transition on this pin sets the CS5012A/14/16 to the hold state and initiates a conversion. This input must remain low at least one CLKIN cycle plus 50 ns.

 **$\overline{\text{CS}}$  – Chip Select, PIN 21.**

When high, the data bus outputs are held in a high impedance state and the input to CAL and INTRLV are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and INTRLV) and a rising transition latches both the CAL and INTRLV inputs. If RD is low, the data bus is driven as indicated by BW and A0.

 **$\overline{\text{RD}}$  – Read, PIN 22.**

When RD and  $\overline{\text{CS}}$  are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

**A0 – Read Address, PIN 23.**

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

**BP/ $\overline{\text{UP}}$  – Bipolar/Unipolar Input Select, PIN 24.**

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar encoding is in straight binary format. Once calibration has been performed, either bipolar or unipolar mode may be selected without the need to recalibrate.

**RST – Reset, PIN 32.**

When taken high for at least 100 ns, all internal digital logic is reset. Upon being taken low, a full calibration sequence is initiated.

**BW – Bus Width Select, PIN 33.**

When hard-wired high, all 12 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D0-D7. A second read cycle places the four LSB's with four trailing zeros on D0-D7. Subsequent reads will toggle the higher/lower order byte. Regardless of BW's status, a read cycle with A0 low yields the status information on D0-D7.

 **$\overline{\text{INTRLV}}$  – Interleave, PIN 34.**

When latched low using  $\overline{\text{CS}}$ , the device goes into interleave calibration mode. A full calibration will complete every 2,014 conversions in the CS5012A, and every 72,051 conversions in the CS5014/16. The effective conversion time extends by 20 clock cycles.

**CAL – Calibrate, PIN 35. (See Addendum appending this data sheet))**

When latched high using  $\overline{\text{CS}}$ , burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 58,280 CLKIN cycles in the CS5012A, and every 1,441,020 CLKIN cycles in the CS5014/16. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning.

**Analog Inputs****AIN – Analog Input, PIN 26.**

Input range in the unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200  $\Omega$ .

**VREF – Voltage Reference, PIN 28.**

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.



## Digital Outputs

### D0 through D15 – Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

3-state output pins. Enabled by  $\overline{CS}$  and  $\overline{RD}$ , they offer the converter's output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer status register data.

### $\overline{EOT}$ – End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal.

### $\overline{EOC}$ – End Of Conversion, PIN 38.

This output indicates the end of a conversion or calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

### SDATA – Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

### SCLK – Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CS5012A/14/16. Serial data is stable on the rising edge of SCLK.

## Analog Outputs

### REFBUF – Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1  $\mu F$  ceramic capacitor must be tied between this pin and VA-.

## Miscellaneous

### TST – Test, PIN 31.

Allows access to the CS5012A/14/16's test functions which are reserved for factory use. Must be tied to DGND.

## PARAMETER DEFINITIONS

### Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

### Differential Linearity

Minimum resolution for which no missing codes is guaranteed. Units in bits.

### Full Scale Error

The deviation of the last code transition from the ideal ( $V_{REF}/2$  LSB's). Units in LSB's.

### Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

### Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/UP high). Units in LSB's.

### Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/UP high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

### Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise)

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

### Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

### Signal-to-Noise Ratio

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

### Aperture Time

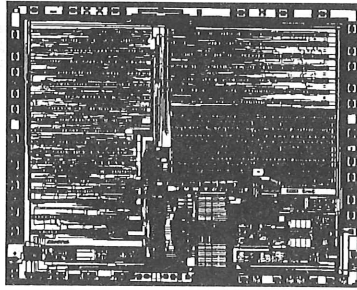
The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

### Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

*NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.*

## DIE INFORMATION



CS5012-YU  
CS5014-YU  
CS5016-YU

3

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

**Assembly Information**

1. CS5012, CS5014, CS5016 die size shall be 0.270" by 0.337" ( $\pm 0.002$ ").
2. The die are suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.
3. Die thickness shall be 0.0175"  $\pm 0.0035$ ". If tighter tolerances are required, contact the factory.

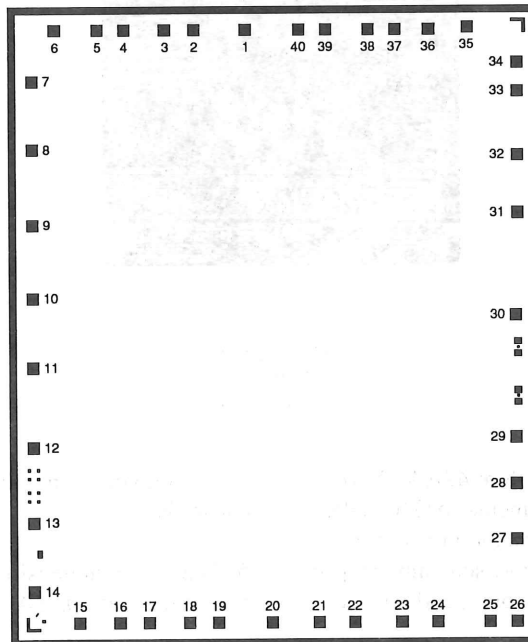
4. The maximum number of die per wafer pack carrier is 16.

5. The cavity dimensions for each die within the wafer pack are 0.350" by 0.350".

6. The die require no particular bonding sequence.

7. Each pin of the CS5012, CS5014, CS5016 has ESD and latch-up protection circuitry. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.

8. Technical constraints limit the viability of accurate performance measurements of precision analog IC's at wafer probe. Although high yield to the limits listed in the specification tables is anticipated, no guarantee is given for unpackaged die product.

**Bonding Diagram for CS5012-YU, CS5014-YU, CS5016-YU**


1 - $\overline{\text{HOLD}}$	21 - $\overline{\text{CS}}$
2 - D0	22 - $\overline{\text{RD}}$
3 - D1	23 - A0
4 - D2	24 - BP/UP
5 - D3	25 - VA+
6 - D4	26 - AIN
7 - D5	27 - AGND
8 - D6	28 - VREF
9 - D7	29 - REFBUF
10 - DGND	30 - VA-
11 - VD+	31 - TST
12 - D8	32 - RST
13 - D9	33 - BW
14 - D10	34 - $\overline{\text{INTRLV}}$
15 - D11	35 - CAL
16 - D12	36 - VD-
17 - D13	37 - $\overline{\text{EOT}}$
18 - D14	38 - $\overline{\text{EOC}}$
19 - D15	39 - SCLK
20 - CLKIN	40 - SDATA

### CS5012A Ordering Guide

Model	Throughput	Conversion Time	Maximum DNL	Temp. Range	Package
CS5012A-KP12	63 kHz	12.25 $\mu$ s	$\pm 1/2$ LSB	0 to 70 $^{\circ}$ C	40-Pin Plastic DIP
CS5012A-KP7	100 kHz	7.20 $\mu$ s	$\pm 1/2$ LSB	0 to 70 $^{\circ}$ C	40-Pin Plastic DIP
CS5012A-KL12	63 kHz	12.25 $\mu$ s	$\pm 1/2$ LSB	0 to 70 $^{\circ}$ C	44-Pin PLCC
CS5012A-KL7	100 kHz	7.20 $\mu$ s	$\pm 1/2$ LSB	0 to 70 $^{\circ}$ C	44-Pin PLCC
CS5012A-BP12	63 kHz	12.25 $\mu$ s	$\pm 1/2$ LSB	-40 to +85 $^{\circ}$ C	40-Pin Plastic DIP
CS5012A-BP7	100 kHz	7.20 $\mu$ s	$\pm 1/2$ LSB	-40 to +85 $^{\circ}$ C	40-Pin Plastic DIP
CS5012A-BL12	63 kHz	12.25 $\mu$ s	$\pm 1/2$ LSB	-40 to +85 $^{\circ}$ C	44-Pin PLCC
CS5012A-BL7	100 kHz	7.20 $\mu$ s	$\pm 1/2$ LSB	-40 to +85 $^{\circ}$ C	44-Pin PLCC
*CS5012-KP24	34 kHz	24.50 $\mu$ s	$\pm 1/2$ LSB	0 to 70 $^{\circ}$ C	40-Pin Plastic DIP
*CS5012-KP12	63 kHz	12.25 $\mu$ s	$\pm 1/2$ LSB	0 to 70 $^{\circ}$ C	40-Pin Plastic DIP
*CS5012-KL24	34 kHz	24.50 $\mu$ s	$\pm 1/2$ LSB	0 to 70 $^{\circ}$ C	44-Pin PLCC
*CS5012-KL12	63 kHz	12.25 $\mu$ s	$\pm 1/2$ LSB	0 to 70 $^{\circ}$ C	44-Pin PLCC
*CS5012-BP24	34 kHz	24.50 $\mu$ s	$\pm 1/2$ LSB	-40 to +85 $^{\circ}$ C	40-Pin CerDIP
*CS5012-BP12	63 kHz	12.25 $\mu$ s	$\pm 1/2$ LSB	-40 to +85 $^{\circ}$ C	40-Pin CerDIP
*CS5012-BL24	34 kHz	24.50 $\mu$ s	$\pm 1/2$ LSB	-40 to +85 $^{\circ}$ C	44-Pin PLCC
*CS5012-BL12	63 kHz	12.25 $\mu$ s	$\pm 1/2$ LSB	-40 to +85 $^{\circ}$ C	44-Pin PLCC
CS5012-TD24	34 kHz	24.50 $\mu$ s	$\pm 1/2$ LSB	-55 to +125 $^{\circ}$ C	40-Pin CerDIP
CS5012-TD12	63 kHz	12.25 $\mu$ s	$\pm 1/2$ LSB	-55 to +125 $^{\circ}$ C	40-Pin CerDIP
CS5012-TE24	34 kHz	24.50 $\mu$ s	$\pm 1/2$ LSB	-55 to +125 $^{\circ}$ C	44-Pin Ceramic LCC
CS5012-TE12	63 kHz	12.25 $\mu$ s	$\pm 1/2$ LSB	-55 to +125 $^{\circ}$ C	44-Pin Ceramic LCC

CS5012-YU

Unpackaged Die

\*The CS5012A is recommended for new designs. The following table shows the upgrade parts.

Old Part Number	New Design Recommended Device.
CS5012-KP24	CS5012A-KP12
CS5012-KP12	CS5012A-KP12
CS5012-KP7	CS5012A-KP7
CS5012-KL24	CS5012A-KL12
CS5012-KL12	CS5012A-KL12
CS5012-KL7	CS5012A-KL7
CS5012-BD24	CS5012A-BP12
CS5012-BD12	CS5012A-BP12
CS5012-BD7	CS5012A-BP7
CS5012-BL24	CS5012A-BL12
CS5012-BL12	CS5012A-BL12
CS5012-BL7	CS5012A-BL7

### MIL-STD-883B Rev C. Versions

SMD Number: 5962-89679

Refer to SMD for ordering information, which includes accuracy and package suffixes.

## CS5014 Ordering Guide

<u>Model</u>	<u>Throughput</u>	<u>Conversion Time</u>	<u>Linearity</u>	<u>Temp. Range</u>	<u>Package</u>
CS5014-KP28	28 kHz	28.50 $\mu$ s	$\pm 0.5$ LSB	0 to 70 $^{\circ}$ C	40-Pin Plastic DIP
CS5014-KP14	56 kHz	14.25 $\mu$ s	$\pm 0.5$ LSB	0 to 70 $^{\circ}$ C	40-Pin Plastic DIP
CS5014-KL28	28 kHz	28.50 $\mu$ s	$\pm 0.5$ LSB	0 to 70 $^{\circ}$ C	44-Pin PLCC
CS5014-KL14	56 kHz	14.25 $\mu$ s	$\pm 0.5$ LSB	0 to 70 $^{\circ}$ C	44-Pin PLCC
CS5014-BP28	28 kHz	28.50 $\mu$ s	$\pm 0.5$ LSB	-40 to +85 $^{\circ}$ C	40-Pin Plastic DIP
CS5014-BP14	56 kHz	14.25 $\mu$ s	$\pm 0.5$ LSB	-40 to +85 $^{\circ}$ C	40-Pin Plastic DIP
CS5014-BL28	28 kHz	28.50 $\mu$ s	$\pm 0.5$ LSB	-40 to +85 $^{\circ}$ C	44-Pin PLCC
CS5014-BL14	56 kHz	14.25 $\mu$ s	$\pm 0.5$ LSB	-40 to +85 $^{\circ}$ C	44-Pin PLCC
CS5014-SD14	56 kHz	14.25 $\mu$ s	$\pm 1.5$ LSB	-55 to +125 $^{\circ}$ C	40-Pin CerDIP
CS5014-TD14	56 kHz	14.25 $\mu$ s	$\pm 0.5$ LSB	-55 to +125 $^{\circ}$ C	40-Pin CerDIP
CS5014-SE14	56 kHz	14.25 $\mu$ s	$\pm 1.5$ LSB	-55 to +125 $^{\circ}$ C	44-Pin Ceramic LCC
CS5014-TE14	56 kHz	14.25 $\mu$ s	$\pm 0.5$ LSB	-55 to +125 $^{\circ}$ C	44-Pin Ceramic LCC

CS5014-YU

Unpackaged Die

### MIL-STD 883B Rev C. Versions

SMD Number: 5962-89674

Refer to SMD for ordering information, which includes accuracy and package suffixes.

## CS5016 Ordering Guide

<u>Model</u>	<u>Linearity</u>	<u>Signal to Noise Ratio</u>	<u>Conversion Time</u>	<u>Temp. Range</u>	<u>Package</u>
CS5016-JP32	.0030%	87 dB	32.50 $\mu$ s	0 to 70 $^{\circ}$ C	40-Pin Plastic DIP
CS5016-JP16	.0030%	87 dB	16.25 $\mu$ s	0 to 70 $^{\circ}$ C	40-Pin Plastic DIP
CS5016-KP32	.0015%	90 dB	32.50 $\mu$ s	0 to 70 $^{\circ}$ C	40-Pin Plastic DIP
CS5016-KP16	.0015%	90 dB	16.25 $\mu$ s	0 to 70 $^{\circ}$ C	40-Pin Plastic DIP
CS5016-JL32	.0030%	87 dB	32.50 $\mu$ s	0 to 70 $^{\circ}$ C	44-Pin PLCC
CS5016-JL16	.0030%	87 dB	16.25 $\mu$ s	0 to 70 $^{\circ}$ C	44-Pin PLCC
CS5016-KL32	.0015%	90 dB	32.50 $\mu$ s	0 to 70 $^{\circ}$ C	44-Pin PLCC
CS5016-KL16	.0015%	90 dB	16.25 $\mu$ s	0 to 70 $^{\circ}$ C	44-Pin PLCC
CS5016-AP32	.0030%	87 dB	32.50 $\mu$ s	-40 to +85 $^{\circ}$ C	40-Pin Plastic DIP
CS5016-AP16	.0030%	87 dB	16.25 $\mu$ s	-40 to +85 $^{\circ}$ C	40-Pin Plastic DIP
CS5016-BP32	.0015%	90 dB	32.50 $\mu$ s	-40 to +85 $^{\circ}$ C	40-Pin Plastic DIP
CS5016-BP16	.0015%	90 dB	16.25 $\mu$ s	-40 to +85 $^{\circ}$ C	40-Pin Plastic DIP
CS5016-AL32	.0030%	87 dB	32.50 $\mu$ s	-40 to +85 $^{\circ}$ C	44-Pin PLCC
CS5016-AL16	.0030%	87 dB	16.25 $\mu$ s	-40 to +85 $^{\circ}$ C	44-Pin PLCC
CS5016-BL32	.0015%	90 dB	32.50 $\mu$ s	-40 to +85 $^{\circ}$ C	44-Pin PLCC
CS5016-BL16	.0015%	90 dB	16.25 $\mu$ s	-40 to +85 $^{\circ}$ C	44-Pin PLCC
CS5016-SD16	.0076%	87 dB	16.25 $\mu$ s	-55 to +125 $^{\circ}$ C	40-Pin CerDIP
CS5016-TD16	.0015%	90 dB	16.25 $\mu$ s	-55 to +125 $^{\circ}$ C	40-Pin CerDIP
CS5016-SE16	.0076%	87 dB	16.25 $\mu$ s	-55 to +125 $^{\circ}$ C	44-Pin Ceramic LCC
CS5016-TE16	.0015%	90 dB	16.25 $\mu$ s	-55 to +125 $^{\circ}$ C	44-Pin Ceramic LCC

CS5016-YU

Unpackaged Die

### MIL-STD 883B Rev C. Versions

SMD Number: 5962-89676

Refer to SMD for ordering information, which includes accuracy and package suffixes.

## ADDENDUM

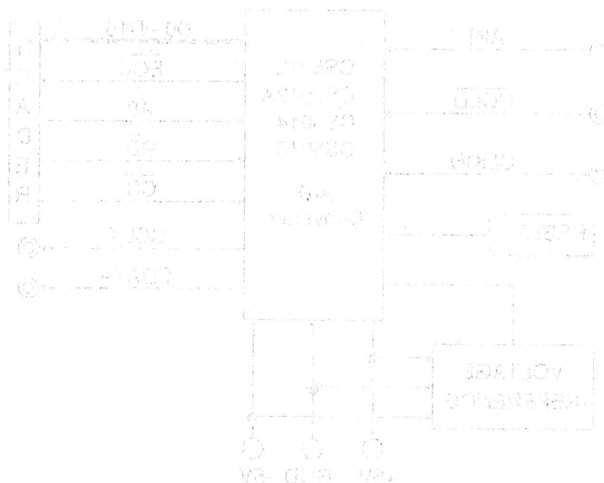
### *Burst Calibration*

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used in the CS5012, CS5014 or CS5016. The silicon for the CS5012A has been revised to prevent this effect.

Interleave calibration works perfectly, provided it is not used intermittently.

The reset calibration always works perfectly, and typically should be used instead of burst mode. The CS5012's and CS5012A/14/16's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset.

If you wish to use burst calibration, please contact the factory for advice and new part availability information.





## Evaluation Board for CS5012, CS5014, CS5016 ADC's

### Features

- Compatible with CS5012, CS5012A, CS5014, CS5016
- PC/uP-Compatible Header Connection
  - 16-Bit Parallel Data
  - End-of-Conversion Output
  - CS, RD, and A0 Control Inputs
- DIP-Switch Selectable:
  - Unipolar/Bipolar Input Range
  - Burst & Interleave Calibration Modes
  - Continuous Conversion
- Adjustable Voltage Reference
- Serial Data and Clock BNC Connections
- Operation from Internally-Generated or Externally-Supplied Master Clock

### General Description

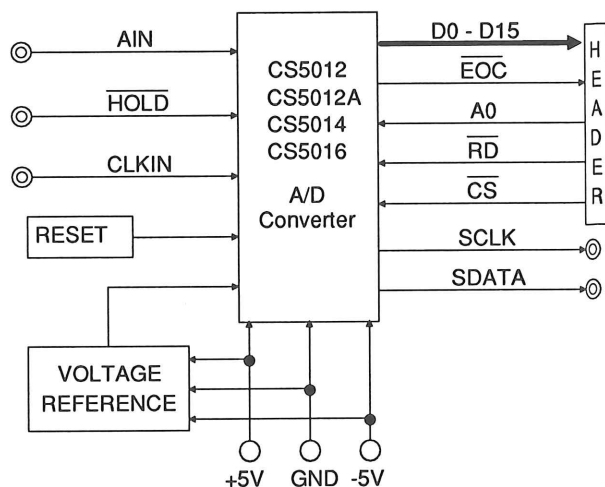
The CDB5012/4/6 is an evaluation board that eases the laboratory characterization of any of the CS5012, CS5012A, CS5014 and CS5016 A/D converters. The board can be easily reconfigured to simulate any combination of sampling, master clock, calibration, and input range conditions.

The converter's parallel output data are available at a 40 pin strip header allowing easy interfacing to PC's or microprocessor busses. Output data is also available in serial form at SCLK and SDATA coaxial BNC connectors.

Evaluation can also be performed over a wide range of input spans using the on-board reference circuitry. Furthermore, the CDB5012,4,6 features DIP-switch selectable unipolar/bipolar input ranges and two calibration modes: burst and interleave cal. Calibration can be initiated at any time by momentarily depressing a reset pushbutton.

**ORDERING INFORMATION:** CDB5012, CDB5012A, CDB5014, CDB5016

### Block Diagram



# Analog Input

The analog input to the A/D converter is supplied through the BNC coaxial connector labeled AIN. Analog input polarity is controlled by the first position switch on the DIP-switch, SW-1. If it is on, the input is unipolar ranging from GND to VREF. If the switch is off, the input range is bipolar with the magnitude of the reference voltage defining both zero- and full-scale ( $\pm VREF$ ).

The A/D converter's internal analog input buffer requires a source impedance of less than 400  $\Omega$  at 1MHz for stability. Acquisition and throughput are specified assuming a dc source impedance of less than 200  $\Omega$ . Infinitely large dc source impedances can be accommodated by adding capacitance (typically 1000pF) from the analog input to ground. However, high dc source resistances degrade acquisition time and consequently throughput.

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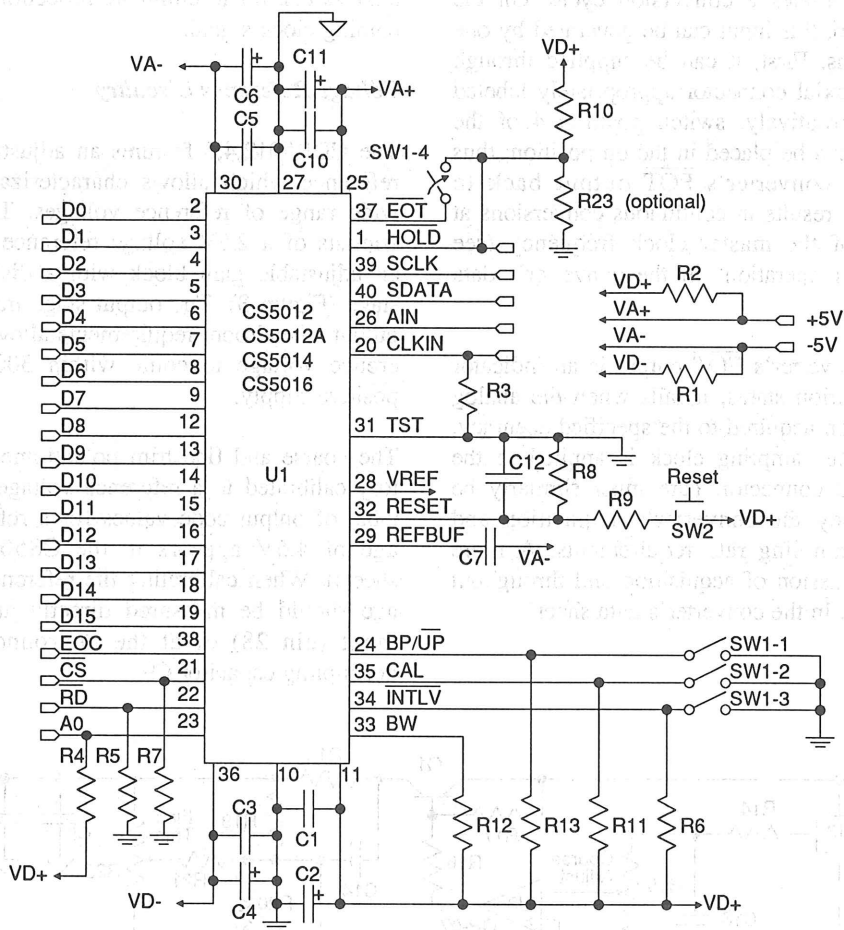


Figure 1. CDB5012,4,6 Schematic  
(Reference Circuitry Appears in Figure 3)

	OFF	ON
Position 1	Bipolar	Unipolar
Position 2	Burst Cal	Normal Operation
Position 3	Normal	Interleaved Cal
Position 4	Normal	Continuous Conversion

**Figure 2. DIP-Switch Definitions**

### Initiating Conversions

A negative transition on the converter's  $\overline{\text{HOLD}}$  pin places the device's analog input into the hold mode and initiates a conversion cycle. On the CDB5012,4,6, this input can be generated by one of two means. First, it can be supplied through the BNC coaxial connector appropriately labeled  $\overline{\text{HOLD}}$ . Alternatively, switch position 4 of the DIP-switch can be placed in the on position, thus looping the converter's  $\overline{\text{EOT}}$  output back to  $\overline{\text{HOLD}}$ . This results in continuous conversions at a fraction of the master clock frequency (see "synchronous operation" in the converter's data sheet).

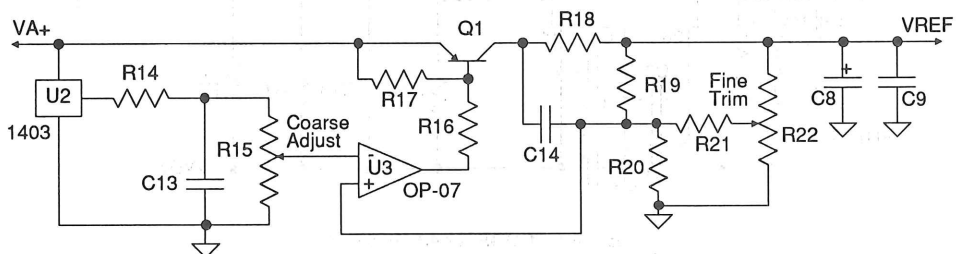
The A/D converter's  $\overline{\text{EOT}}$  output is an indicator of its acquisition status; it falls when the analog input has been acquired to the specified accuracy. If an external sampling clock is applied to the  $\overline{\text{HOLD}}$  BNC connector, care must similarly be taken to obey the converter's acquisition and maximum sampling rate requirements. A more detailed discussion of acquisition and throughput can be found in the converter's data sheet.

The CDB5012,4,6 is shipped from the factory without the  $\overline{\text{HOLD}}$  BNC input terminated for operation with an external sampling clock. However, location R23 is reserved for the insertion of a  $51\ \Omega$  resistor to eliminate reflections of the incoming clock signal.

### Voltage Reference Circuitry

The CDB5012,4,6 features an adjustable voltage reference which allows characterization over a wide range of reference voltages. The circuitry consists of a 2.5V voltage reference (1403) and an adjustable gain block with a discrete output stage (Figure 3). The output stage minimizes the output's headroom requirements allowing the reference voltage to come within 300mV of the positive supply.

The coarse and fine trim potentiometers are factory calibrated to a reference voltage of 4.5V (a table of output code values for a reference voltage of 4.5V appears in the CS5012,4,6 data sheets). When calibrating the reference, the voltage should be measured directly at the VREF input (pin 28) or at the ungrounded lead of decoupling capacitor C9.



**Figure 3. Voltage Reference Circuitry**

### Reset/Self-Calibration Modes

The A/D converter will usually reset itself upon power-up. Since this function is not guaranteed, the converter must be reset upon power-up in system operation. The converter can be reset on the CDB5012,4,6 board by momentarily depressing pushbutton SW-2 thus initiating a full calibration cycle; 1,443,840 master clock cycles later the converter is ready for normal operation.

The converters also feature two other modes of calibration: burst and interleave. Burst calibration can be initiated by moving switch position 2 on the DIP-switch to the off position. In this mode (CAL high), the A/D converter continually loops through calibration cycles until CAL returns low. Interleave can be initiated by setting switch position 3 to the on position. In the interleave mode (INTRLV low), the converter appends one small portion of a calibration cycle (20 master clock cycles) to each conversion cycle. Thus, a full calibration cycle completes every 72,192 conversion cycles.

A more detailed discussion of the converters' calibration modes and capabilities can be found in their data sheets.

### Parallel Output Data/Microprocessor Interface

The converter's outputs D0-D15, its  $\overline{CS}$ ,  $\overline{RD}$ , and A0 inputs, and its  $\overline{EOC}$  output are available at the 40 pin header. The  $\overline{CS}$  and  $\overline{RD}$  inputs are pulled low through 10 k $\Omega$  resistors placing the converter in a microprocessor-independent mode. Control input A0 is pulled up, insuring the converter's output word, rather than the status register, appears at the header.

The converter's 3-state output buffers and microprocessor interface can be exercised by driving the  $\overline{CS}$  and/or  $\overline{RD}$  inputs at the header. Similarly, the converter's 8-bit status register can be obtained on D0-D7 by driving A0 low.

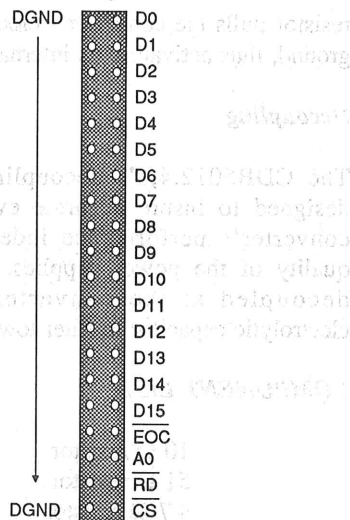


Figure 4. Header Pin Definitions

The converter's  $\overline{EOC}$  and data outputs are not buffered on the CDB5012,4,6. Therefore, careful attention should be paid to the load presented by any cabling, especially if the 3-state output buffers are to be exercised at speed. Twisted ribbon cable is typically specified at 10pF/ft, so several feet can generally be accommodated.

### Serial Output Data

Serial output data is available at the two BNC connections SCLK and SDATA. Data appears MSB first, LSB last, and is valid on the rising edge of SCLK.

### Master Clock

The A/D converter operates from a master clock which can either be internally-generated or externally-supplied. For operation with an external clock, the BNC connector labeled CLKIN should be driven with a TTL clock signal. The CDB5012,4,6 is shipped from the factory with the CLKIN input terminated by a 51  $\Omega$  resistor to eliminate line reflections of the incoming clock. If the CLKIN BNC input is left floating, this

resistor pulls the converter's clock input down to ground, thus activating its internal oscillator.

### Decoupling

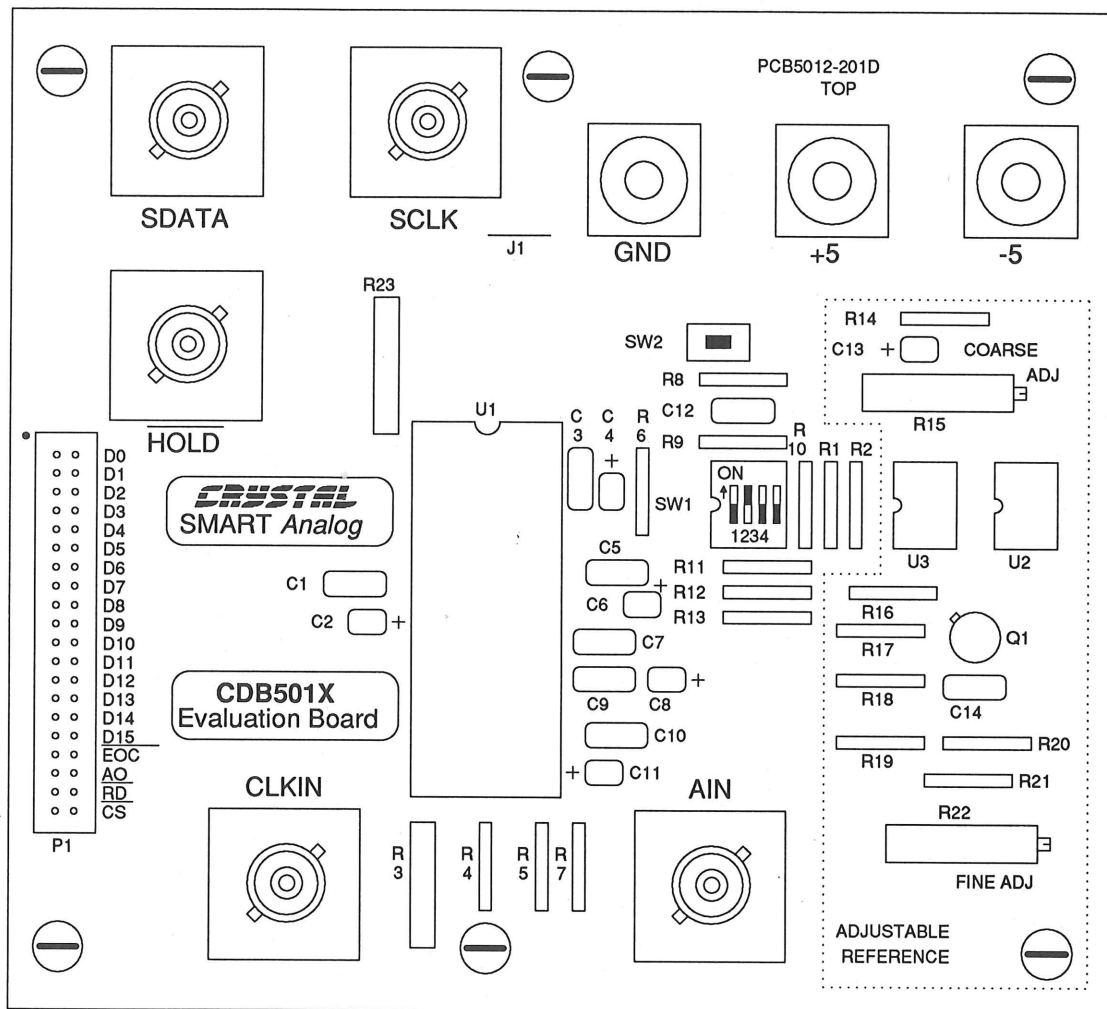
The CDB5012,4,6's decoupling scheme was designed to insure accurate evaluation of the converter's performance independent of the quality of the power supplies. Each supply is decoupled at the converter with a 10 $\mu$ F electrolytic capacitor to filter low frequency noise

and a 0.1 $\mu$ F ceramic capacitor to handle higher frequencies. The auto-zeroing action of the converter's comparator provides extremely good power supply rejection at low frequencies. Depending on the quality of the system's power supplies, the decoupling scheme could be relaxed in actual use.

### COMPONENT LIST

10 $\Omega$ resistor	R1, R2
51 $\Omega$ resistor	R3
4.7 $\Omega$ resistor	R18
1 k $\Omega$ resistor	R9, R14
560 $\Omega$ resistor	R17
10 k $\Omega$ resistor	R4, R5, R6, R7, R8, R10, R11, R12, R13
2.43 k $\Omega$ resistor	R19, R20
3.3 k $\Omega$ resistor	R16
240 k $\Omega$ resistor	R21
50 k $\Omega$ potentiometer	R15
50 k $\Omega$ potentiometer	R22
0.068 $\mu$ F capacitor	C14
0.1 $\mu$ F capacitor	C1, C3, C5, C7, C9, C10, C12
10 $\mu$ F capacitor	C2, C4, C6, C8, C11, C13
CS501X/511X A/D converter	U1
1403 2.5V reference	U2
OP07 op amp	U3
2N2907A transistor	Q1
4 pos. SPST DIP switch	SW1
N.O. SPST pushbutton	SW2
20 pin header	CON1
bulkhead BNC	CON2, CON3, CON4, CON5, CON6
red banana jack	CON7
black banana jack	CON8
green banana jack	CON9
1" 4-40 spacer	POST1, POST2, POST3, POST4, POST5, POST6
3/8" 4-40 screw	SC1, SC2, SC3, SC4, SC5, SC6

\* 2910V \*



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Figure 5. Board Layout

• Notes •





## 12-Bit, 400 kHz, Sampling A/D Converters

### Features

- Monolithic CMOS A/D Converter
  - 0.5 $\mu$ s Track/Hold Amplifier
  - 2 $\mu$ s A/D Converter
  - On-Chip Voltage Reference
  - Flexible Serial Output Port
- True 12-Bit Performance (Includes Reference)
  - Total Unadjusted Error:  $\pm 1/2$  LSB
  - DNL:  $\pm 1/2$  LSB
- Low Distortion
  - Total Harmonic Distortion: -80 dB
  - Peak Harmonic or Noise: -80 dB
- Low Power: 50mW

### General Description

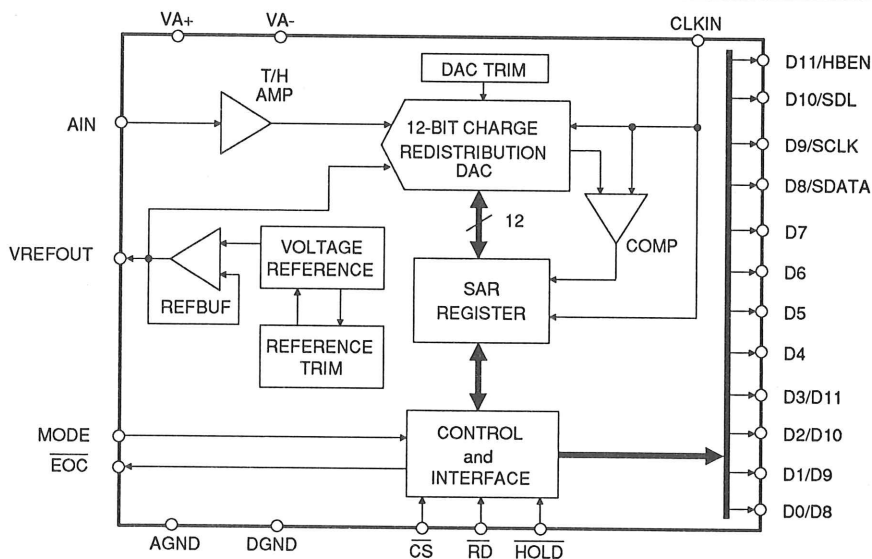
The CS5030, CS5031, and CS5032 are complete monolithic CMOS analog-to-digital converters capable of 400 kHz throughput. On-chip calibration circuitry achieves true 12-bit performance (including reference drift) over the full operating temperature range without external adjustments.

The CS5030/1/2 have a high speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Conversion results are available in either 12-bit parallel, two 8-bit bytes, or serial data.

The CS5030/1/2 are available in a 24-pin, 0.3" plastic dual-in-line package (PDIP), Cerdip and small outline (SOIC) package.

### ORDERING INFORMATION:

Contact Crystal Semiconductor



### Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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APR '92  
DS90PP1  
3-55

• Notes •

## 16-Bit, 100 kHz/20 kHz A/D Converters

### Features

- Monolithic CMOS A/D Converters  
Inherent Sampling Architecture  
2-Channel Input Multiplexer  
Flexible Serial Output Port
- Ultra-Low Distortion  
S/(N+D): 92 dB  
THD: 0.001%
- Conversion Time  
CS5101A: 8  $\mu$ s  
CS5102A: 40  $\mu$ s
- Linearity Error:  $\pm 0.001\%$  FS  
Guaranteed No Missing Codes
- Self-Calibration Maintains Accuracy  
Over Time and Temperature
- Low Power Consumption  
CS5101A: 320 mW  
CS5102A: 44 mW  
Power-down Mode: < 1 mW
- Evaluation Board Available

### General Description

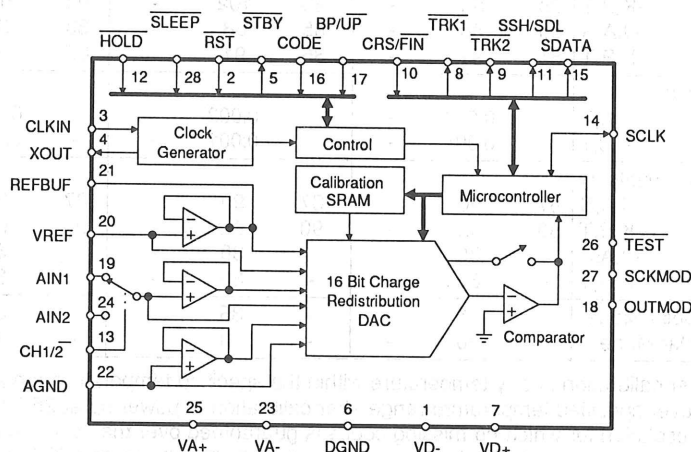
The CS5101A and CS5102A are 16-bit monolithic CMOS analog-to-digital converters capable of 100 kHz (5101A) and 20 kHz (5102A) throughput. The CS5102A's low power consumption of 44 mW, coupled with a power down mode, makes it particularly suitable for battery powered operation.

On-chip self-calibration circuitry achieves nonlinearity of  $\pm 0.001\%$  of FS and guarantees 16-bit no missing codes over the entire specified temperature range. Superior linearity also leads to 92 dB S/(N+D) with harmonics below -100 dB. Offset and full-scale errors are minimized during the calibration cycle, eliminating the need for external trimming.

The CS5101A and CS5102A each consist of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, clock generator, comparator, and serial communications port. The inherent sampling architecture of the device eliminates the need for an external track and hold amplifier.

The converters' 16-bit data is output in serial form with either binary or 2's complement coding. Three output timing modes are available for easy interfacing to microcontrollers and shift registers. Unipolar and bipolar input ranges are digitally selectable.

**ORDERING INFORMATION:** Page 3-93



**ANALOG CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}, V_{D+} = 5V$ ;  $V_{A-}, V_{D-} = -5V$ ;  $V_{REF} = 4.5V$ ; Full-Scale Input Sinewave, 1 kHz; CLKIN = 4 MHz for -16, 8 MHz for -8;  $f_s = 50$  kHz for -16, 100 kHz for -8; Bipolar Mode; FRN Mode; AIN1 and AIN2 tied together, each channel tested separately; Analog Source Impedance = 50  $\Omega$  with 1000 pF to AGND unless otherwise specified)

Parameter*	CS5101A-J,K			CS5101A-A,B			CS5101A-S,T			Units	
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Specified Temperature Range	0 to +70			-40 to +85			-55 to +125			°C	
Accuracy											
Linearity Error (Note 1)	-J,A,S	-	0.002	0.003	-	0.002	0.003	-	0.002	0.004	%FS
	-K,B,T	-	0.001	0.002	-	0.001	0.002	-	0.001	0.003	%FS
	(Note 2) Drift	-	± 1/4	-	-	± 1/4	-	-	± 1/2	-	ΔLSB
Differential Linearity (Note 3, 4)	16	-	-	16	-	-	16	-	-	Bits	
Full Scale Error	(Note 1) -J,A,S	-	± 1	± 4	-	± 1	± 4	-	± 2	± 5	LSB
	-K,B,T	-	± 1	± 3	-	± 1	± 3	-	± 2	± 4	LSB
	(Note 2) Drift	-	± 1	-	-	± 1	-	-	± 2	-	ΔLSB
Unipolar Offset	(Note 1) -J,A,S	-	± 2	± 5	-	± 2	± 5	-	± 2	± 5	LSB
	-K,B,T	-	± 2	± 4	-	± 2	± 4	-	± 2	± 4	LSB
	(Note 2) Drift	-	± 1	-	-	± 1	-	-	± 2	-	ΔLSB
Bipolar Offset	(Note 1) -J,A,S	-	± 2	± 5	-	± 2	± 5	-	± 2	± 5	LSB
	-K,B,T	-	± 2	± 3	-	± 2	± 3	-	± 2	± 3	LSB
	(Note 2) Drift	-	± 1	-	-	± 2	-	-	± 2	-	ΔLSB
Bipolar Negative Full-Scale Error	(Note 1) -J,A,S	-	± 1	± 4	-	± 1	± 4	-	± 1	± 5	LSB
	-K,B,T	-	± 1	± 3	-	± 1	± 3	-	± 1	± 3	LSB
	(Note 2) Drift	-	± 1	-	-	± 1	-	-	± 2	-	ΔLSB
Dynamic Performance (Bipolar Mode)											
Peak Harmonic or Spurious Noise (Note 1)	1 kHz Input	-J,A,S	96	100	-	96	100	-	94	100	dB
		-K,B,T	98	102	-	98	102	-	98	102	dB
	12 kHz Input	-J,A,S	85	88	-	85	88	-	83	88	dB
		-K,B,T	85	91	-	85	91	-	85	91	dB
Total Harmonic Distortion	-J,A,S	-	0.002	-	-	0.002	-	-	0.002	-	%
	-K,B,T	-	0.001	-	-	0.001	-	-	0.001	-	%
Signal-to-Noise Ratio (Note 1)	0dB Input	-J,A,S	87	90	-	87	90	-	87	90	dB
		-K,B,T	90	92	-	90	92	-	90	92	dB
	-60 dB Input	-J,A,S	-	30	-	-	30	-	-	30	dB
		-K,B,T	-	32	-	-	32	-	-	32	dB
Noise (Note 5)	Unipolar Mode	-	35	-	-	35	-	-	35	-	μVrms
	Bipolar Mode	-	70	-	-	70	-	-	70	-	μVrms

- Notes: 1. Applies after calibration at any temperature within the specified temperature range. At temp  
2. Total drift over specified temperature range after calibration at power-up at 25 °C.  
3. Minimum resolution for which no missing codes is guaranteed over the specified temperature range.  
4. Clock speeds of less than 1.0 MHz, at temperatures >100°C will degrade DNL performance.  
5. Wideband noise aliased into the baseband. Referred to the input.

\*Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

### ANALOG CHARACTERISTICS (continued)

Parameter		Symbol	CS5101A -J,K		CS5101A -A,B		CS5101A -S,T		Units
			Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range		-	0 to +70		-40 to +85		-55 to +125		°C
Analog Input									
Aperture Time		-	-	25	-	-	25	-	ns
Aperture Jitter		-	-	100	-	-	100	-	ps
Input Capacitance (Note 6)	Unipolar Mode	-	-	320	425	-	320	425	pF
	Bipolar Mode	-	-	200	265	-	200	265	pF
Conversion & Throughput									
Conversion Time (Note 7)	-8	t <sub>c</sub>	-	-	8.12	-	-	8.12	μs
	-16	t <sub>c</sub>	-	-	16.25	-	-	16.25	μs
Acquisition Time (Note 8)	-8	t <sub>a</sub>	-	-	1.88	-	-	1.88	μs
	-16	t <sub>a</sub>	-	-	2.6 3.75	-	-	2.6 3.75	μs
Throughput (Note 9)	-8	f <sub>tp</sub>	100	-	-	100	-	-	kHz
	-16	f <sub>tp</sub>	50	-	-	50	-	-	kHz
Power Supplies									
Power Supply Current									
(SLEEP High) (Note 10)	Positive Analog	I <sub>A+</sub>	-	21	28	-	21	28	mA
	Negative Analog	I <sub>A-</sub>	-	-21	-28	-	-21	-28	mA
	Positive Digital	I <sub>D+</sub>	-	11	15	-	11	15	mA
	Negative Digital	I <sub>D-</sub>	-	-11	-15	-	-11	-15	mA
Power Consumption (Notes 10, 11)	(SLEEP High)	P <sub>do</sub>	-	320	430	-	320	430	mW
	(SLEEP Low)	P <sub>ds</sub>	-	1	-	-	1	-	mW
Power Supply Rejection:									
(Note 12)	Positive Supplies	PSR	-	84	-	-	84	-	dB
	Negative Supplies	PSR	-	84	-	-	84	-	dB

- Notes:
- Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 30 pF.
  - Conversion time scales directly to the master clock speed. The times shown are for synchronous, internal loopback (FRN mode) with 8.0 MHz CLKIN. In PDT, RBT, and SSC modes, asynchronous delay between the falling edge of HOLD and the start of conversion may add to the apparent conversion time. This delay will not exceed 1.5 master clock cycles + 10 ns. In PDT, RBT, and SSC modes, CLKIN can be increased as long as the HOLD sample rate is 100 kHz max.
  - The CS5101A requires 6 clock cycles of coarse charge, followed by a minimum of 1.125 μs of fine charge. FRN mode allows 9 clock cycles for fine charge which provides for the minimum 1.125 μs with an 8 MHz clock, however; in PDT, RBT, or SSC modes, at clock frequencies of 8 MHz or less, fine charge may be less than 9 clock cycles. This reflects the typ. specification (6 clock cycles + 1.125 μs).
  - Throughput is the sum of the acquisition and conversion times. It will vary in accordance with conditions affecting acquisition and conversion times, as described above.
  - All outputs unloaded. All inputs at VD+ or DGND.
  - Power consumption in the sleep mode applies with no master clock applied (CLKIN held high or low).
  - With 300 mV p-p, 1 kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 23 shows a plot of typical power supply rejection versus frequency.

**SWITCHING CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}, V_{D+} = 5V \pm 10\%$ ;  
 $V_{A-}, V_{D-} = -5V \pm 10\%$ ; Inputs: Logic 0 = 0V, Logic 1 =  $V_{D+}$ ;  $C_L = 50$  pF)

Parameter	Symbol	Min	Typ	Max	Units
CLKIN Period (Note 4)	$t_{clk}$	108	-	10,000	ns
	$t_{clk}$	250	-	10,000	ns
CLKIN Low Time	$t_{clkL}$	37.5	-	-	ns
CLKIN High Time	$t_{clkH}$	37.5	-	-	ns
Crystal Frequency (Note 13)	$f_{xtal}$	2.0	-	9.216	MHz
	$f_{xtal}$	2.0	-	4.0	MHz
SLEEP Rising to Oscillator Stable (Note 14)	-	-	2	-	ms
RST Pulse Width	$t_{rst}$	150	-	-	ns
RST to STBY Falling	$t_{drrs}$	-	100	-	ns
RST Rising to STBY Rising	$t_{cal}$	-	11,528,160	-	clk
CH1/2 Edge to TRK1, TRK2 Rising (Note 15)	$t_{drsh1}$	-	80	-	ns
CH1/2 Edge to TRK1, TRK2 Falling (Note 15)	$t_{dfsh4}$	-	-	68 $t_{clk}+260$	ns
HOLD to SSH Falling (Note 16)	$t_{dfsh2}$	-	60	-	ns
HOLD to TRK1, TRK2, Falling (Note 16)	$t_{dfsh1}$	66 $t_{clk}$	-	68 $t_{clk}+260$	ns
HOLD to TRK1, TRK2, SSH Rising (Note 16)	$t_{drsh}$	-	120	-	ns
HOLD Pulse Width (Note 17)	$t_{hold}$	1 $t_{clk}+20$	-	63 $t_{clk}$	ns
HOLD to CH1/2 Edge (Note 16)	$t_{dhlri}$	15	-	64 $t_{clk}$	ns
HOLD Falling to CLKIN Falling (Note 17)	$t_{hcf}$	95	-	1 $t_{clk}+10$	ns

- Note: 13. External loading capacitors are required to allow the crystal to oscillate. Maximum crystal frequency is 8.0 MHz in FRN mode (100 kHz sample rate).  
 14. With a 8 MHz crystal, two 10 pF loading capacitors and a 10 M $\Omega$  parallel resistor (see Figure 8).  
 15. These times are for FRN mode.  
 16. SSH only works correctly if  $\overline{HOLD}$  falling edge is within +15 to +30 ns of CH1/2 edge or if CH1/2 edge occurs after  $\overline{HOLD}$  rises to 64  $t_{clk}$  after  $\overline{HOLD}$  has fallen. These times are for SSC, PDT and RBT modes.  
 17. When  $\overline{HOLD}$  goes low, the analog sample is captured immediately. To start conversion,  $\overline{HOLD}$  must be latched by a falling edge of CLKIN. Conversion will begin on the next rising edge of CLKIN after  $\overline{HOLD}$  is latched. If  $\overline{HOLD}$  is operated synchronous to CLKIN, the  $\overline{HOLD}$  pulse width may be as narrow as 150 ns for all CLKIN frequencies if CLKIN falls 95 ns after  $\overline{HOLD}$  falls. This ensures that the  $\overline{HOLD}$  pulse will meet the minimum specification for  $t_{hcf}$ .

**ANALOG CHARACTERISTICS** (TA = TMIN to TMAX; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; Full-Scale Input Sinewave, 200 Hz; CLKIN = 1.6 MHz; fs = 20 kHz; Bipolar Mode; FRN Mode; AIN1 and AIN2 tied together, each channel tested separately; Analog Source Impedance = 50 Ω with 1000pF to AGND unless otherwise specified)

Parameter*		CS5102A -J,K			CS5102A -A,B			CS5102A -S,T			Units	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125			°C	
Accuracy												
Linearity Error	(Note 1)	-J,A,S	-	0.002	0.003	-	0.002	0.003	-	0.002	0.004	%FS
		-K,B,T	-	0.001	0.0015	-	0.001	0.0015	-	0.001	0.002	%FS
	(Note 2)	Drift	-	±1/4	-	-	±1/4	-	-	±1/2	-	ΔLSB
Differential Linearity (Note 3, 18)			16	-	-	16	-	-	16	-	-	Bits
Full Scale Error	(Note 1)	-J,A,S	-	±2	±4	-	±2	±4	-	±2	±5	LSB
		-K,B,T	-	±2	±3	-	±2	±3	-	±2	±3	LSB
	(Note 2)	Drift	-	±1	-	-	±1	-	-	±2	-	ΔLSB
Unipolar Offset	(Note 1)	-J,A,S	-	±1	±4	-	±1	±4	-	±1	±5	LSB
		-K,B,T	-	±1	±3	-	±1	±3	-	±1	±3	LSB
	(Note 2)	Drift	-	±1	-	-	±1	-	-	±2	-	ΔLSB
Bipolar Offset	(Note 1)	-J,A,S	-	±1	±4	-	±1	±4	-	±1	±5	LSB
		-K,B,T	-	±1	±3	-	±1	±3	-	±1	±3	LSB
	(Note 2)	Drift	-	±1	-	-	±2	-	-	±2	-	ΔLSB
Bipolar Negative Full-Scale Error	(Note 1)	-J,A,S	-	±2	±4	-	±2	±4	-	±2	±5	LSB
		-K,B,T	-	±2	±3	-	±2	±3	-	±2	±3	LSB
	(Note 2)	Drift	-	±1	-	-	±2	-	-	±2	-	ΔLSB
Dynamic Performance (Bipolar Mode)												
Peak Harmonic or Spurious Noise (Note 1)	-J,A,S	96	100	-	96	100	-	94	100	-	dB	
	-K,B,T	98	102	-	98	102	-	98	102	-	dB	
Total Harmonic Distortion	-J,A,S	-	0.002	-	-	0.002	-	-	0.002	-	%	
	-K,B,T	-	0.001	-	-	0.001	-	-	0.001	-	%	
Signal-to-Noise Ratio	(Note 1)											
	0 dB Input	-J,A,S	87	90	-	87	90	-	87	90	-	dB
		-K,B,T	90	92	-	90	92	-	90	92	-	dB
	-60 dB Input	-J,A,S	-	30	-	-	30	-	-	30	-	dB
		-K,B,T	-	32	-	-	32	-	-	32	-	dB
Noise (Note 5)	Unipolar Mode	-	35	-	-	35	-	-	35	-	μVrms	
	Bipolar Mode	-	70	-	-	70	-	-	70	-	μVrms	

Notes: 18. Clock speeds of less than 1.6 MHz, at temperatures >100°C will degrade DNL performance.

\*Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.



**ANALOG CHARACTERISTICS** (continued)

Parameter		Symbol	CS5102A -J,K Min Typ Max			CS5102A -A,B Min Typ Max			CS5102A -S,T Min Typ Max			Units
Specified Temperature Range		-	0 to +70			-40 to +85			-55 to +125			°C
Analog Input												
Aperture Time		-	-	30	-	-	30	-	-	30	-	ns
Aperture Jitter		-	-	100	-	-	100	-	-	100	-	ps
Input Capacitance (Note 6)	Unipolar Mode	-	-	320	425	-	320	425	-	320	425	pF
	Bipolar Mode	-	-	200	265	-	200	265	-	200	265	pF
Conversion & Throughput												
Conversion Time (Note 19)		t <sub>c</sub>	-	-	40.625	-	-	40.625	-	-	40.625	μs
Acquisition Time (Note 20)		t <sub>a</sub>	-	-	9.375	-	-	9.375	-	-	9.375	μs
Throughput (Note 21)		f <sub>tp</sub>	20	-	-	20	-	-	20	-	-	kHz
Power Supplies												
Power Supply Current												
(SLEEP High) (Note 22)	Positive Analog	I <sub>A+</sub>	-	2.4	3.5	-	2.4	3.5	-	2.4	3.5	mA
	Negative Analog	I <sub>A-</sub>	-	-2.4	-3.5	-	-2.4	-3.5	-	-2.4	-3.5	mA
	Positive Digital	I <sub>D+</sub>	-	2.5	3.5	-	2.5	3.5	-	2.5	3.5	mA
	Negative Digital	I <sub>D-</sub>	-	-1.5	-2.5	-	-1.5	-2.5	-	-1.5	-2.5	mA
Power Consumption (Notes 11, 22)	(SLEEP High)	P <sub>do</sub>	-	44	65	-	44	65	-	44	65	mW
	(SLEEP Low)	P <sub>ds</sub>	-	1	-	-	1	-	-	1	-	mW
Power Supply Rejection (Note 23)												
	Positive Supplies	PSR	-	84	-	-	84	-	-	84	-	dB
	Negative Supplies	PSR	-	84	-	-	84	-	-	84	-	dB

- Notes: 19. Conversion time scales directly to the master clock speed. The times shown are for synchronous, internal loopback (FRN mode). In PDT, RBT, and SSC modes, asynchronous delay between the falling edge of HOLD and the start of conversion may add to the apparent conversion time. This delay will not exceed 1 master clock cycle + 140 ns.
20. The CS5102A requires 6 clock cycles of coarse charge, followed by a minimum of 5.625 μs of fine charge. FRN mode allows 9 clock cycles for fine charge which provides for the minimum 5.625 μs with an 1.6 MHz clock, however; in PDT, RBT, or SSC modes, at clock frequencies less than 1.6 MHz, fine charge may be less than 9 clock cycles.
21. Throughput is the sum of the acquisition and conversion times. It will vary in accordance with conditions affecting acquisition and conversion times, as described above.
22. All outputs unloaded. All inputs at VD+ or DGND. See table below for power dissipation vs. clock frequency
23. With 300 mV p-p, 1 kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 23 shows a plot of typical power supply rejection versus frequency.

Typ. Power (mW)	CLKIN (MHz)
34	0.8
37	1.0
39	1.2
41	1.4
44	1.6

### SWITCHING CHARACTERISTICS ( $T_A = T_{MIN}$ to $T_{MAX}$ ;

$V_{A+}, V_{D+} = 5V \pm 10\%$ ;  $V_{A-}, V_{D-} = -5V \pm 10\%$ ; Inputs: Logic 0 = 0V, Logic 1 =  $V_{D+}$ ;  $C_L = 50$  pF)

Parameter	Symbol	Min	Typ	Max	Units
CLKIN Period (Note 18, 24)	$t_{clk}$	0.5	-	10	$\mu s$
CLKIN Low Time	$t_{clkL}$	200	-	-	ns
CLKIN High Time	$t_{clkH}$	200	-	-	ns
Crystal Frequency (Note 24, 25)	$f_{xtal}$	TBD	1.6	2.0	MHz
SLEEP Rising to Oscillator Stable (Note 26)	-	-	20	-	ms
RST Pulse Width	$t_{rst}$	150	-	-	ns
RST to STBY Falling	$t_{drss}$	-	100	-	ns
RST Rising to STBY Rising	$t_{cal}$	-	2,882,040	-	tclk
CH1/2 Edge to TRK1, TRK2 Rising (Note 27)	$t_{drsh1}$	-	80	-	ns
CH1/2 Edge to TRK1, TRK2 Falling (Note 27)	$t_{dfsh4}$	-	-	$68t_{clk}+260$	ns
HOLD to SSH Falling (Note 28)	$t_{dfsh2}$	-	60	-	ns
HOLD to TRK1, TRK2, Falling (Note 28)	$t_{dfsh1}$	$66t_{clk}$	-	$68t_{clk}+260$	ns
HOLD to TRK1, TRK2, SSH Rising (Note 28)	$t_{drsh}$	-	120	-	ns
HOLD Pulse Width (Note 29)	$t_{hold}$	$1t_{clk}+20$	-	$63t_{clk}$	ns
HOLD to CH1/2 Edge (Note 28)	$t_{dhlri}$	15	-	$64t_{clk}$	ns
HOLD Falling to CLKIN Falling (Note 29)	$t_{hcf}$	55	-	$1t_{clk}+10$	ns

Note: 24. Minimum CLKIN period is 0.625  $\mu s$  in FRN mode (20 kHz sample rate). At temperatures  $>+85^\circ C$ , and with clock frequencies  $>1.6$  MHz, analog performance may be degraded.

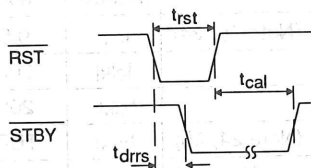
25. External loading capacitors are required to allow the crystal to oscillate. Maximum crystal frequency is 1.6 MHz in FRN mode (20 kHz sample rate).

26. With a 2.0 MHz crystal, two 33 pF loading capacitors and a 10 M $\Omega$  parallel resistor (see Figure 8).

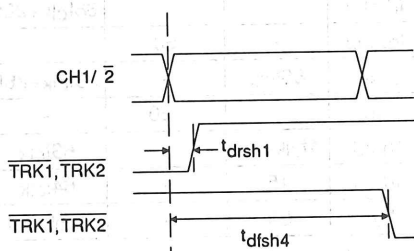
27. These times are for FRN mode.

28. SSH only works correctly if  $\overline{HOLD}$  falling edge is within +15 to +30 ns of CH1/2 edge or if CH1/2 edge occurs after  $\overline{HOLD}$  rises to 64  $t_{clk}$  after  $\overline{HOLD}$  has fallen. These times are for SSC, PDT and RBT modes.

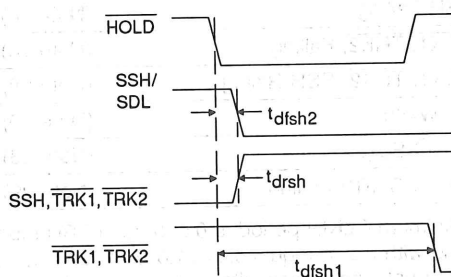
29. When  $\overline{HOLD}$  goes low, the analog sample is captured immediately. To start conversion,  $\overline{HOLD}$  must be latched by a falling edge of CLKIN. Conversion will begin on the next rising edge of CLKIN after  $\overline{HOLD}$  is latched. If  $\overline{HOLD}$  is operated synchronous to CLKIN, the  $\overline{HOLD}$  pulse width may be as narrow as 150 ns for all CLKIN frequencies if CLKIN falls 55 ns after  $\overline{HOLD}$  falls. This ensures that the  $\overline{HOLD}$  pulse will meet the minimum specification for  $t_{hcf}$ .



**Reset and Calibration Timing**

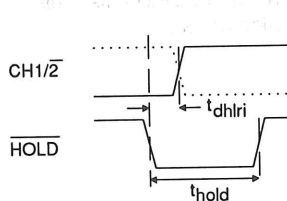


**a. FRN Mode**

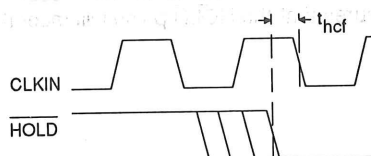


**b. PDT, RBT Mode**

**Control Output Timing**



**Channel Selection Timing**



**Start Conversion Timing**

**SWITCHING CHARACTERISTICS** (Continued)

Parameter	Symbol	Min	Typ	Max	Units
<b>PDT and RBT Modes</b>					
SCLK Input Pulse Period	t <sub>sclk</sub>	200	-	-	ns
SCLK Input Pulse Width Low	t <sub>sclkL</sub>	50	-	-	ns
SCLK Input Pulse Width High	t <sub>sclkH</sub>	50	-	-	ns
SCLK Input Falling to SDATA Valid	t <sub>dss</sub>	-	100	150	ns
HOLD Falling to SDATA Valid	t <sub>dhs</sub>	-	140	230	ns
TRK1, TRK2 Falling to SDATA Valid	t <sub>dts</sub>	-	65	125	ns
<b>FRN and SSC Modes</b>					
SCLK Output Pulse Width Low	t <sub>slkL</sub>	-	2t <sub>clk</sub>	-	t <sub>clk</sub>
SCLK Output Pulse Width High	t <sub>slkH</sub>	-	2t <sub>clk</sub>	-	t <sub>clk</sub>
SDATA Valid Before Rising SCLK	t <sub>ss</sub>	2t <sub>clk</sub> -100	-	-	ns
SDATA Valid After Rising SCLK	t <sub>sh</sub>	2t <sub>clk</sub> -100	-	-	ns
SDL Falling to 1st Rising SCLK	t <sub>rsclk</sub>	-	2t <sub>clk</sub>	-	ns
Last Rising SCLK to SDL Rising	t <sub>rsdl</sub>	-	2t <sub>clk</sub>	2t <sub>clk</sub> +165	ns
	t <sub>rsdl</sub>	-	2t <sub>clk</sub>	2t <sub>clk</sub> +200	ns
HOLD Falling to 1st Falling SCLK	t <sub>hfs</sub>	6t <sub>clk</sub>	-	8t <sub>clk</sub> +165	ns
	t <sub>hfs</sub>	6t <sub>clk</sub>	-	8t <sub>clk</sub> +200	ns
CH1/2 Edge to 1st Falling SCLK	t <sub>chfs</sub>	-	7t <sub>clk</sub>	-	t <sub>clk</sub>

Note: 30. Only valid for TRK1, TRK2 falling when SCLK is low. If SCLK is high when TRK1, TRK2 falls, then SDATA is valid t<sub>dss</sub> time after the next falling SCLK.

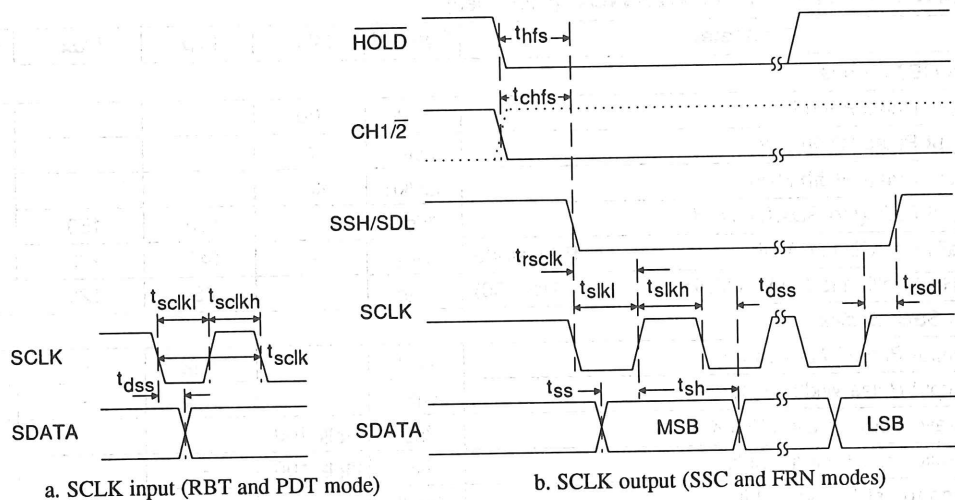
**DIGITAL CHARACTERISTICS** (T<sub>A</sub> = T<sub>min</sub> to T<sub>max</sub>; V<sub>A+</sub>, V<sub>D+</sub> = 5V ± 10%; V<sub>A-</sub>, V<sub>D-</sub> = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention Power Supply Voltage V <sub>A+</sub> and V <sub>D+</sub>	V <sub>MR</sub>	2.0	-	-	V
High-Level Input Voltage	V <sub>IH</sub>	2.0	-	-	V
Low-Level Input Voltage	V <sub>IL</sub>	-	-	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	(V <sub>D+</sub> )-1.0	-	-	V
Low-Level Output Voltage	V <sub>OL</sub>	-	-	0.4	V
Input Leakage Current	I <sub>in</sub>	-	-	10	μA
Digital Output Pin Capacitance	C <sub>out</sub>	-	9	-	pF

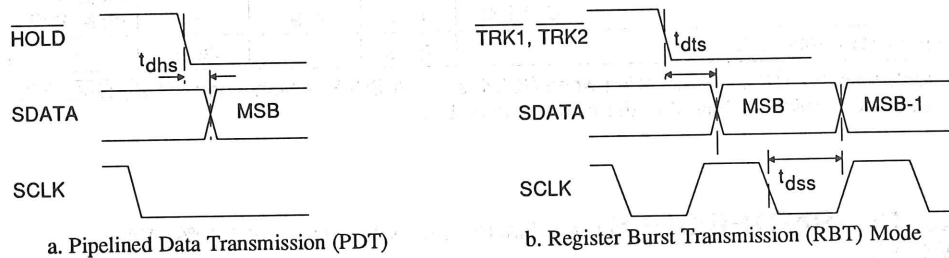
Note: 31. V<sub>A-</sub> and V<sub>D-</sub> can be any value from zero to -5V for memory retention. Neither V<sub>A-</sub> or V<sub>D-</sub> should be allowed to go positive. AIN1, AIN2 or VREF must not be greater than V<sub>A+</sub> or V<sub>D+</sub>.

This parameter is guaranteed by characterization.

32. I<sub>OUT</sub> = -100 μA. This specification guarantees TTL compatibility (V<sub>OH</sub> = 2.4V @ I<sub>OUT</sub> = -40 μA).



### Serial Data Timing



### Data Transmission Timing

### RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 33)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:					
Positive Digital	VD+	4.5	5.0	VA+	V
Negative Digital	VD-	-4.5	-5.0	-5.5	V
Positive Analog	VA+	4.5	5.0	5.5	V
Negative Analog	VA-	-4.5	-5.0	-5.5	V
Analog Reference Voltage	VREF	2.5	4.5	(VA+)-0.5	V
Analog Input Voltage:					
(Note 34) Unipolar	VAIN	AGND	-	VREF	V
Bipolar	VAIN	-VREF	-	VREF	V

Notes: 33. All voltages with respect to ground.

34. The CS5101A and CS5102A can accept input voltages up to the analog supplies (VA+ and VA-). They will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode, with binary coding (CODE = low).

3

### ABSOLUTE MAXIMUM RATINGS\* (AGND, DGND = 0V, all voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:					
Positive Digital (Note 35)	VD+	-0.3	-	6.0	V
Negative Digital	VD-	0.3	-	-6.0	V
Positive Analog	VA+	-0.3	-	6.0	V
Negative Analog	VA-	0.3	-	-6.0	V
Input Current, Any Pin Except Supplies (Note 36)	I <sub>in</sub>	-	-	±10	mA
Analog Input Voltage (AIN and VREF pins)	V <sub>INA</sub>	(VA-)-0.3	-	(VA+)+0.3	V
Digital Input Voltage	V <sub>IND</sub>	-0.3	-	(VA+)+0.3	V
Ambient Operating Temperature	T <sub>A</sub>	-55	-	125	°C
Storage Temperature	T <sub>stg</sub>	-65	-	150	°C

Note: 35. In addition, VD+ must not be greater than (VA+) +0.3V

36. Transient currents of up to 100 mA will not cause SCR latch-up.

\*WARNING: Operation beyond these limits may result in permanent damage to the device.

## GENERAL DESCRIPTION

The CS5101A and CS5102A are 2-channel, 16-bit A/D converters. The devices include an inherent sample/hold and an on-chip analog switch for 2-channel operation. Both channels can thus be sampled and converted at rates up to 50 kHz each (CS5101A) or 10 kHz each (CS5102A). Alternatively, each of the devices can be operated as a single channel ADC operating at 100 kHz (CS5101A) or 20 kHz (CS5102A).

Both the CS5101A and CS5102A can be configured to accept either unipolar or bipolar input ranges, and data is output serially in either binary or 2's complement coding. The devices can be configured in 3 different output modes, as well as an internal, synchronous loopback mode. The CS5101A and CS5102A provide coarse charge/fine charge control, to allow accurate tracking of high-slew signals.

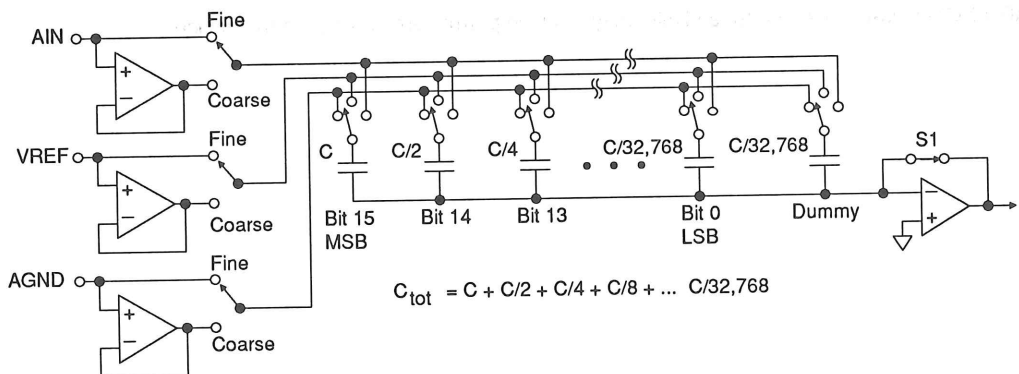
## THEORY OF OPERATION

The CS5101A and CS5102A implement the successive approximation algorithm using a charge redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the

array share a common node at the comparator's input. As shown in Figure 1, their other terminals are capable of being connected to AGND, VREF, or AIN (1 or 2). When the device is not calibrating or converting, all capacitors are tied to AIN. Switch S1 is closed and the charge on the array, tracks the input signal.

When the conversion command is issued, switch S1 opens. This traps the charge on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, which when connected to the reference will drive the voltage at the floating node to zero. That binary fraction of capacitance represents the converter's digital output.



**Figure 1. Coarse Charge Input Buffers and Charge Redistribution DAC**



### Calibration

The ability of the CS5101A or the CS5102A to convert accurately to 16-bits clearly depends on the accuracy of its comparator and DAC. Each device utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 16-bit accuracy from the DAC, the CS5101A and CS5102A use a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors in parallel which can be manipulated to adjust the overall bit weight. An on-chip microcontroller precisely adjusts each capacitor with a resolution of 18 bits.

The CS5101A and CS5102A should be reset upon power-up, thus initiating a calibration cycle. The device then stores its calibration coefficients in on-chip SRAM. When the CS5101A and CS5102A are in power-down mode (SLEEP low), they retain the calibration coefficients in memory, and need not be recalibrated when normal operation is resumed.

### OPERATION OVERVIEW

Monolithic design and inherent sampling architecture make the CS5101A and CS5102A extremely easy to use.

#### Initiating Conversions

A falling transition on the  $\overline{\text{HOLD}}$  pin places the input in the hold mode and initiates a conversion cycle. The charge is trapped on the capacitor array the instant  $\overline{\text{HOLD}}$  goes low. The device will complete conversion of the sample within 66 master clock cycles, then automatically return to

the track mode. After allowing a short time for acquisition, the device will be ready for another conversion.

In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the  $\overline{\text{HOLD}}$  input. The duty cycle of this clock is not critical. The  $\overline{\text{HOLD}}$  input is latched internally by the master clock, so it need only remain low for  $1/f_{\text{clk}} + 20 \text{ ns}$ , but no longer than the minimum conversion time minus two master clocks or an additional conversion cycle will be initiated with inadequate time for acquisition. In Free Run mode,  $\text{SCKMOD} = \text{OUTMOD} = 0$ , the device will convert at a rate of  $\text{CLKIN}/80$ , and the  $\overline{\text{HOLD}}$  input is ignored.

As with any high-resolution A-to-D system, it is recommended that sampling is synchronized to the master system clock in order to minimize the effects of clock feedthrough. However, the CS5101A and CS5102A may be operated entirely asynchronous to the master clock if necessary.

#### Tracking the Input

Upon completing a conversion cycle the CS5101A and CS5102A immediately return to the track mode. The  $\text{CH1}/\overline{2}$  pin directly controls the input switch, and therefore directly determines which channel will be tracked. Ideally, the  $\text{CH1}/\overline{2}$  pin should be switched during the conversion cycle, thereby nullifying the input mux switching time, and guaranteeing a stable input at the start of acquisition. If, however, the  $\text{CH1}/\overline{2}$  control is changed during the acquisition phase, adequate coarse charge and fine charge time must be allowed before initiating conversion.

When the CS5101A or the CS5102A enters tracking mode, it uses an internal input buffer amplifier to provide the bulk of the charge on the capacitor array (coarse-charge), thereby reducing the current load on the external analog circuitry. Coarse-charge is internally initiated for 6 clock cycles at the end of every conversion. The buffer

amplifier is then bypassed, and the capacitor array is directly connected to the input. This is referred to as fine-charge, during which the charge on the array is allowed to accurately settle to the input voltage (see Figure 10).

With a full scale input step, the coarse-charge input buffer of the CS5101A will charge the capacitor array within 1% in 650 ns. The converter timing allows 6 clock cycles for coarse charge settling time. When the CS5101A switches to fine-charge mode, its slew rate is somewhat reduced. In fine-charge, the CS5101A can slew at 2 V/ $\mu$ s in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input, so the CS5101A can slew at 4V/ $\mu$ s.

With a full scale input step, the coarse-charge input buffer of the CS5102A will charge the capacitor array within 1% in 3.75  $\mu$ s. The converter timing allows 6 clock cycles for coarse charge settling time. When in fine-charge mode, the CS5102A can slew at 0.4 V/ $\mu$ s in unipolar mode; and at 0.8 V/ $\mu$ s in bipolar mode.

Acquisition of fast slewing signals can be hastened if the voltage change occurs during or immediately following the conversion cycle. For instance, in multiple channel applications (using either the device's internal channel selector or an external MUX), channel selection should occur while the CS5101A or the CS5102A is converting. Multiplexer switching and settling time is thereby removed from the overall throughput equation.

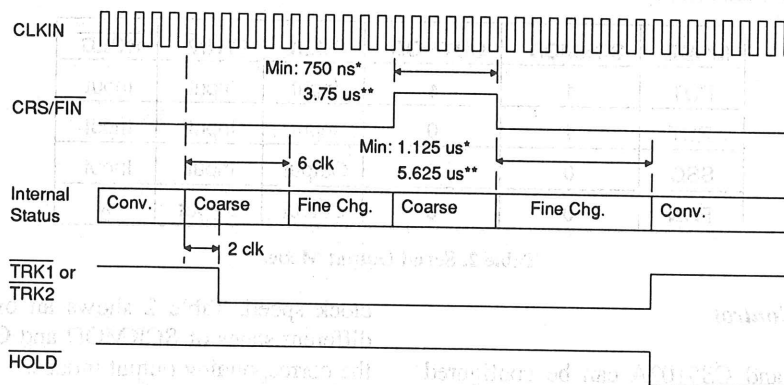
If the input signal changes drastically during the acquisition period (such as changing the signal source), the device should be in coarse-charge for an adequate period following the change. The CS5101A and CS5102A can be forced into coarse-charge by bringing CRS/ $\overline{\text{FIN}}$  high. The buffer amplifier is engaged when CRS/ $\overline{\text{FIN}}$  is high, and may be switched in any number of times during tracking. If CRS/ $\overline{\text{FIN}}$  is held low,

the CS5101A and CS5102A will only coarse-charge for the first 6 clock cycles following a conversion, and will stay in fine-charge until  $\overline{\text{HOLD}}$  goes low. To get an accurate sample using the CS5101A, at least 750 ns of coarse-charge, followed by 1.125  $\mu$ s of fine-charge is required before initiating a conversion. If coarse charge is not invoked, then up to 25  $\mu$ s should be allowed after a step change input for proper acquisition. To get an accurate sample using the CS5102A, at least 3.75  $\mu$ s of coarse-charge, followed by 5.625  $\mu$ s of fine-charge is required before initiating a conversion (see Figure 2). If coarse charge is not invoked, then up to 125  $\mu$ s should be allowed after a step change input for proper acquisition. The CRS/ $\overline{\text{FIN}}$  pin must be low prior to  $\overline{\text{HOLD}}$  becoming active and be held low during conversion.

### **Master Clock**

The CS5101A and CS5102A can operate either from an externally-supplied master clock, or from their own crystal oscillator (with a crystal). To enable the internal crystal oscillator, simply tie a crystal across the XOUT and CLKIN pins and add 2 capacitors and a resistor, as shown on the system connection diagram in Figure 8.

Calibration and conversion times directly scale to the master clock frequency. The CS5101A-8 can operate with clock or crystal frequencies up to 9.216 MHz (8.0 MHz in FRN mode). This allows maximum throughput of up to 50 kHz per channel in dual-channel operation, or 100 kHz in a single channel configuration. The CS5101A-16 can accept a maximum clock speed of 4 MHz, with corresponding throughput of 50 kHz. The CS5102A can operate with clock or crystal frequencies up to 2.0 MHz (1.6 MHz in FRN mode). This allows maximum throughput of up to 10 kHz per channel in dual-channel operation, or 20 kHz in a single channel configuration. For 16 bit performance a 1.6 MHz clock is recommended. This 1.6 MHz clock yields a maximum



\* Applies to 5101A

\*\* Applies to 5102A

Figure 2. Coarse-Charge/Fine-Charge Control

throughput of 20 kHz in a single channel configuration.

### Asynchronous Sampling Considerations

When  $\overline{\text{HOLD}}$  goes low, the analog sample is captured immediately. The  $\overline{\text{HOLD}}$  signal is latched by the next falling edge of CLKIN, and conversion then starts on the subsequent rising edge. If  $\overline{\text{HOLD}}$  is asynchronous to CLKIN, then there will be a 1.5 CLKIN cycle uncertainty as to when conversion starts. Considering the CS5101A with an 8 MHz CLKIN, with a 100 kHz  $\overline{\text{HOLD}}$  signal, then this 1.5 CLKIN uncertainty will result in a 1.5 CLKIN period possible reduction in fine charge time for the next conversion.

This reduced fine charge time will be less than the minimum specification. If the CLKIN frequency is increased slightly (for example, to 8.192 MHz) then sufficient fine charge time will always occur. The maximum frequency for CLKIN is specified at 9.216 MHz; it is recommended that for asynchronous operation at 100 kHz, CLKIN should be between 8.192 MHz and 9.216 MHz.

### Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/ $\overline{\text{UP}}$  low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. In the bipolar configuration (BP/ $\overline{\text{UP}}$  high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF.

Unipolar Input Voltage	Offset Binary	Two's Complement	Bipolar Input Voltage
$>(\text{VREF}-1.5 \text{ LSB})$	FFFF	7FFF	$>(\text{VREF}-1.5 \text{ LSB})$
VREF-1.5 LSB	FFFF ----- FFFE	7FFF ----- 7FFE	VREF-1.5 LSB
VREF/2-0.5 LSB	8000 ----- 7FFF	0000 ----- FFFF	-0.5 LSB
+0.5 LSB	0001 ----- 0000	8001 ----- 8000	-VREF+0.5 LSB
$<(+0.5 \text{ LSB})$	0000	8000	$<(-\text{VREF}+0.5 \text{ LSB})$

Table 1. Output Coding

The CS5101A and CS5102A can output data in either 2's complement, or binary format. If the CODE pin is high, the output is in 2's complement format with a range of -32,768 to +32,767. If the CODE pin is low, the output is in binary format with a range of 0 to +65,535. See table 1 for output coding.

MODE	SCKMOD	OUTMOD	SCLK	CH1/2	HOLD
PDT	1	1	Input	Input	Input
RBT	1	0	Input	Input	Input
SSC	0	1	Output	Input	Input
FRN	0	0	Output	Output	X

**Table 2. Serial Output Modes**

### Output Mode Control

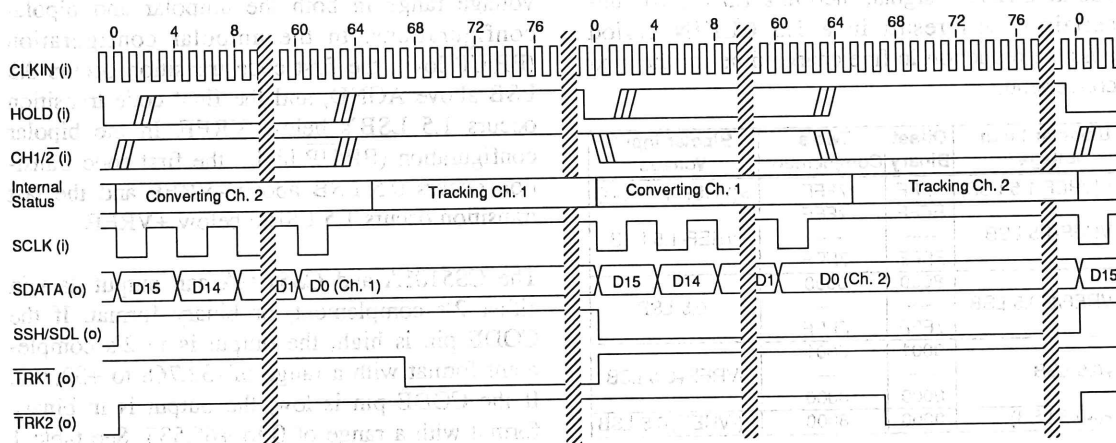
The CS5101A and CS5102A can be configured in three different output modes, as well as an internal, synchronous loop-back mode. This allows great flexibility for design into a wide variety of systems. The operating mode is selected by setting the states of the SCKMOD and OUTMOD pins. In all modes, data is output on SDATA, starting with the MSB. Each subsequent data bit is updated on the falling edge of SCLK.

When SCKMOD is high, SCLK is an input, allowing the data to be clocked out with an external serial clock at rates up to 5 MHz. Additional clock edges after #16 will clock out logic '1's on SDATA. Tying SCKMOD low reconfigures SCLK as an output, and the converter clocks out each bit as it's determined during the conversion process, at a rate of 1/4 the master

clock speed. Table 2 shows an overview of the different states of SCKMOD and OUTMOD, and the corresponding output modes.

### Pipelined Data Transmission (PDT)

PDT mode is selected by tying both SCKMOD and OUTMOD high. In PDT mode, the SCLK pin is an input. Data is registered during conversion cycle, and output during the following conversion cycle. HOLD must be brought low, initiating another conversion, before data from the previous conversion is available on SDATA. If all the data has not been clocked out before the next falling edge of  $\overline{\text{HOLD}}$ , the old data will be lost (Figure 3).



**Figure 3. Pipelined Data Transmission Mode (PDT)**

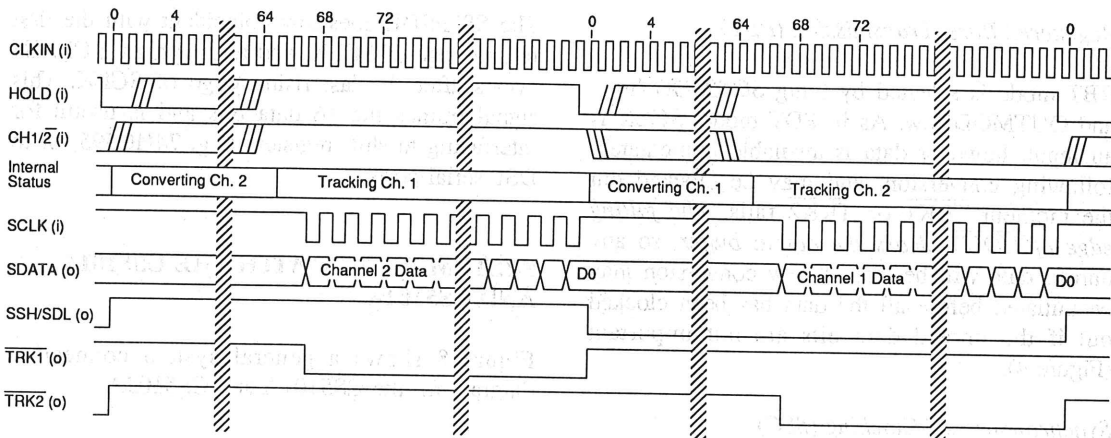


Figure 4. Registered Burst Transmission Mode (RBT)

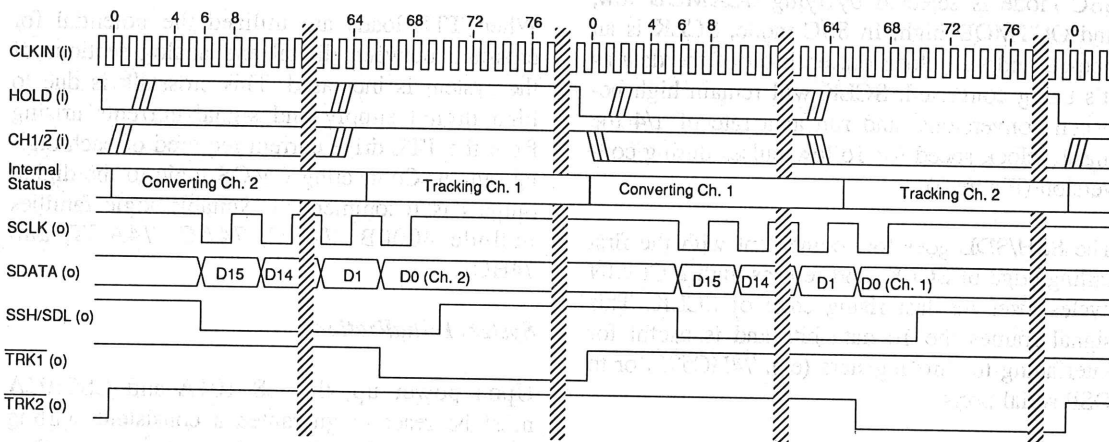


Figure 5. Synchronous Self-Clocking Mode (SSC)

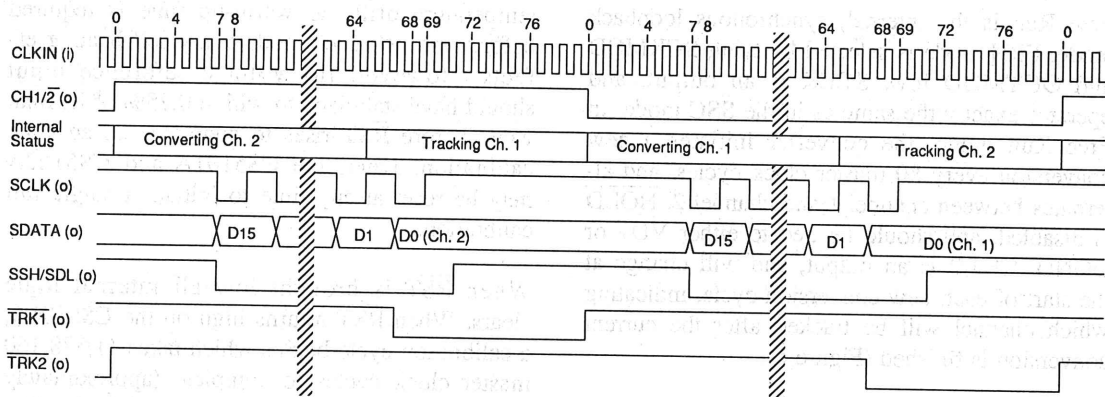


Figure 6. Free Run Mode (FRN)

### Registered Burst Transmission (RBT)

RBT mode is selected by tying SCKMOD high, and OUTMOD low. As in PDT mode, SCLK is an input, however data is available immediately following conversion, and may be clocked out the moment TRK1 or TRK2 falls. *The falling edge of HOLD clears the output buffer*, so any unread data will be lost. A new conversion may be initiated before all the data has been clocked out if the unread data bits are not important (Figure 4).

### Synchronous Self-Clocking (SSC)

SSC mode is selected by tying SCKMOD low, and OUTMOD high. In SSC mode, SCLK is an output, and will clock out each bit of the data as it's being converted. SCLK will remain high between conversions, and run at a rate of 1/4 the master clock speed for 16 low pulses during conversion (Figure 5).

The SSH/SDL goes low coincident with the first falling edge of SCLK, and returns high 2 CLKIN cycles after the last rising edge of SCLK. This signal frames the 16 data bits and is useful for interfacing to shift registers (e.g. 74HC595) or to DSP serial ports.

### Free Run (FRN)

Free Run is the internal, synchronous loopback mode. FRN mode is selected by tying SCKMOD and OUTMOD low. SCLK is an output, and operates exactly the same as in the SSC mode. In Free Run mode, the converter initiates a new conversion every 80 master clock cycles, and alternates between channel 1 and channel 2.  $\overline{\text{HOLD}}$  is disabled, and should be tied to either VD+ or DGND. CH1/2 is an output, and will change at the start of each new conversion cycle, indicating which channel will be tracked after the current conversion is finished (Figure 6).

The SSH/SDL goes low coincident with the first falling edge of SCLK, and returns high 2 CLKIN cycles after the last rising edge of SCLK. This signal frames the 16 data bits and is useful for interfacing to shift registers (e.g. 74HC595) or to DSP serial ports.

## SYSTEM DESIGN WITH THE CS5101A AND CS5102A

Figure 8 shows a general system connection diagram for the CS5101A and CS5102A.

### Digital Circuit Connections

When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

### System Initialization

Upon power up, the CS5101A and CS5102A must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to each device's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before  $\overline{\text{RST}}$  rises to guarantee an accurate calibration. Later, the CS5101A and CS5102A may be reset at any time to initiate a single full calibration.

When  $\overline{\text{RST}}$  is brought low all internal logic clears. When  $\overline{\text{RST}}$  returns high on the CS5101A, a calibration cycle begins which takes 11,528,160 master clock cycles to complete (approximately 1.4 seconds with an 8 MHz master clock). The



calibration cycle on the CS5102A takes 2,882,040 master clock cycles to complete (approximately 1.8 seconds with a 1.6 MHz master clock). The CS5101A's and CS5102A's  $\overline{\text{STBY}}$  output remains low throughout the calibration sequence, and a rising transition indicates the device is ready for normal operation. While calibrating, the CS5101A and CS5102A will ignore changes on the  $\overline{\text{HOLD}}$  input.

To perform the reset function, a simple power-on reset circuit can be built using a resistor and capacitor as shown in Figure 7. The resistor

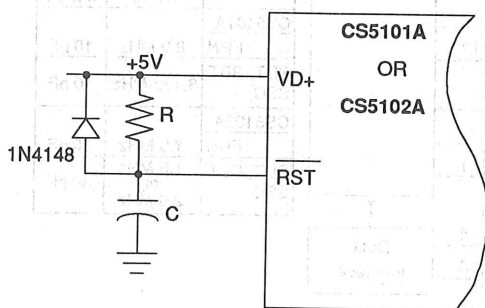


Figure 7. Power-up Reset Circuit

should be less than or equal to 10 k $\Omega$ . The system power supplies, voltage reference, and clock should all be established prior  $\overline{\text{RST}}$  rising.

### Single-Channel Operation

The CS5101A and CS5102A can alternatively be used to sample one channel by tying the  $\text{CH1}/2$  input high or low. The unused AIN pin should be tied to the analog input signal or to AGND. (If operating in free run mode, AIN1 and AIN2 must be tied to the same source, as  $\text{CH1}/2$  is reconfigured as an output.)

### ANALOG CIRCUIT CONNECTIONS

Most popular successive approximation A/D converters generate dynamic loads at their analog

connections. The CS5101A and CS5102A internally buffer all analog inputs (AIN1, AIN2, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

### Reference Considerations

An application note titled "Voltage References for the CS501X Series of A/D Converters" is available for the CS5101A and CS5102A. In addition to working through a reference circuit design example, it offers several built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5101A and CS5102A each include an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to coarse-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after coarse-charging from the buffer. This creates an ac current load as the CS5101A and CS5102A sequence through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog



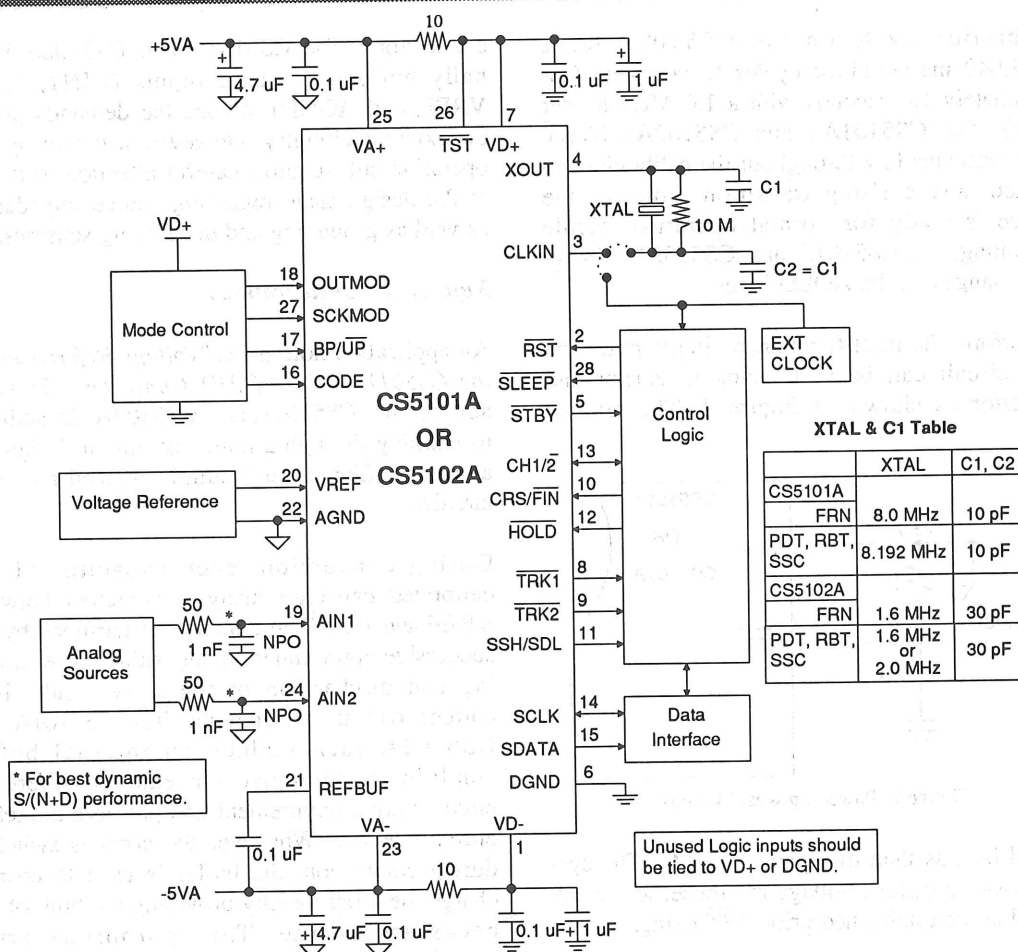


Figure 8. CS5101A/CS5102A System Connection Diagram

input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate

frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At the full-rated 9.216 MHz clock (CS5101A), the reference must supply a maximum load current of 20  $\mu$ A peak-to-peak (2  $\mu$ A typical). An output impedance of 2  $\Omega$  will therefore yield a maximum error of 40  $\mu$ V. At the full-rated 2.0 MHz clock (CS5102A), the refer-

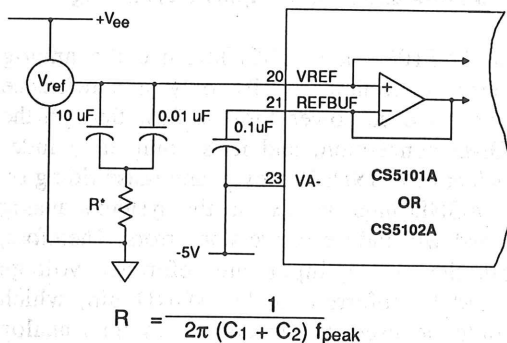


Figure 9. Reference Connections

ence must supply a maximum load current of 5  $\mu$ A peak-to-peak (0.5  $\mu$ A typical). An output impedance of 2  $\Omega$  will therefore yield a maximum error of 10.0  $\mu$ V. With a 4.5 V reference and LSB size of 138  $\mu$ V this would insure approximately 1/14 LSB accuracy. A 10  $\mu$ F capacitor exhibits an impedance of less than 2  $\Omega$  at frequencies greater than 16 kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors. The equation in Figure 9 can be used to help calculate the optimum value of R for a particular reference. The term "f<sub>peak</sub>" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CS5101A and CS5102A can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5101A and CS5102A can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby in-

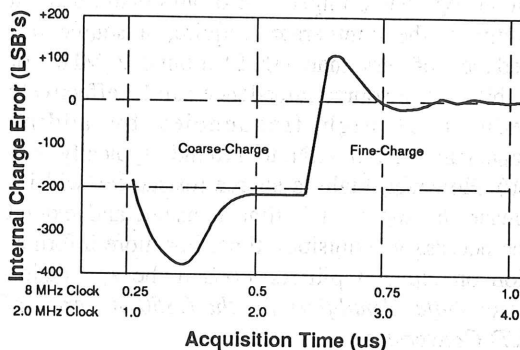


Figure 10. Charge Settling Time  
(8 and 2.0 MHz Clocks)

creasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1  $\mu$ F ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: Voltage References for the CS501X Series of A/D Converters".

### Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for coarse-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 10 shows this operation. During coarse-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage may be offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

Fine-charge settling is specified as a maximum of 1.125  $\mu$ s (CS5101A) or 5.625  $\mu$ s (CS5102A) for

an analog source impedance of less than 50  $\Omega$ . In addition, the comparator requires a source impedance of less than 400  $\Omega$  around 2 MHz for stability. The source impedance can be effectively reduced at high frequencies by adding capacitance from AIN to ground (typically 200 pF). However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more information on input amplifiers, consult the application note: *Buffer Amplifiers for the CS501X Series of A/D Converters*.

### ***SLEEP Mode Operation***

The CS5101A and CS5102A include a SLEEP pin. When SLEEP is active (low) each device will dissipate very low power to retain its calibration memory when the device is not sampling. It does not require calibration after SLEEP is made inactive (high). When coming out of SLEEP, sampling can begin as soon as the oscillator starts (time will depend on the particular oscillator components) and the REFBUF capacitor is charged (which takes about 3 ms for the CS5101A, 50 ms for the CS5102A). To achieve minimum start-up time, use an external clock and leave the voltage reference powered-up. Connect a resistor (2 k $\Omega$ ) between pins 20 and 21 to keep the REFBUF capacitor charged. Conversion can then begin as soon as the A/D circuitry has stabilized and performed a track cycle.

To retain calibration memory while SLEEP is active (low) VA+ and VD+ must be maintained at greater than 2.0V. VA- and VD- can be allowed to go to 0 volts. The voltages into VA- and VD- cannot just be "shut-off" as these pins cannot be allowed to float to potentials greater than AGND/DGND. If the supply voltages to VA- and VD- are removed, use a transistor switch to short these to the power supply ground while in SLEEP mode.

### ***Grounding and Power Supply Decoupling***

The CS5101A and CS5102A use the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground reference.

The digital and analog supplies are isolated within the CS5101A and CS5102A and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1  $\mu$ F ceramic capacitors. If significant low-frequency noise is present on the supplies, tantalum capacitors are recommended in parallel with the 0.1  $\mu$ F capacitors.

The positive digital power supply of the CS5101A and CS5102A must never exceed the positive analog supply by more than a diode drop or the CS5101A and CS5102A could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram (Figure 8) shows a decoupling scheme which allows the CS5101A and CS5102A to be powered from a single set of  $\pm 5$ V rails. The positive digital supply is derived from the analog supply through a 10  $\Omega$  resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10  $\Omega$  resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CS5101A and CS5102A require careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the devices. The CDB5101A evaluation board is available for the CS5101A, and the CDB5102A evaluation board is available for the CS5102A. The availability of these boards avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. Each board comes with a socketed CS5101A or CS5102A, and can be reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

### **CS5101A AND CS5102A PERFORMANCE**

#### **Differential Nonlinearity**

The self-calibration scheme utilized in the CS5101A and CS5102A features a calibration resolution of 1/4 LSB, or 18-bits. This ideally yields DNL of  $\pm 1/4$  LSB, with code widths ranging from 3/4 to 5/4 LSB's.

Traditional laser trimmed ADC's have significant differential nonlinearities. Appearing as wide and narrow codes, DNL often causes entire sections of the transfer function to be missing. Although their affect is minor on  $S/(N+D)$  with high amplitude signals, DNL errors dominate performance with low-level signals. For instance, a signal 80 dB below full-scale will slew past only 6 or 7 codes. Half of those codes could be missing with a conventional 16-bit ADC which achieves only 14-bit DNL.

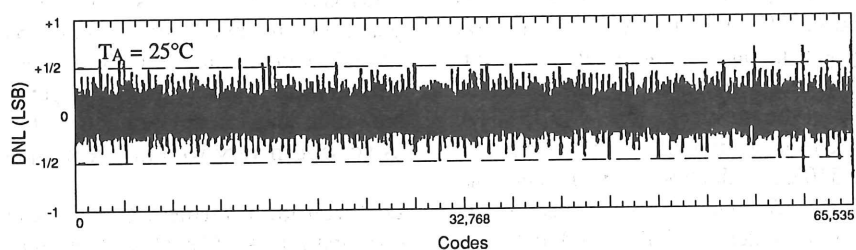
The most common source of DNL errors in conventional ADC's is bit weight errors. These can arise due to accuracy limitations in factory trim stations, thermal or physical stresses after calibration, and/or drifts due to aging or temperature variations in the field. Bit-weight errors have a drastic effect on a converter's ac performance.

They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions.

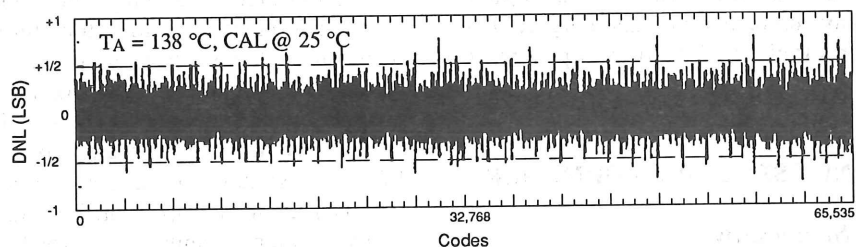
Differential nonlinearities in successive-approximation ADC's also arise due to dynamic errors in the comparator. Such errors can dominate if the converter's throughput/sampling rate is too high. The comparator will not be allowed sufficient time to settle during each bit decision in the successive-approximation algorithm. The worst-case codes for dynamic errors are the major transitions (1/2 FS; 1/4, 3/4 FS; etc.). Since DNL effects are most critical with low-level signals, the codes around mid-scale (1/2 FS) are most important. Yet those codes are worst-case for dynamic DNL errors!

With all linearity calibration performed on-chip to 18-bits, the CS5101A and CS5102A maintain accurate bit weights. DNL errors are dominated by residual calibration errors of  $\pm 1/4$  LSB rather than dynamic errors in the comparator. Furthermore, *all* DNL effects on  $S/(N+D)$  are buried by white broadband noise. (See Figures 17 and 19).

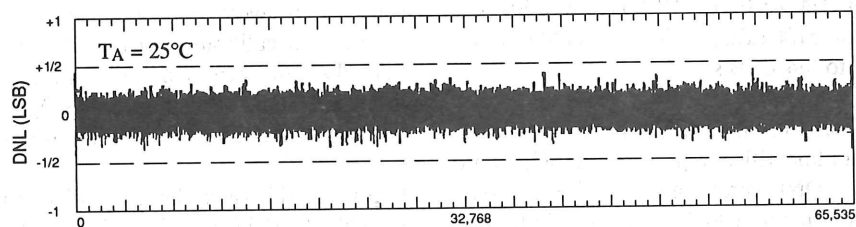
Figure 11 illustrates the DNL histogram plot of a typical CS5101A at 25°C. Figure 12 illustrates the DNL of the CS5101A at 138°C ambient after calibration at 25°C ambient. Figures 13 and 14 illustrate the DNL of the CS5102A at 25°C and 138°C ambient, respectively. A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will



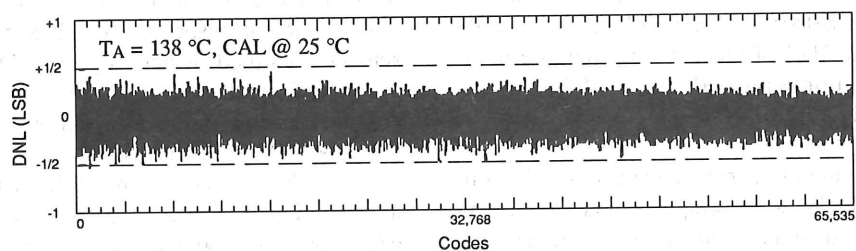
**Figure 11. CS5101A DNL Plot; Ambient Temperature at 25°C**



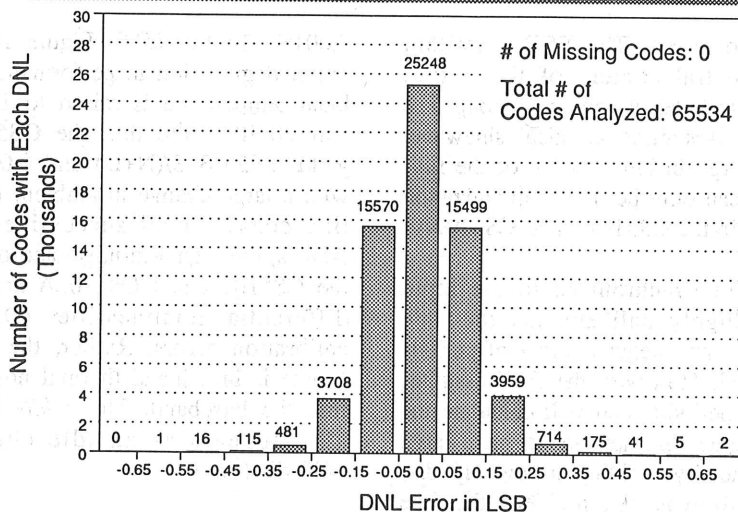
**Figure 12. CS5101A DNL Plot; Ambient Temperature at 138°C**



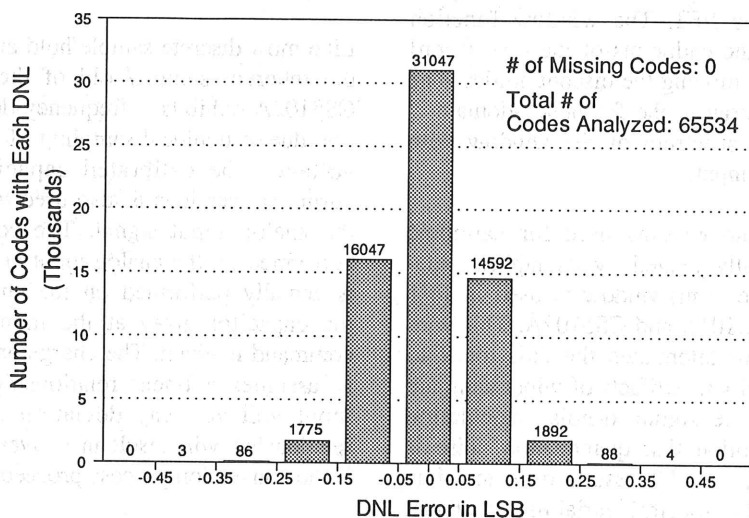
**Figure 13. CS5102A DNL Plot; Ambient Temperature at 25°C**



**Figure 14. CS5102A DNL Plot; Ambient Temperature at 138°C**



**Figure 15. CS5101A DNL Error Distribution**



**Figure 16. CS5102A DNL Error Distribution**

appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Figures 15 and 16 illustrate the code width distribution of the DNL plots shown in Figures 11 and 13 respectively. The DNL error distribution plots indicate that the CS5101A and CS5102A calibrate the majority of their codes to tighter

tolerance than the DNL plots in Figures 11 and 13 appear to indicate.

### ***FFT Tests and Windowing***

In the factory, the CS5101A and CS5102A are tested using Fast Fourier Transform (FFT) techniques to analyze the converters' dynamic performance. A pure sinewave is applied to the device, and a "time record" of 1024 samples is



captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5101A and CS5102A.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. A five term window is used in FFT testing of the CS5101A and CS5102A. This windowing algorithm attenuates the side-lobes to below the noise floor. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. Averaging the FFT results from ten time records filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics are visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Crystal Semiconductor.

As illustrated in Figure 17, the CS5101A typically provides about 92 dB S/(N+D) and

0.001% THD at 25°C. Figure 18 illustrates only minor degradation in performance when the ambient temperature is raised to 138°C. Figure 19 and 20 illustrate that the CS5102A typically yields >92 dB S/(N+D) and 0.001% THD even with a large change in ambient temperature. Unlike conventional successive-approximation ADC's, the signal-to-noise and dynamic range of the CS5101A and CS5102A are not limited by differential nonlinearities (DNL) caused by calibration errors. Rather, the dominant noise source is broadband thermal noise which aliases into the baseband. This *white* broadband noise also appears as an idle channel noise of 1/2 LSB (rms).

### *Sampling Distortion*

Like most discrete sample/hold amplifier designs, the inherent sample/hold of the CS5101A and CS5102A exhibits a frequency-dependent distortion due to nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the HOLD command is given. The charge on the array ideally assumes a linear relationship to the analog input voltage. Any deviation from this linear relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between the charge on the array and the analog input voltage and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figures 17,18,19, and 20).

The ideal relationship between the charge on the array and the input voltage can also be distorted



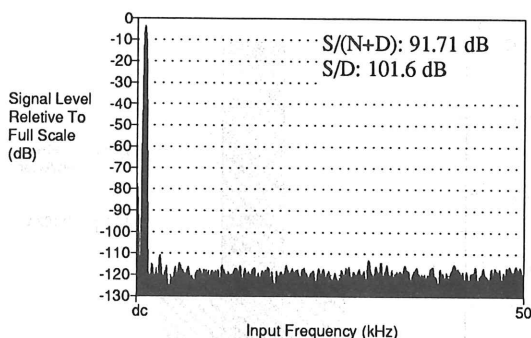


Figure 17. CS5101A FFT (SSC Mode, 1-Channel)

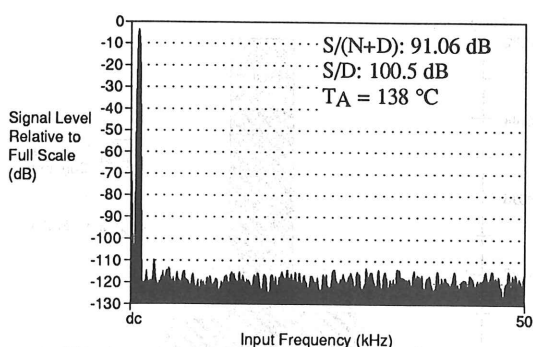


Figure 18. CS5101A FFT (SSC Mode, 1-Channel)

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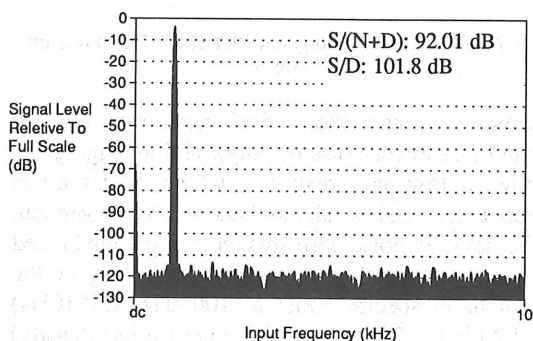


Figure 19. CS5102A FFT (SSC Mode, 1-Channel)

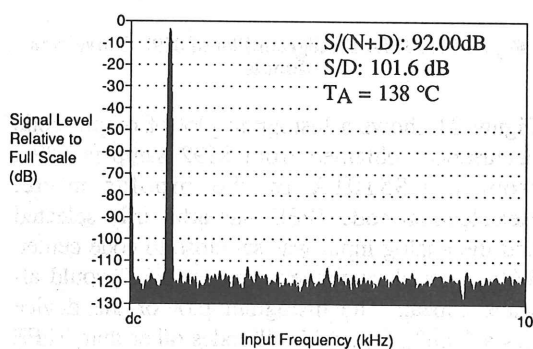


Figure 20. CS5102A FFT (SSC Mode, 1-Channel)

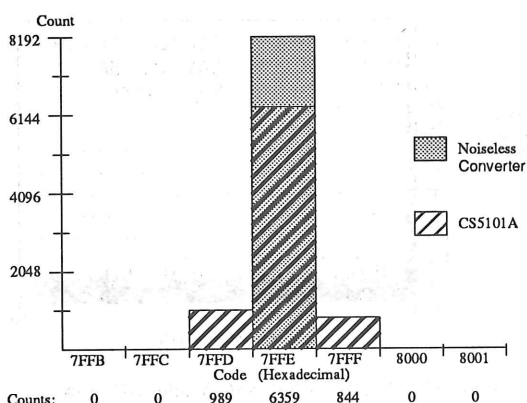
at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency and slew rate. This distortion is negligible at signal levels below -10 dB of full-scale.

### Noise

An A/D converter's noise can be described like that of any other analog component. However, the converter's output is in digital form so any filtering of its noise must be performed in the digital domain. Digitized samples of analog in-

puts are often considered individual, static snapshots in time with no uncertainty or noise. In reality, the result of each conversion depends on the analog input level and the instantaneous value of noise sources in the ADC. If sequential samples from the ADC are treated as a "waveform", simple filtering can be implemented in software to improve noise performance with minimal processing overhead.

All analog circuitry in the CS5101A and CS5102A is wideband in order to achieve fast conversions and high throughput. Wideband noise in the CS5101A and CS5102A integrates to 35  $\mu\text{V}$  rms in unipolar mode (70  $\mu\text{V}$  rms in bipolar mode). This is approximately 1/2 LSB rms with a 4.5V reference in both modes.

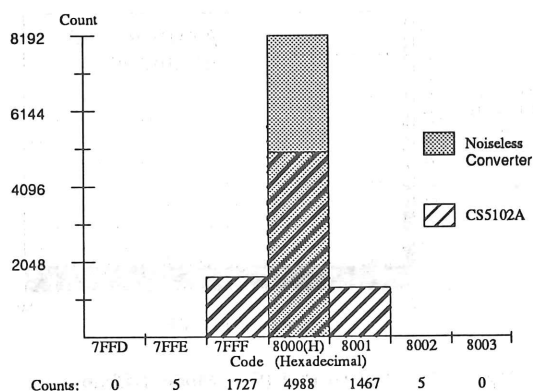


**Figure 21. 5101A Histogram Plot of 8192 Conversion Inputs**

Figure 21 shows a histogram plot of output code occurrences obtained from 8192 samples taken from a CS5101A in the bipolar mode. Hexadecimal code 7FFE was arbitrarily selected and the analog input was set close to code center. With a noiseless converter, code 7FFE would always appear. The histogram plot of the device has a "bell" shape with all codes other than 7FFE due to internal noise. Figure 22 illustrates the noise histogram of the CS5102A.

In a sampled data system all information about the analog input applied to the sample/hold appears in the baseband from dc to one-half the sampling rate. This includes high-frequency components which alias into the baseband. Low-pass (anti-alias) filters are therefore used to remove frequency components in the input signal which are above one-half the sample rate. However, all wideband noise introduced by the CS5101A and CS5102A still aliases into the baseband. This "white" noise is evenly spread from dc to one-half the sampling rate and integrates to 35  $\mu$ V rms in unipolar mode.

Noise in the digital domain can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Over-

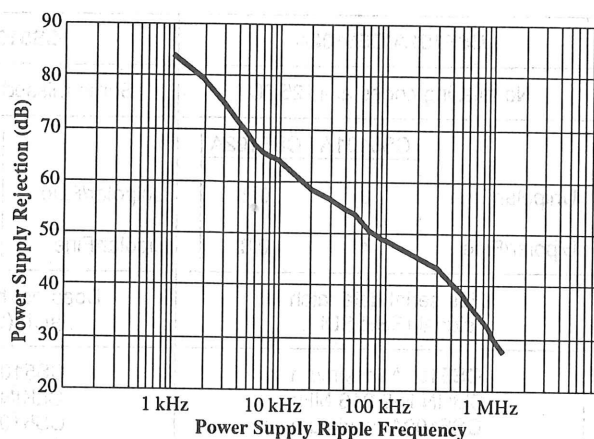


**Figure 22. 5102A Histogram Plot of 8192 Conversion Inputs**

sampling spreads the device's noise over a wider band (for lower noise density), and averaging applies a low-pass response which filters noise above the desired signal bandwidth. In general, the device's noise performance can be maximized in any application by always sampling at the maximum specified rate of 100 kHz (CS5101A) or 20 kHz (CS5102A) (for lowest noise density) and digitally filtering to the desired signal bandwidth.

### Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependency causes distortion at high frequencies. The proprietary architecture of the CS5101A and CS5102A avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter, due to component noise, assumes a random nature. With only 100 ps peak-to-peak aperture jitter, the CS5101A and CS5102A can process full-scale signals up to 1/2 the throughput frequency without significant errors due to aperture jitter.



**Figure 23. Power Supply Rejection**

### Power Supply Rejection

The power supply rejection performance of the CS5101A and CS5102A is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the device's accuracy. This is because the CS5101A and CS5102A adjust their offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 23 shows power supply rejection of the CS5101A and CS5102A in the bipolar mode with the analog input grounded and a 300 mV p-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The plot shows worst-case rejection for all combinations

of conversion rates and input conditions in the bipolar mode.

### CS5101A/CS5102A Improvements Over Earlier CS5101/CS5102

The CS5101A/CS5102A are improved versions of the earlier CS5101/CS5102 devices. Primary improvements are:

- 1) Improved DNL at high temperature (>70 °C)
- 2) Improved input slew rate, yielding improved full scale settling between conversions.
- 3) Modifying the previous SSH pin to SSH/SDL (Simultaneous Sample Hold/Serial Data Latch). The SSH/SDL new function provides a logic signal which frames the 16 data bits in SSC and FRN serial modes. This signal is ideal for easy interface to serial to parallel shift registers (74HC595) and to DSP serial ports.

Table 3 summarizes all the improvements.

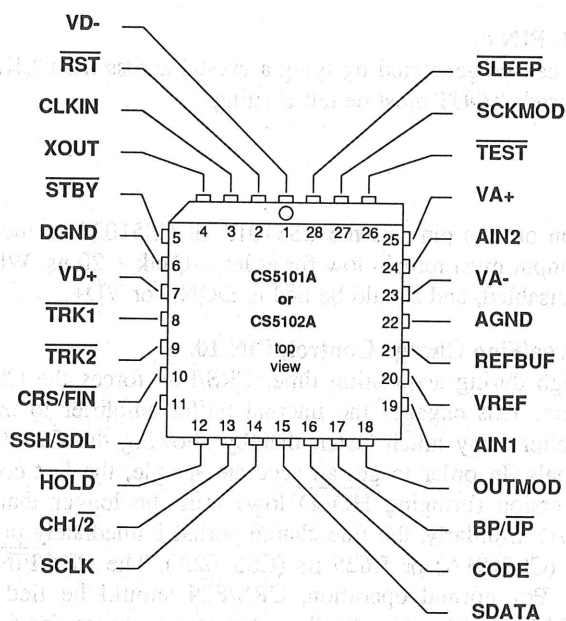
Function	CS5101A/CS5102A			CS5101/CS5102		
Better DNL	No missing codes at +125 °C			Some missed codes at +125 °C		
Faster Fine Charge Slew Rate (V/μs)		CS5101A	CS5102A		CS5101	CS5102
	Unipolar/Fine	2	0.4	Unipolar/Fine	1.3	0.1
	Bipolar/Fine	4	0.8	Bipolar/Fine	2.6	0.2
Improved Serial Interface	Has serial data latch signal (SSH/SDL).			Does not have serial data latch (SDL) signal.		
CLKIN Rate	CS5101A maximum CLKIN is 9.216 MHz CS5102A maximum CLKIN is 2.0 MHz			CS5101 maximum CLKIN is 8.0 MHz CS5102 maximum CLKIN is 1.6 MHz		
Code and BP/UP Pin Function	Independent setting of 2's complement or offset binary coding (CODE) and bipolar or unipolar input range (BP/UP)			Selecting unipolar input range forces offset binary operation, independent of the CODE pin state		
CRS/FIN Pin	Can be high or low during calibration			CRS/FIN must be held low during calibration		

**Table 3. CS5101A/CS5102A Improvements over CS5101/CS5102**

### PIN DESCRIPTIONS

NEGATIVE DIGITAL POWER	VD-	1	28	SLEEP	SLEEP (LOW POWER) MODE
RESET & INITIATE CALIBRATION	RST	2	27	SCKMOD	SERIAL CLOCK MODE SELECT
MASTER CLOCK INPUT	CLKIN	3	26	TEST	TEST
CRYSTAL OUTPUT	XOUT	4	25	VA+	POSITIVE ANALOG POWER
STANDBY (CALIBRATING)	STBY	5	24	AIN2	CHANNEL 2 ANALOG INPUT
DIGITAL GROUND	DGND	6	23	VA-	NEGATIVE ANALOG POWER
POSITIVE DIGITAL POWER	VD+	7	22	AGND	ANALOG GROUND
TRACKING CHANNEL 1	TRK1	8	21	REFBUF	REFERENCE BUFFER
TRACKING CHANNEL 2	TRK2	9	20	VREF	VOLTAGE REFERENCE
COARSE/FINE CHARGE CONTROL	CRS/FIN	10	19	AIN1	CHANNEL 1 ANALOG INPUT
SIMULTANEOUS S/H/SERIAL DATA LATCH	SSH/SDL	11	18	OUTMOD	OUTPUT MODE SELECT
HOLD & CONVERT	HOLD	12	17	BP/UP	BIPOLAR/UNIPOLAR SELECT
INPUT CHANNEL SELECT	CH1/2	13	16	CODE	BINARY/2's COMPLEMENT SELECT
SERIAL DATA CLOCK	SCLK	14	15	SDATA	SERIAL DATA OUTPUT

3



### ***Power Supply Connections***

**VD+ - Positive Digital Power, PIN 7.**

Positive digital power supply. Nominally +5 volts.

**VD- - Negative Digital Power, PIN 1.**

Negative digital power supply. Nominally -5 volts.

**DGND - Digital Ground, PIN 6.**

Digital ground [reference].

**VA+ - Positive Analog Power, PIN 25.**

Positive analog power supply. Nominally +5 volts.

**VA- - Negative Analog Power, PIN 23.**

Negative analog power supply. Nominally -5 volts.

**AGND - Analog Ground, PIN 22.**

Analog ground reference.

### ***Oscillator***

**CLKIN - Clock Input, PIN 3.**

All conversions and calibrations are timed from a master clock which can be externally supplied by driving CLKIN [with a CMOS-compatible clock].

**XOUT - Crystal Output, PIN 4.**

The master clock can be generated by tying a crystal across the CLKIN and XOUT pins. If an external clock is used, XOUT must be left floating.

### ***Digital Inputs***

**HOLD - Hold, PIN 12.**

A falling transition on this pin sets the CS5101A or CS5102A to the hold state and initiates a conversion. This input must remain low for at least  $1/t_{clk} + 20$  ns. When operating in Free Run Mode, HOLD is disabled, and should be tied to DGND or VD+.

**CRS/FIN - Coarse Charge/Fine Charge Control, PIN 10.**

When brought high during acquisition time, CRS/FIN forces the CS5101A or CS5102A into coarse charge state. This engages the internal buffer amplifier to track the analog input and charges the capacitor array much faster, thereby allowing the CS5101A or CS5102A to track high slewing signals. In order to get an accurate sample, the last coarse charge period before initiating a conversion (bringing HOLD low) must be longer than  $0.75 \mu s$  (CS5101A) or  $3.75 \mu s$  (CS5102A). Similarly, the fine charge period immediately prior to conversion must be at least  $1.125 \mu s$  (CS5101A) or  $5.625 \mu s$  (CS5102A). The CRS/FIN pin must be low during conversion time. For normal operation, CRS/FIN should be tied low, in which case the CS5101A or CS5102A will automatically enter coarse charge for 6 clock cycles immediately after the end of conversion.

**CH1/2 - Left/Right Input Channel Select, PIN 13.**

Status at the end of a conversion cycle determines which analog input channel will be acquired for the next conversion cycle. When in Free Run Mode, CH1/2 is an output, and will indicate which channel is being sampled during the current acquisition phase.

**SLEEP - Sleep, PIN 28.**

When brought low causes the CS5101A or CS5102A to enter a power-down state. All calibration coefficients are retained in memory, so no recalibration is needed after returning to the normal operating mode. If using the internal crystal oscillator, time must be allowed after SLEEP returns high for the crystal oscillator to stabilize. SLEEP should be tied high for normal operation.

**CODE - 2's Complement/Binary Coding Select, PIN 16.**

Determines whether output data appears in 2's complement or binary format. If high, 2's complement; if low, binary.

**BP/UP - Bipolar/Unipolar Input Range Select, PIN 17.**

When low, the CS5101A or CS5102A accepts a unipolar input range from AGND to VREF. When high, the CS5101A or CS5102A accepts bipolar inputs from -VREF to +VREF.

**SCKMOD - Serial Clock Mode Select, PIN 27.**

When high, the SCLK pin is an input; when low, it is an output. Used in conjunction with OUTMOD to select one of 4 output modes described in Table 2.

**OUTMOD - Output Mode Select, PIN 18.**

The status of SCKMOD and OUTMOD determine which of four output modes is utilized. The four modes are described in Table 2.

**SCLK - Serial Clock, PIN 14.**

Serial data changes status on a falling edge of this input, and is valid on a rising edge. When SCKMOD is high SCLK acts as an input. When SCKMOD is low the CS5101A or CS5102A generates its own serial clock at one-fourth the master clock frequency and SCLK is an output.

**RST - Reset, PIN 2.**

When taken low, all internal digital logic is reset. Upon returning high, a full calibration sequence is initiated which takes 11,528,160 CLKIN cycles (CS5101A) or 2,882,040 CLKIN cycles (CS5102A) to complete. During calibration, the HOLD input will be ignored. The CS5101A or CS5102A must be reset at power-up for calibration, however; calibration is maintained during SLEEP mode, and need not be repeated when resuming normal operation.

**Analog Inputs**
**AIN1, AIN2 - Channel 1 and 2 Analog Inputs, PINS 19 and 24.**

Analog input connections for the left and right input channels.

**VREF - Voltage Reference, PIN 20.**

The analog reference voltage which sets the analog input range. In unipolar mode VREF sets full-scale; in bipolar mode its magnitude sets both positive and negative full-scale.



### **Digital Outputs**

#### **STBY - Standby (Calibrating), PIN 5.**

Indicates calibration status after reset. Remains low throughout the calibration sequence and returns high upon completion.

#### **SDATA - Serial Output, PIN 15.**

Presents each output data bit on a falling edge of SCLK. Data is valid to be latched on the rising edge of SCLK.

#### **SSH/SDL - Simultaneous Sample/Hold / Serial Data Latch, PIN 11.**

Used to control an external sample/hold amplifier to achieve simultaneous sampling between channels. In FRN and SSC modes (SCLK is an output), this signal provides a convenient latch signal which forms the 16 data bits. This can be used to control external serial to parallel latches, or to control the serial port in a DSP.

#### **TRK1, TRK2 - Tracking Channel 1, Tracking Channel 2, PINS 8 and 9.**

Falls low at the end of a conversion cycle, indicating the acquisition phase for the corresponding channel. The TRK1 or TRK2 pin will return high at the beginning of conversion for that channel.

### **Analog Outputs**

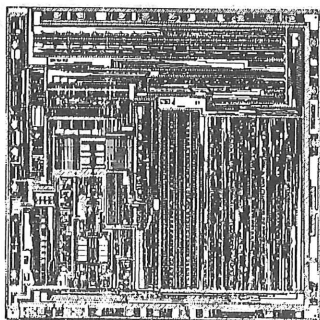
#### **REFBUF - Reference Buffer Output, PIN 21.**

Reference buffer output. A 0.1  $\mu$ F ceramic capacitor must be tied between this pin and VA-.

### **Miscellaneous**

#### **TEST - Test, PIN 26.**

Allows access to the CS5101A's and the CS5102A's test functions which are reserved for factory use. Must be tied to VD+.

**DIE INFORMATION**

**CS5101A-YU  
CS5102A-YU**

**3**

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

**Assembly Information**

1. Die size for the CS5101A & CS5102A die are 0.273" X 0.265" ( $\pm 0.002$ ").

2. The die are suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.

3. Die thickness shall be 0.0175"  $\pm 0.0035$ ". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 25.

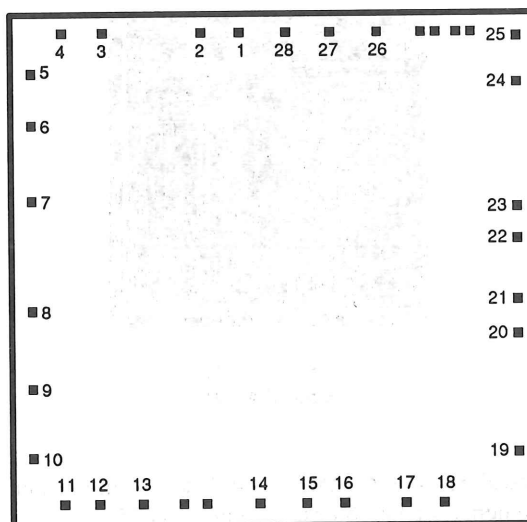
5. The cavity dimensions for each die within the waffle pack are .300" by .300" (Waffle Pack Type H20-300).

6. The die require no particular bonding sequence.

7. Each pin of the CS5101A and CS5102A has ESD and latch-up protection circuitry. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.

8. Technical constraints limit the viability of accurate performance measurements of precision analog IC's at wafer probe. Although high yield to the limits listed in the specification tables is anticipated, no guarantee is given for unpackaged die product.

**CS5101A-U, CS5102A-U Bonding Diagram**



- |                     |                    |
|---------------------|--------------------|
| 1 - <u>VD-</u>      | 15 - <u>SDATA</u>  |
| 2 - <u>RST</u>      | 16 - <u>CODE</u>   |
| 3 - <u>CLKIN</u>    | 17 - <u>BP/UP</u>  |
| 4 - <u>XOUT</u>     | 18 - <u>OUTMOD</u> |
| 5 - <u>STBY</u>     | 19 - <u>AIN1</u>   |
| 6 - <u>DGND</u>     | 20 - <u>VREF</u>   |
| 7 - <u>VD+</u>      | 21 - <u>REFBUF</u> |
| 8 - <u>TRK1</u>     | 22 - <u>AGND</u>   |
| 9 - <u>TRK2</u>     | 23 - <u>VA-</u>    |
| 10 - <u>CRS/FIN</u> | 24 - <u>AIN2</u>   |
| 11 - <u>SSH</u>     | 25 - <u>VA+</u>    |
| 12 - <u>HOLD</u>    | 26 - <u>TEST</u>   |
| 13 - <u>CH1/2</u>   | 27 - <u>SCKMOD</u> |
| 14 - <u>SCLK</u>    | 28 - <u>SLEEP</u>  |

**Ordering Guide (CS5101A)**

Model	Conversion Time	Throughput	Linearity	Temperature	Package
CS5101A-JP8	8.13 $\mu$ s	100 kHz	0.003%	0 to 70 °C	28-Pin Plastic DIP
CS5101A-KP8	8.13 $\mu$ s	100 kHz	0.002%	0 to 70 °C	28-Pin Plastic DIP
CS5101A-JP16	16.25 $\mu$ s	50 kHz	0.003%	0 to 70 °C	28-Pin Plastic DIP
CS5101A-JL8	8.13 $\mu$ s	100 kHz	0.003%	0 to 70 °C	28-Pin PLCC
CS5101A-KL8	8.13 $\mu$ s	100 kHz	0.002%	0 to 70 °C	28-Pin PLCC
CS5101A-JL16	16.25 $\mu$ s	50 kHz	0.003%	0 to 70 °C	28-Pin PLCC
CS5101A-AP8	8.13 $\mu$ s	100 kHz	0.003%	-40 to 85 °C	28-Pin Plastic DIP
CS5101A-BP8	8.13 $\mu$ s	100 kHz	0.002%	-40 to 85 °C	28-Pin Plastic DIP
CS5101A-AL8	8.13 $\mu$ s	100 kHz	0.003%	-40 to 85 °C	28-Pin PLCC
CS5101A-BL8	8.13 $\mu$ s	100 kHz	0.002%	-40 to 85 °C	28-Pin PLCC
CS5101A-SD8	8.13 $\mu$ s	100 kHz	0.004%	-55 to 125 °C	28-Pin CerDIP
CS5101A-TD8	8.13 $\mu$ s	100 kHz	0.003%	-55 to 125 °C	28-Pin CerDIP

CS5101A-YU

Unpackaged Die

**3**
**MIL-STD-883 Rev C. (SMD) Versions**

SMD Number: 5962-91691

Refer to SMD for accuracy and package suffixes.

**Ordering Guide (CS5102A)**

Model	Conversion Time	Throughput	Linearity	Temperature	Package
CS5102A-JP	40 $\mu$ s	20 kHz	0.003%	0 to 70 °C	28-Pin Plastic DIP
CS5102A-KP	40 $\mu$ s	20 kHz	0.0015%	0 to 70 °C	28-Pin Plastic DIP
CS5102A-JL	40 $\mu$ s	20 kHz	0.003%	0 to 70 °C	28-Pin PLCC
CS5102A-KL	40 $\mu$ s	20 kHz	0.0015%	0 to 70 °C	28-Pin PLCC
CS5102A-AP	40 $\mu$ s	20 kHz	0.003%	-40 to 85 °C	28-Pin Plastic DIP
CS5102A-BP	40 $\mu$ s	20 kHz	0.0015%	-40 to 85 °C	28-Pin Plastic DIP
CS5102A-AL	40 $\mu$ s	20 kHz	0.003%	-40 to 85 °C	28-Pin PLCC
CS5102A-BL	40 $\mu$ s	20 kHz	0.0015%	-40 to 85 °C	28-Pin PLCC
CS5102A-SD	40 $\mu$ s	20 kHz	0.004%	-55 to 125 °C	28-Pin CerDIP
CS5102A-TD	40 $\mu$ s	20 kHz	0.002%	-55 to 125 °C	28-Pin CerDIP

CS5102A-YU

Unpackaged Die

**MIL-STD-883 Rev C. (SMD) Versions**

SMD Number: 5962-91692

Refer to SMD for accuracy and package suffixes.

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**PARAMETER DEFINITIONS****Linearity Error**

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

**Differential Linearity**

Minimum resolution for which no missing codes is guaranteed. Units in bits.

**Full Scale Error**

The deviation of the last code transition from the ideal ( $V_{REF}-3/2$  LSB's). Units in LSB's.

**Unipolar Offset**

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

**Bipolar Offset**

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/UP high). Units in LSB's.

**Bipolar Negative Full-Scale Error**

The deviation of the first code transition from the ideal when in bipolar mode (BP/UP high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

**Signal to Peak Harmonic or Noise**

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

**Total Harmonic Distortion**

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

**Signal-to-(Noise + Distortion)**

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

**Aperture Time**

The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

**Aperture Jitter**

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

## Evaluation Board for CS5101A & CS5102A

### Features

- Serial to Parallel Conversion
- Adjustable Voltage Reference
- $\pm 5$  V Regulators
- Digital and Analog Patch Areas

### General Description

The CDB5101A/5102A Evaluation Board allows fast evaluation of the CS5101A and CS5102A 2-Channel, 16-bit Analog-to-Digital Converters.

Analog inputs are via BNC connectors. Digital outputs are available both directly from the ADC in serial form, and in 16 bit parallel form.

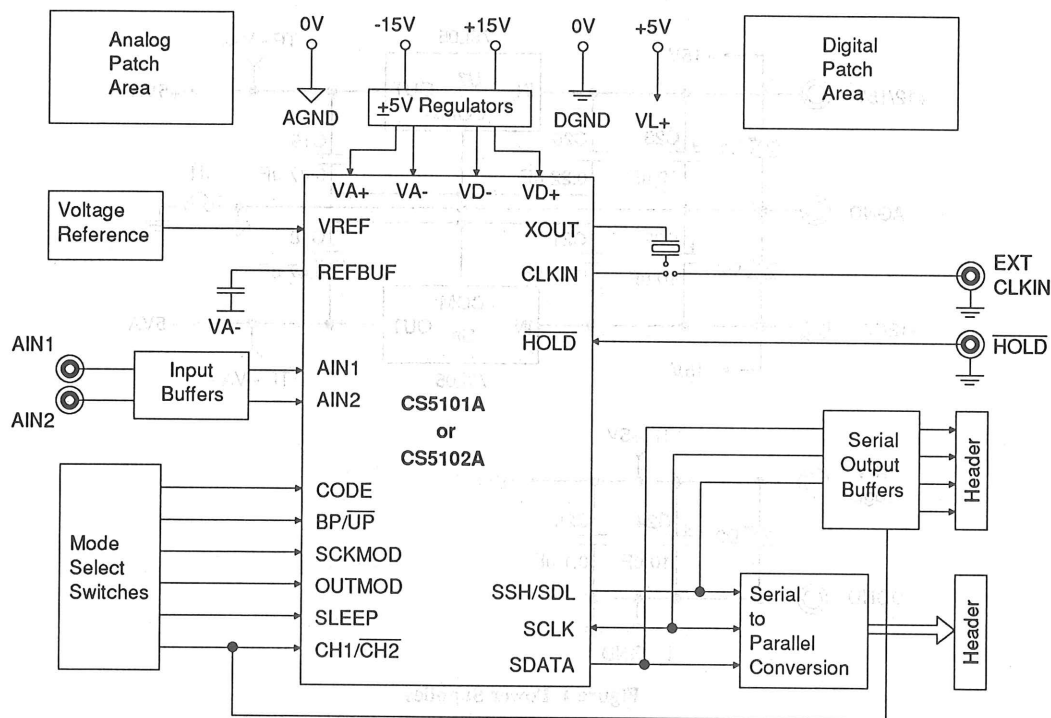
An adjustable monolithic voltage reference is included.

### Ordering Information

CDB5101A  
CDB5102A

3

### Block Diagram



## Power Supplies

Figure 1 shows the power supply arrangements. The analog section of the board is powered by  $\pm 12/15$  volts, which is regulated down to  $\pm 5V$  for the ADC. A separate +5V digital supply is required to power the discrete logic.

### Analog Input

The CS5101A/02A converters have a two-channel multiplexer input. Separate amplifiers (see Figure 2) are provided on the evaluation board to drive each input independently. If the converter is used in FRN mode, the multiplexer "ping-pongs" between channels. If only one signal is to be digitized in FRN mode at full speed, the AIN1 and AIN2 pins on the converter should be shorted together. Then the amplifier circuitry

for the unused channel should be disconnected. For example, if only Analog Input one is used (in FRN mode) as the input, short the AIN1 and AIN2 pins of the converter and remove R15 and C15.

If you do not want to use the on-board amplifiers, connect your signal to TP27 for channel 1 and TP32 for channel 2. Use TP28 and TP31 to break the connection to the output of the on-board buffers. Your own buffer amplifiers may be installed in the 2 analog patch areas. For critical 2 channel applications, keep the signal path for the 2 channels identical.

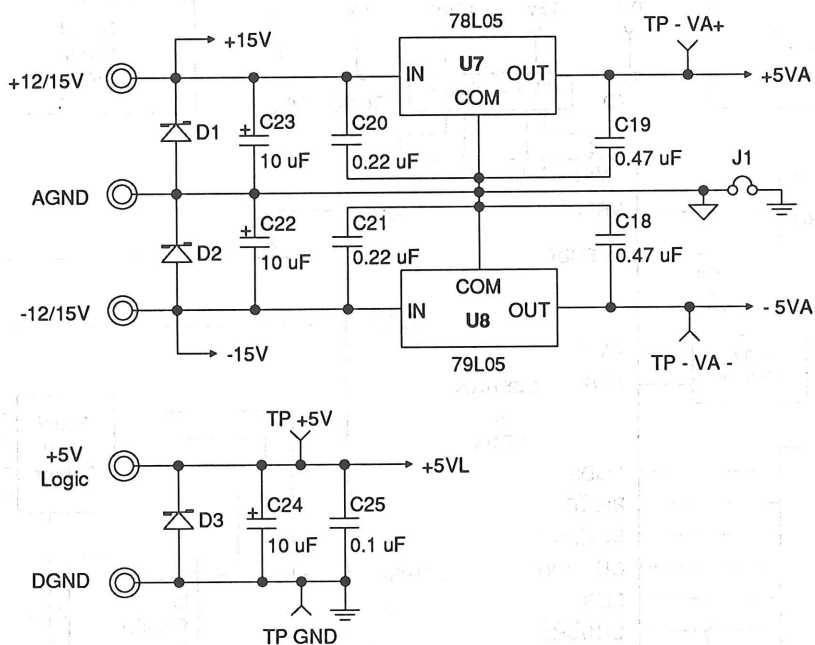


Figure 1. Power Supplies



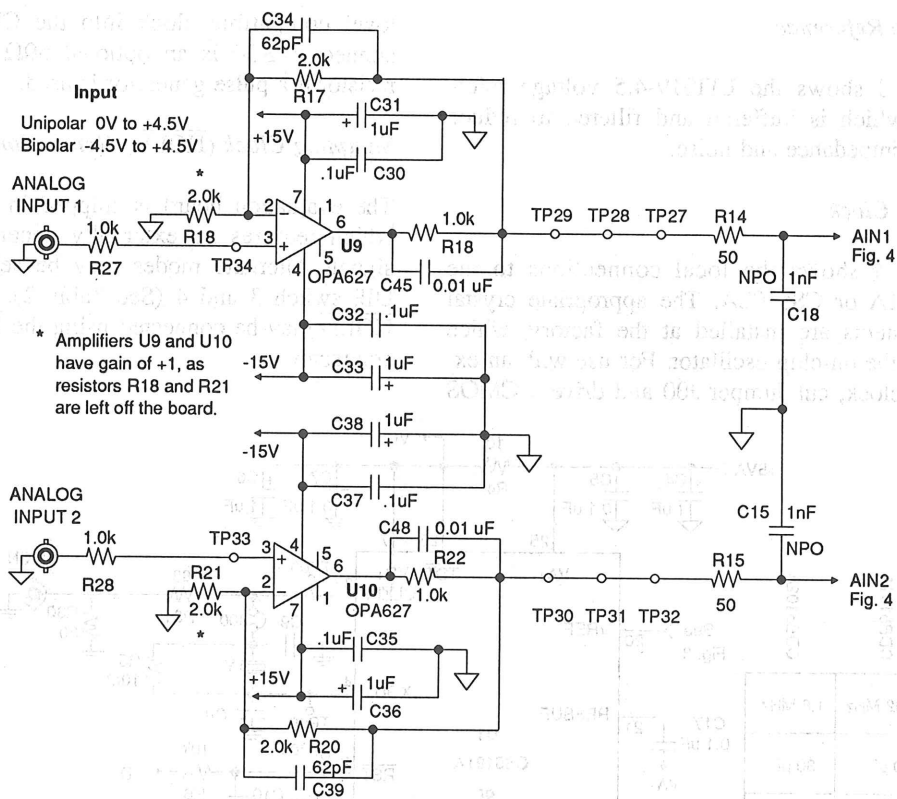


Figure 2. Input Buffer Circuit.

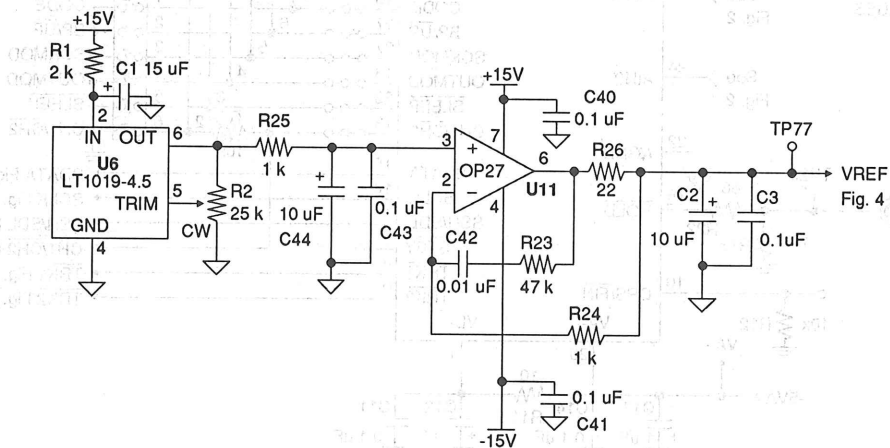


Figure 3. Voltage Reference

## Voltage Reference

Figure 3 shows the LTI019-4.5 voltage reference, which is buffered and filtered to reduce output impedance and noise.

## Master Clock

Figure 4 shows the local connections to the CS5101A or CS5102A. The appropriate crystal components are installed at the factory, which utilize the on-chip oscillator. For use with an external clock, cut Jumper J00 and drive a CMOS

level compatible clock into the CLKIN BNC connector. R30 is an optional 50Ω terminating resistor if a pulse generator is used.

## Sampling Clock (HOLD) Generation

The evaluation board is shipped in FRN mode, which requires no externally generated HOLD signal. Alternate modes may be selected using DIP switch 3 and 4 (See Table 2). An external HOLD may be connected using the HOLD BNC connector.

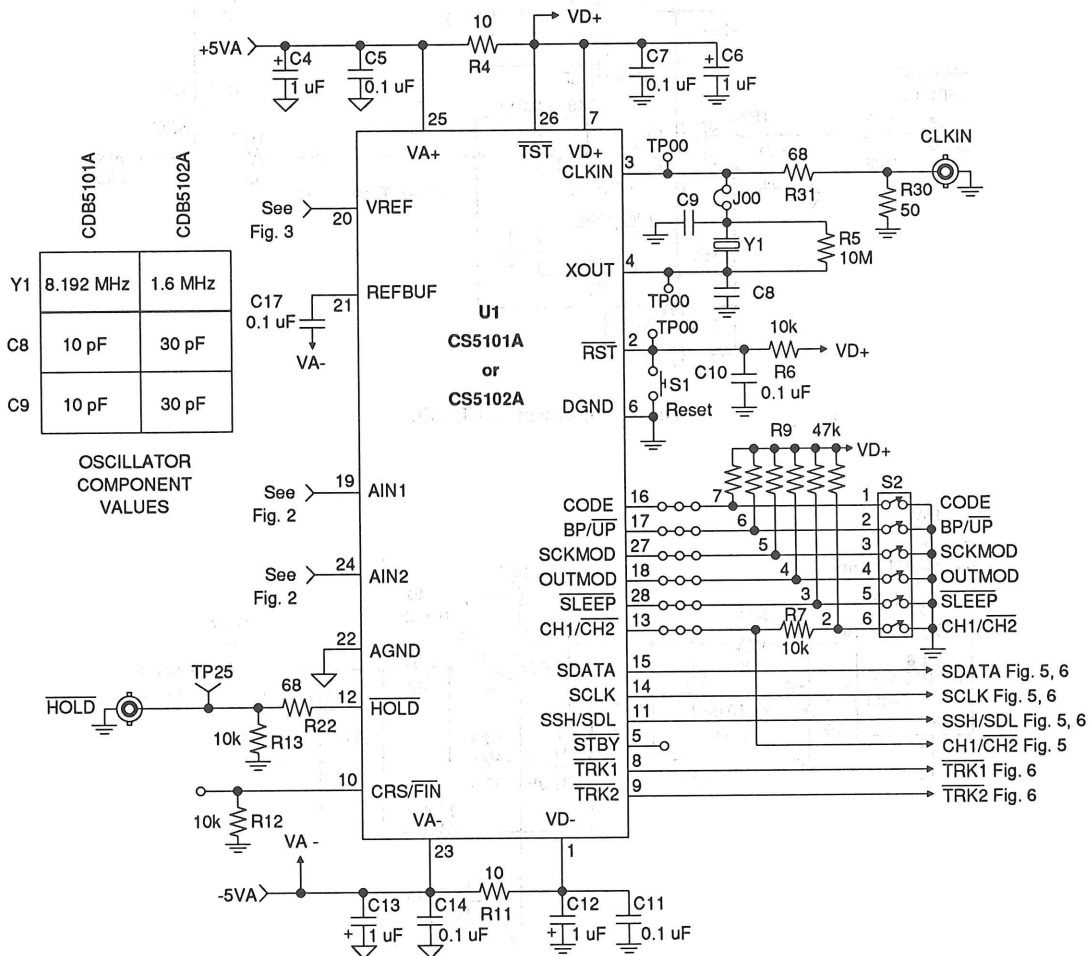


Figure 4. ADC Connections

### Control Signals

Figure 5 shows 2 headers are provided for serial data output and control signals. JP3 provides SDATA and SSH/SDL outputs. It also allows access to SCLK & CH1/CH2 which may be inputs or outputs depending on the serial mode selected by the DIP switches. Jumpers J10, J11, J12, & J13 must be set to correspond with the appropriate directions of SCLK and CH1/CH2.

JP5 provides output only access to the +5V logic supply, SCLK, SDATA and SLATCH, the serial to parallel latching control.

### Serial to Parallel Conversion

When operating in the FRN or SSC serial port modes, the CS5101A/02A readily provides the three signals (SCLK, SDATA, and SSH/SDL) to support serial to parallel conversion of its output data.

Figure 6 Shows 2 74HC595's provided to convert the serial output of the ADC to parallel. A handshake flip-flop, U3, is provided for the parallel interface if required. When parallel data is available to read,  $\overline{DRDY}$  goes low. The computer reads the data and sets DACK high and then low. This resets the flip-flop for the next word. JP4 selects whether both CH1 and CH2 data appears alternately, or CH1 only, or CH2 only.

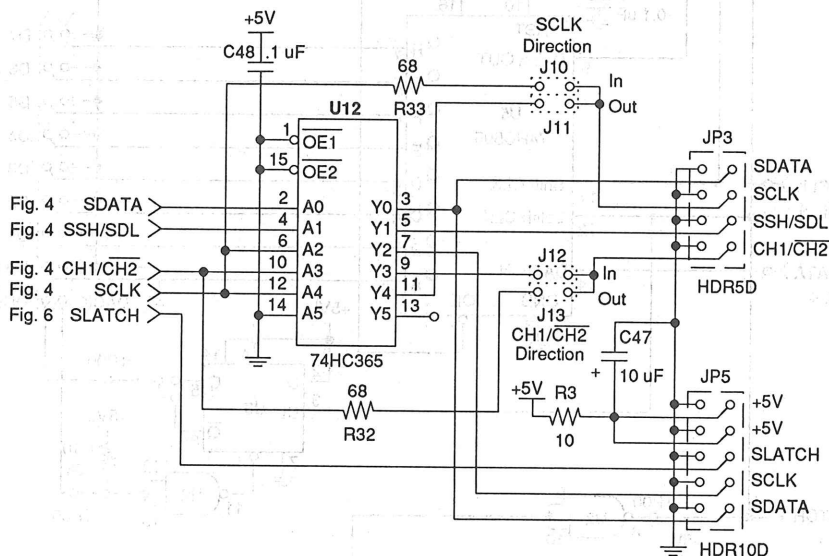


Figure 5. Serial Output Buffers

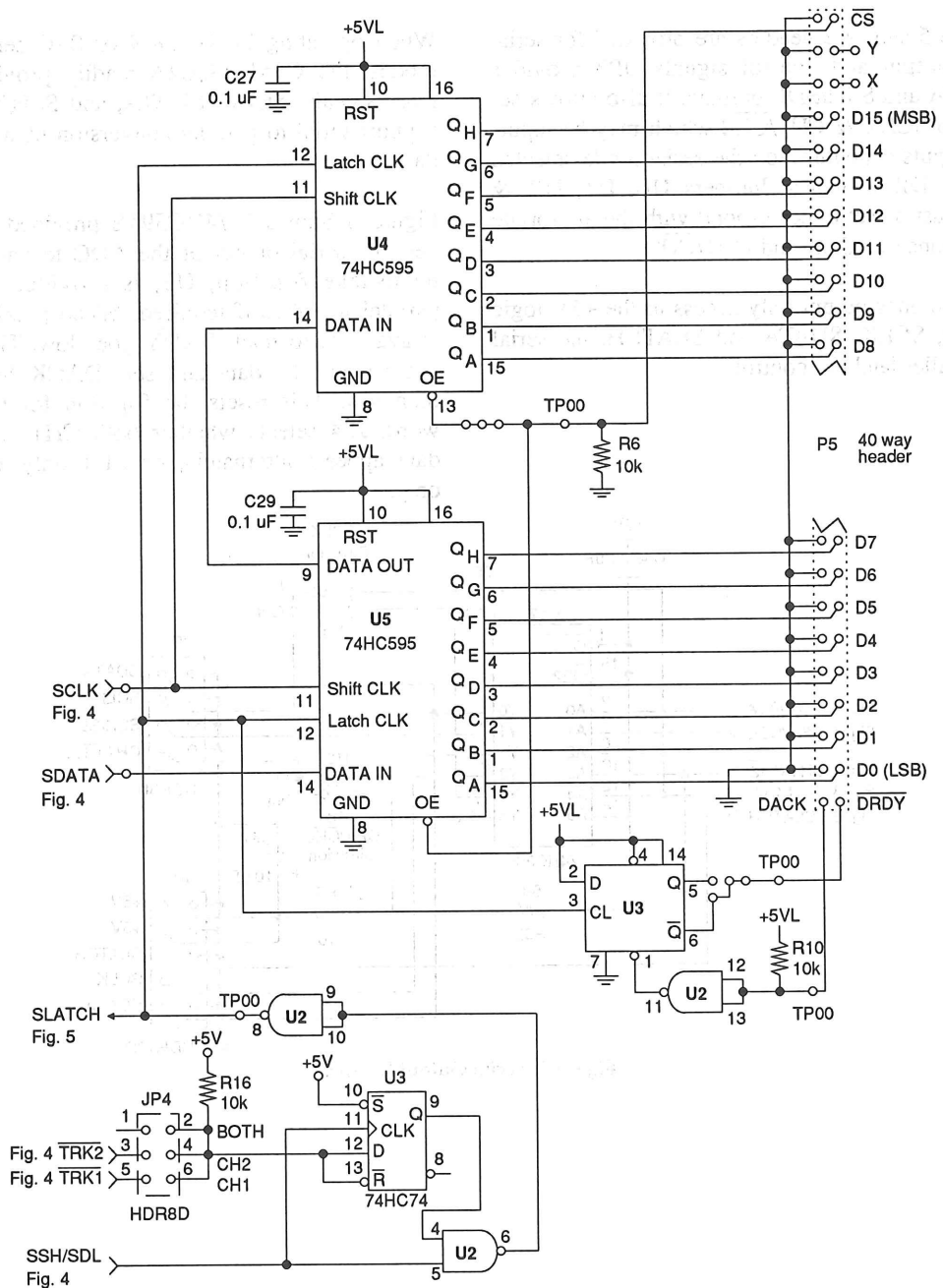


Figure 6. Serial to Parallel Converter

			OPEN	CLOSE
			2's Complement	Binary
<div> <div>OPEN</div> <div> <div>1</div> <div>0</div> </div> <div>2</div> <div>3</div> <div>4</div> <div>5</div> <div>6</div> </div>	CODE			
	BP/UP		Bipolar	Unipolar
	SCKMOD		Selects Serial Port	
	OUTMOD		Mode. See Table 2.	
	SLEEP		Normal Mode	Sleep Mode
	CH1/CH2*		AIN1	AIN2

\*SW6 is not active when the converter is operating in the FRN mode.

**Table 1. DIP Switch Selections**

SCKMOD (SW3)	OUTMOD (SW4)	CS5101A/CS5102A Output Mode
CLOSE	CLOSE	(FRN) Free Run
CLOSE	OPEN	(SSC) Synchronous Self Clocking
OPEN	CLOSE	(RBT) Registered Burst Transmission
OPEN	OPEN	(PDT) Pipelined Data Transmission

**Table 2. Output Mode Selections**

### DIP Switches

Tables 1 and 2 show the DIP switch settings.

### Miscellaneous Hints on Using the Evaluation Board

Always depress the reset button after powering up the board. The CS5101A & CS5102A are self calibrating ADC's which require a reset to initiate the internal calibration procedure.

Crystal Semiconductor has software, available on request, which allows the evaluation board to be connected to a Metrabyte PIO12 parallel I/O card (which uses an Intel 8255 PIO chip), which is plugged into an IBM PC or compatible computer. The software is assembly language drivers to read the data from the board. Also included is source code, in Fortran, of an FFT routine.

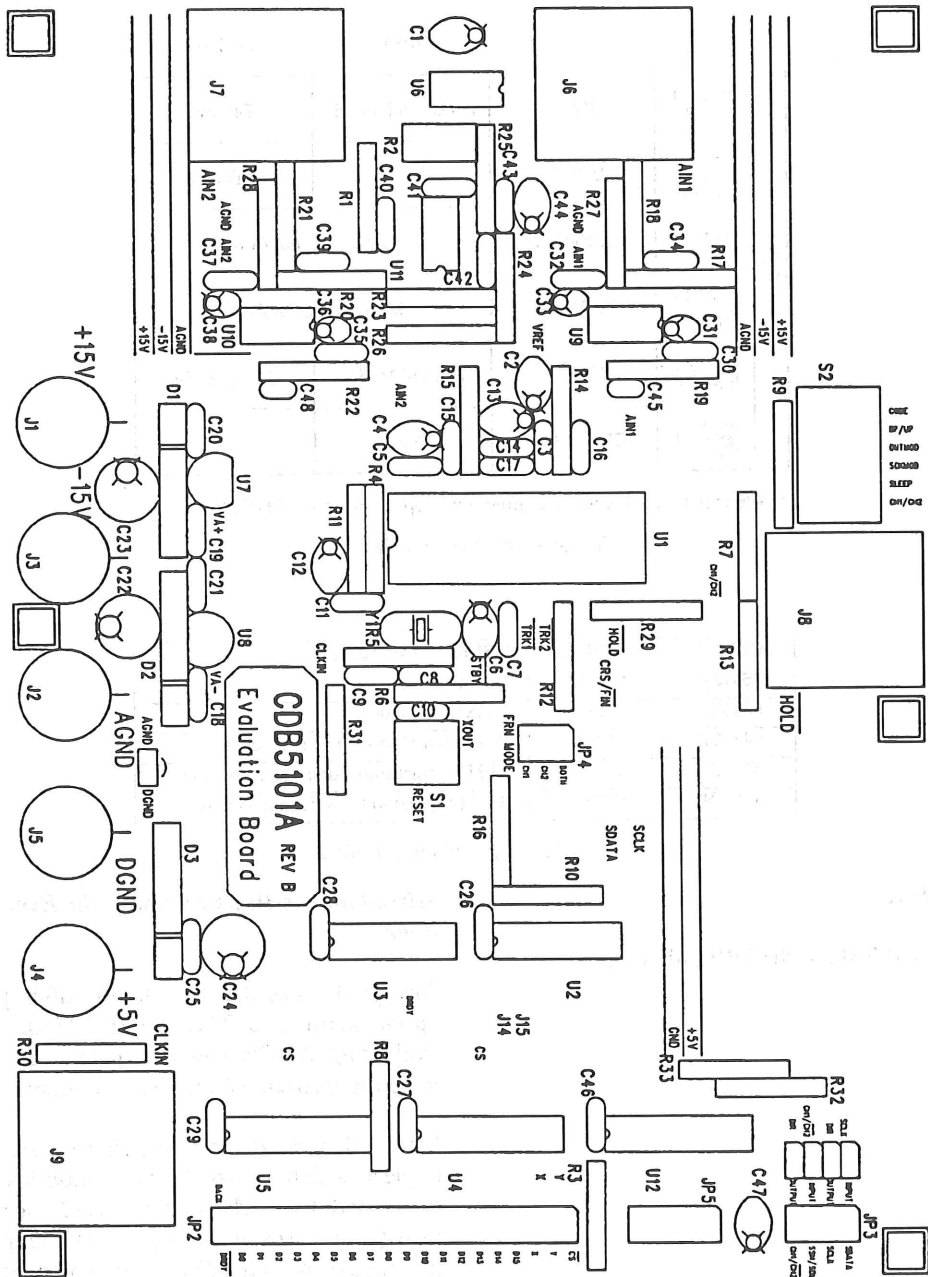
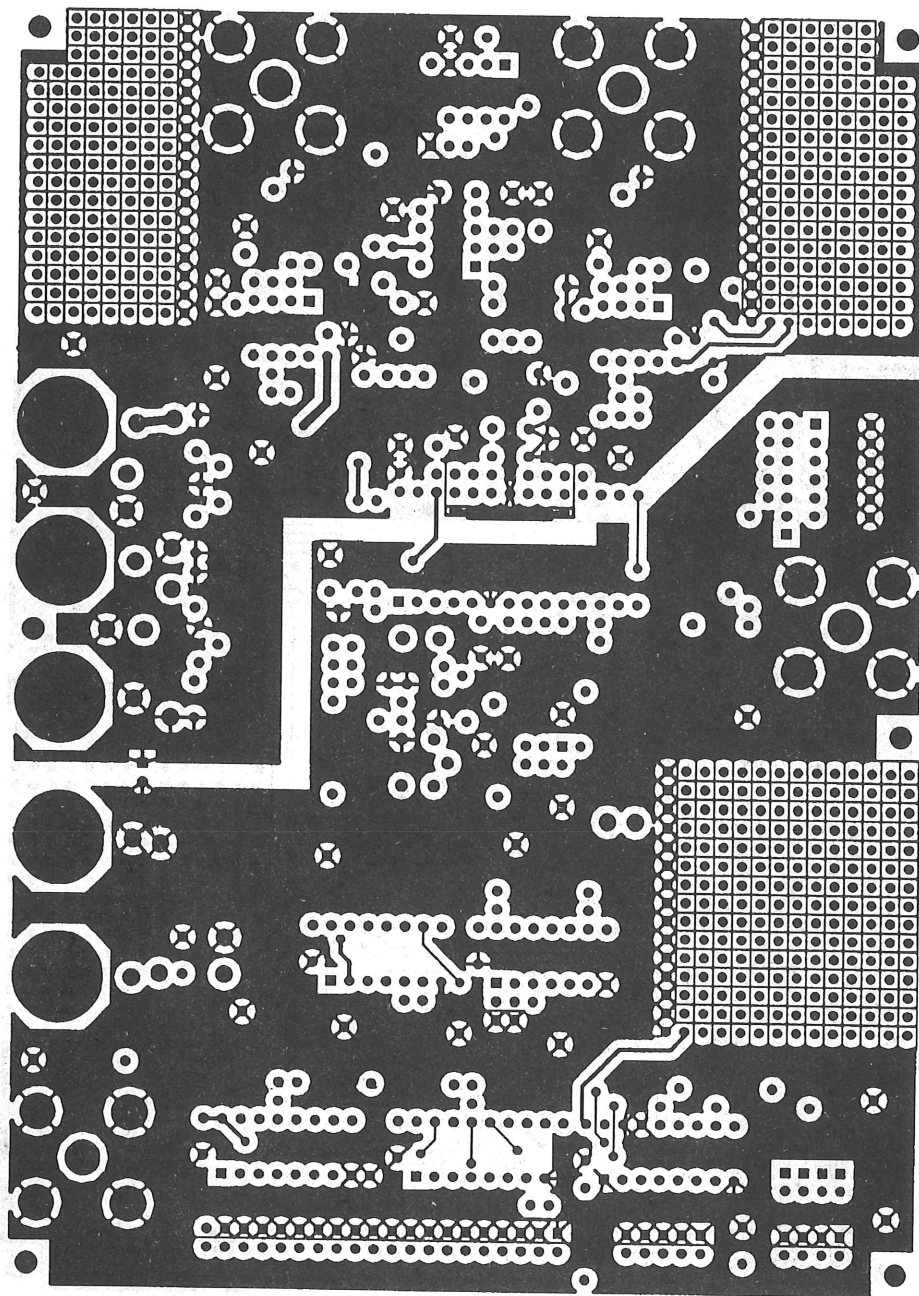


Figure 7. CDB5101A/02A Rev. B Layout



3

Figure 8. CDB5101A/02A Rev. B Component Side



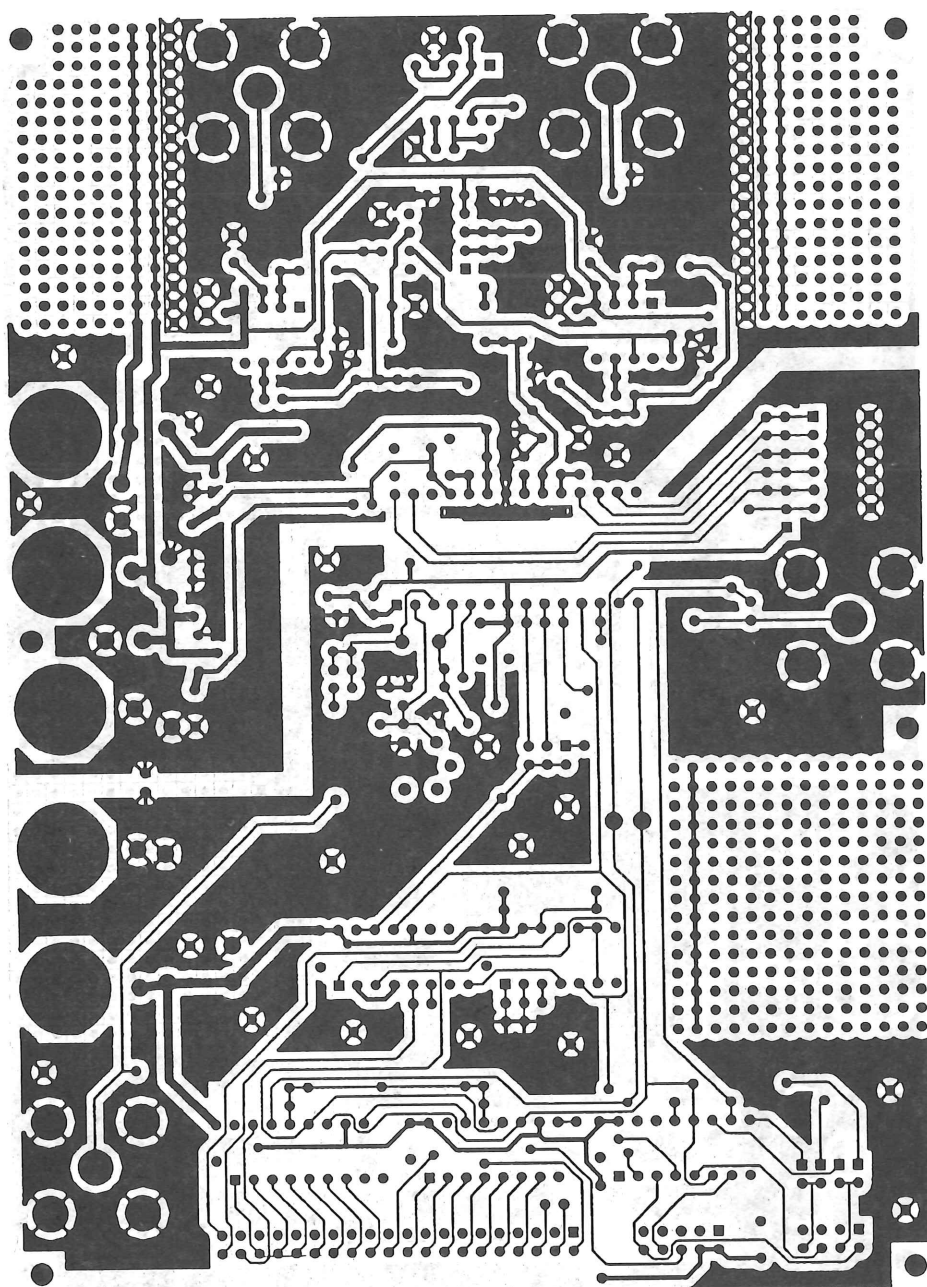


Figure 9. CDB5101A/02A Rev. B Solder Side

# 16-Bit, 20 kHz Oversampling A/D Converter

## Features

- Complete Voiceband DSP Front-End  
16-Bit A/D Converter  
Internal Track & Hold Amplifier  
On-Chip Voltage Reference  
Linear-Phase Digital Filter
- On-Chip PLL for Simplified Output  
Phase Locking in Modem Applications
- 84 dB Dynamic Range
- 80 dB Total Harmonic Distortion
- Output Word Rates up to 20 kHz
- DSP-Compatible Serial Interface
- Low Power Dissipation: 220 mW

## General Description

The CS5317 is an ideal analog front-end for voiceband signal processing applications such as high-performance modems, passive sonar, and voice recognition systems. It includes a 16-bit A/D converter with an internal track & hold amplifier, a voltage reference, and a linear-phase digital filter.

An on-chip phase-lock loop (PLL) circuit simplifies the CS5317's use in applications where the output word rate must be locked to an external sampling signal.

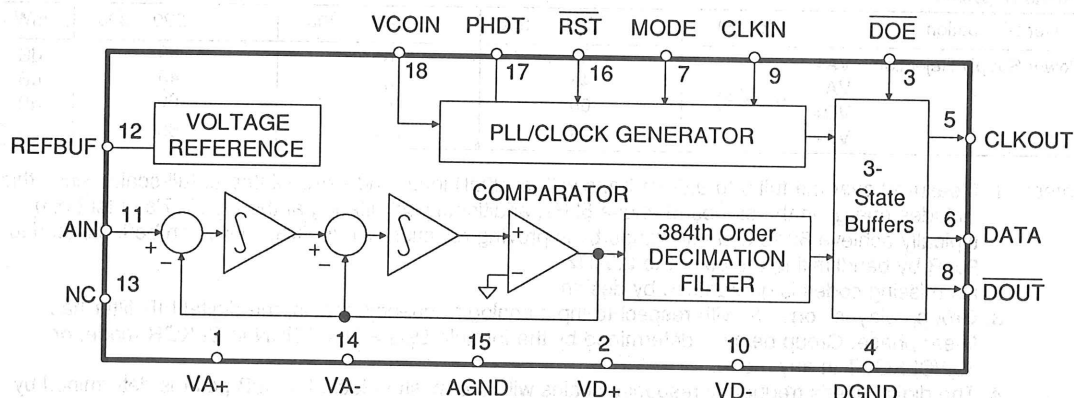
The CS5317 uses delta-sigma modulation to achieve 16-bit output word rates up to 20 kHz. The delta-sigma technique utilizes oversampling followed by a digital filtering and decimation process. The combination of oversampling and digital filtering greatly eases antialias requirements. Thus, the CS5317 offers 84 dB dynamic range and 80 dB THD and signal bandwidths up to 10 kHz at a fraction of the cost of hybrid and discrete solutions.

The CS5317's advanced CMOS construction provides low power consumption of 220 mW and the inherent reliability of monolithic devices.

**ORDERING INFORMATION:** Page 3-125

3

## Block Diagram



**ANALOG CHARACTERISTICS** ( $T_A = T_{MIN} - T_{MAX}$ ;  $V_{A+}, V_{D+} = 5V \pm 10\%$ ;  $V_{A-}, V_{D-} = -5V \pm 10\%$ ; CLKIN = 4.9152 MHz in CLKOR mode; 1kHz Input Sinewave; with 1.2 k $\Omega$ , .01  $\mu$ F antialiasing filter.)

Parameter*	CS5317-K			CS5317-B			CS5317-T			Units
	min	typ	max	min	typ	max	min	typ	max	
Specified Temperature Range	0 to 70			- 40 to + 85			- 55 to + 125			°C
Resolution	16			16			16			Bits
Dynamic Performance										
Dynamic Range (Note 1)	78	84		78	84		78	84		dB
Total Harmonic Distortion	72	80		72	80		72	80		dB
Signal to Intermodulation Distortion	84			84			84			dB
dc Accuracy										
Differential Nonlinearity (Note 2)	± 0.4			± 0.4			± 0.4			LSB
Positive Full-Scale Error	± 150			± 150			± 150			mV
Positive Full-Scale Drift	± 500			± 500			± 500			µV/°C
Bipolar Offset Error	± 10			± 10			± 10			mV
Bipolar Offset Drift	± 50			± 50			± 50			µV/°C
Filter Characteristics										
Absolute Group Delay (Note 3)	78.125			78.125			78.125			µs
Passband Frequency (Note 4)	5			5			5			kHz
Input Characteristics										
AC Input Impedance (1kHz)	80			80			80			kohms
Analog Input Full Scale Signal Level	± 2.75			± 2.75			± 2.75			V
Power Supplies										
Power Dissipation (Note 5)	220		300	220		300	220		300	mW
Power Supply Rejection (Note 6)	VA+	60		60		60				dB
	VA-	45		45		45				dB
	VD+	60		60		60				dB
	VD-	55		55		55				dB

- Notes:
1. Measured over the full 0 to 9.6kHz band with a -20dB input and extrapolated to full-scale. Since this includes energy in the stopband above 5kHz, additional post-filtering at the CS5317's output can typically achieve 88dB dynamic range by improving rejection above 5kHz. This can be increased to 90dB by bandlimiting the output to 2.5kHz.
  2. No missing codes is guaranteed by design.
  3. Group delay is constant with respect to input analog frequency; that is, the digital FIR filter has linear phase. Group delay is determined by the formula  $D_{grp} = 384/CLKIN$  in CLKOR mode, or  $192/CLKOUT$  in any mode.
  4. The digital filter's frequency response scales with the master clock. Its -3dB point is determined by  $f_{-3dB} = CLKIN/977.3$  in CLKOR mode, or  $CLKOUT/488.65$  in any mode.
  5. All outputs unloaded. All inputs CMOS levels.
  6. With 300mV p-p, 1kHz ripple applied to each supply separately.

\* Refer to the *Parameter Definitions* section after the Pin Description section.

**ANALOG CHARACTERISTICS** (Continued)

Parameter	CS5317-K			CS5317-B			CS5317-T			Units
	min	typ	max	min	typ	max	min	typ	max	
Specified Temperature Range	0 to 70			- 40 to +85			- 55 to +125			°C
<b>Phase-Lock Loop Characteristics</b>										
VCO Gain Constant, Ko (Note 7)	- 4	- 10	- 30	- 4	- 10	- 30	- 4	- 10	- 30	M rad/Vs
VCO operating frequency	1.28		5.12	1.28		5.12	1.28		5.12	MHz
Phase Detector Gain Control, Kd	- 3	- 8	- 12	- 3	- 8	- 12	- 3	- 8	- 12	uA/rad
Phase Detector Prop. Delay (Note 8)		50	100		50	100		50	100	ns

Notes: 7. Over 1.28 MHz to 5.12 MHz VCO output range, where VCO frequency = 2 \* CLKOUT.

8. Delay from an input edge to the phase detector to a response at the PHDT output pin.

**3**
**DIGITAL CHARACTERISTICS** ( $T_A = T_{MIN} - T_{MAX}$ ;  $V_{A+}, V_{D+} = 5V \pm 10\%$ ;  $V_{A-}, V_{D-} = -5V \pm 10\%$ )  
 All measurements performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	$V_{IH}$	2.0	-	-	V
Low-Level Input Voltage	$V_{IL}$	-	-	0.8	V
High-Level Output Voltage (Note 9)	$V_{OH}$	$V_{D+} - 1.0V$	-	-	V
Low-Level Output Voltage $I_{out} = 1.6mA$	$V_{OL}$	-	-	0.4	V
Input Leakage Current	$I_{in}$	-	-	10	uA
3-State Leakage Current	$I_{OZ}$	-	-	$\pm 10$	uA
Digital Output Pin Capacitance	$C_{out}$	-	9	-	pF

Note: 9.  $I_{out} = -100\mu A$ . This specification guarantees the ability to drive one TTL load ( $V_{OH} = 2.4V$  @  $I_{out} = -40\mu A$ ).

**RECOMMENDED OPERATING CONDITIONS** (DGND, AGND = 0 V, see Note 10.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	4.5	5.0	5.5	V
	Negative Digital	-4.5	-5.0	-5.5	V
	Positive Analog	4.5	5.0	5.5	V
	Negative Analog	-4.5	-5.0	-5.5	V
Master Clock Frequency	$f_{clk}$	0.01	-	5.12	MHz

Note: 10. All voltages with respect to ground.

Specifications are subject to change without notice.

**SWITCHING CHARACTERISTICS** ( $T_A = T_{MIN} - T_{MAX}$ ;  $C_L = 50 \text{ pF}$ ;  $V_{D+} = 5V \pm 10\%$ ;  $V_{D-} = -5V \pm 10\%$ )

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency: CLKIN					
CLKG1 Mode	$f_{clk1}$	-	-	20	kHz
CLKG2 Mode	$f_{clk2}$	-	-	10	kHz
CLKOR Mode	$f_{clkor}$	-	-	5.12	MHz
Output Word Rate: $\overline{DOUT}$	$f_{dout}$	-	-	20	kHz
Rise Times: Any Digital Input	$t_{risein}$	-	20	1000	ns
Any Digital Output	$t_{riseout}$	-	15	20	ns
Fall Times: Any Digital Input	$t_{fallin}$	-	20	1000	ns
Any Digital Output	$t_{fallout}$	-	15	20	ns
CLKIN Duty Cycle					
CLKG1 and CLKG2 Modes	Pulse Width Low	$t_{pwl1}$	200	-	ns
	Pulse Width High	$t_{pwh1}$	200	-	ns
CLKOR Mode	Pulse Width Low	$t_{pwl1}$	45	-	ns
	Pulse Width High	$t_{pwh1}$	45	-	ns
$\overline{RST}$ Pulse Width Low	$t_{pwr}$	400	-	-	ns
Set Up Times:					
$\overline{RST}$ High to CLKIN High	$t_{su1}$	40	-	-	ns
CLKIN High to $\overline{RST}$ High	$t_{su2}$	40	-	-	ns
Propagation Delays:					
$\overline{DOE}$ Falling to Data Valid	$t_{ph1}$	-	-	150	ns
CLKIN Rising to $\overline{DOUT}$ Falling (Note 11)	$t_{ph2}$	-	1	-	CLKOUT cycles
$\overline{DOE}$ Rising to Hi-Z Output	$t_{ph1}$	-	-	80	ns
CLKOUT Rising to $\overline{DOUT}$ Falling	$t_{ph2}$	-	-	60	ns
CLKOUT Rising to $\overline{DOUT}$ Rising	$t_{ph3}$	-	-	60	ns
CLKOUT Rising to Data Valid	$t_{ph4}$	-	-	100	ns
CLKIN Rising to CLKOUT Falling	$t_{ph5}$	-	-	200	ns
CLKIN Rising to CLKOUT Rising (Note 12)	$t_{ph6}$	-	-	200	ns

Notes: 11. CLKIN only pertains to CLKG1 and CLKG2 modes.

12. Only valid in CLKOR mode.

**ABSOLUTE MAXIMUM RATINGS** (DGND, AGND = 0 V, all voltages with respect to ground.)

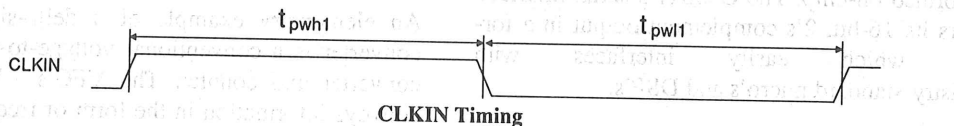
Parameter	Symbol	Min	Max	Units
DC Power Supplies:				
Positive Digital	$V_{D+}$	-0.3	$V_{A+} + 0.3$	V
Negative Digital	$V_{D-}$	0.3	-6.0	V
Positive Analog	$V_{A+}$	-0.3	6.0	V
Negative Analog	$V_{A-}$	0.3	-6.0	V
Input Current, Any Pin Except Supplies (Note 13)	$I_{in}$	-	$\pm 10$	mA
Analog Input Voltage (AIN and VREF pins)	$V_{INA}$	$V_{A-} - 0.3$	$V_{A+} + 0.3$	V
Digital Input Voltage	$V_{IND}$	-0.3	$V_{D+} + 0.3$	V
Ambient Operating Temperature	$T_A$	-55	125	°C
Storage Temperature	$T_{stg}$	-65	150	°C

Note: 13. Transient currents up to 100mA will not cause SCR latch-up.

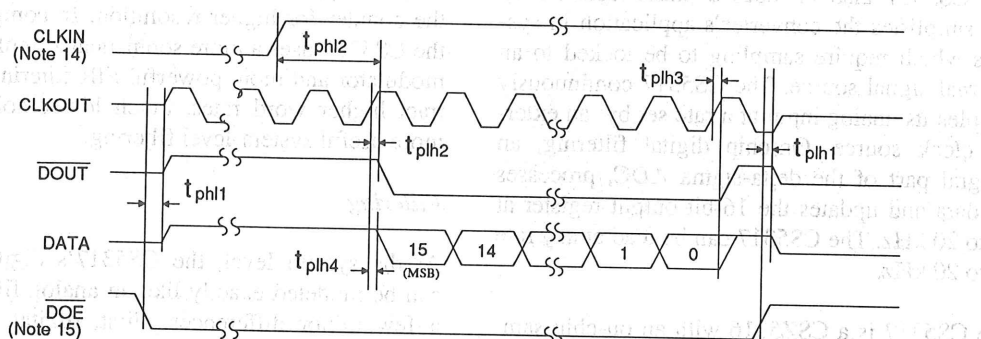
WARNING: Operating this device at or beyond these extremes may result in permanent damage to the device.  
Normal operation of the part is not guaranteed at these extremes.



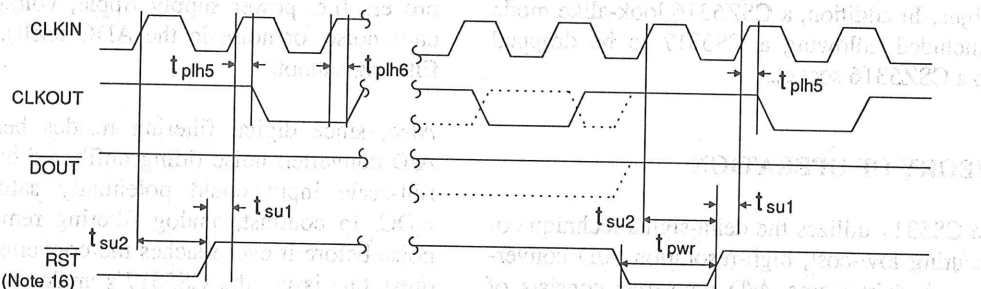
Rise and Fall Times



CLKIN Timing



Serial Output Timing



Reset Timing

- Notes: 14. CLKIN only pertains to CLKG1 and CLKG2 modes.  
 15. If DOE is brought high during serial data transfer, CLKOUT,  $\overline{\text{DOUT}}$ , and DATA will immediately 3-state and the rest of the serial data is lost.  
 16. RST must be held high except in the clock override (CLKOR) mode where it can be used to align the phases of all internal clocks.

## GENERAL DESCRIPTION

The CS5317 functions as a complete data conversion subsystem for voiceband signal processing. The A/D converter, sample/hold, voltage reference, and much of the antialiasing filtering are performed on-chip. The CS5317's serial interface offers its 16-bit, 2's complement output in a format which easily interfaces with industry-standard micro's and DSP's.

The CS5317 also includes a phase-locked loop that simplifies the converter's application in systems which require sampling to be locked to an external signal source. The CS5317 continuously samples its analog input at a rate set by an external clock source. On-chip digital filtering, an integral part of the delta-sigma ADC, processes the data and updates the 16-bit output register at up to 20 kHz. The CS5317 can be read at any rate up to 20 kHz.

The CS5317 is a CSZ5316 with an on-chip sampling clock generator. As such, it replaces the CSZ5316 and should be considered for all new designs. In addition, a CSZ5316 look-alike mode is included, allowing a CS5317 to be dropped into a CSZ5316 socket.

## THEORY OF OPERATION

The CS5317 utilizes the delta-sigma technique of executing low-cost, high-resolution A/D conversions. A delta-sigma A/D converter consists of two basic blocks: an analog modulator and a digital filter.

### *Conversion*

The analog modulator consists of a 1-bit A/D converter (that is, a comparator) embedded in an analog negative feedback loop with high open-loop gain. The modulator samples and converts the analog input at a rate well above the bandwidth of interest (2.5 MHz for the CS5317).

The modulator's 1-bit output conveys information in the form of duty cycle. The digital filter then processes the 1-bit signal and extracts a high resolution output at a much lower rate (that is, 16-bits at a 20 kHz word rate with a 5 kHz input bandwidth).

An elementary example of a delta-sigma A/D converter is a conventional voltage-to-frequency converter and counter. The VFC's 1-bit output conveys information in the form of frequency (or duty-cycle), which is then filtered (averaged) by the counter for higher resolution. In comparison, the CS5317 uses a more sophisticated multi-order modulator and more powerful FIR filtering to extract higher word rates, much lower noise, and more useful system-level filtering.

### *Filtering*

At the system level, the CS5317's digital filter can be modeled exactly like an analog filter with a few minor differences. First, digital filtering resides *behind* the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself). Analog filtering cannot.

Also, since digital filtering resides behind the A/D converter, noise riding unfiltered on a near-full-scale input could potentially saturate the ADC. In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS5317's analog modulator and digital filter reserve headroom such that the device can process signals with 100mV "excursions" above full-scale and still output accurately converted and filtered data. Filtered input signals above full-scale still result in an output of all ones.

An Application Note called "Delta Sigma Overview" contains more details on delta-sigma conversion and digital filtering.



# SYSTEM DESIGN WITH THE CS5317

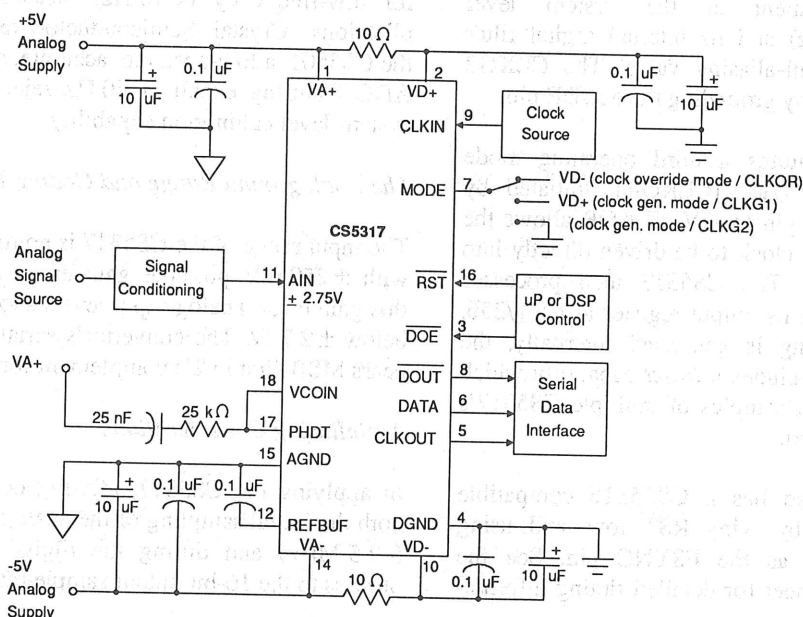
Like a tracking ADC, the CS5317 continuously samples and converts, always tracking the analog input signal and updating its output register at a 20 kHz rate. The device can be read at any rate to create any system-level sampling rate desired up to 20kHz.

## Clocking

Oversampling is a critical function in delta-sigma A/D conversion. Although system-level *output* sample rates typically remain between 7kHz and 20kHz in voiceband applications, the CS5317 actually samples and converts the analog input at rates up to 2.56 MHz. This *internal* sampling rate is typically set by a master clock which is on the order of several megahertz. See Table 1 for a complete description of the clock relationships in the various CS5317 operating modes.

Some systems such as echo-cancelling modems, though, require the *output* sampling rate to be locked to a sampling signal which is 20 kHz or below. For this reason the CS5317 includes an on-chip phase-lock loop (PLL) which can generate its requisite 5.12 MHz master clock from a 20 kHz sampling signal.

The CS5317 features two modes of operation which utilize the internal PLL. The first, termed *Clock Generation 1* (CLKG1), accepts a sampling clock up to 20 kHz at the CLKIN pin and internally generates the requisite 5.12 MHz clock. The CS5317 then processes samples updating its output register at the rate defined at CLKIN, typically 20 kHz. For a 20 kHz clock input the digital filter's 3 dB corner is set at 5.239 kHz, so *CLKG1 provides a factor of 2X oversampling at the system level* (20 kHz is twice the minimum possible sampling frequency needed to reconstruct a 5 kHz input). The CLKG1 mode is initiated by tying the MODE input to +5V.



**Figure 1. System Connection Diagram with Example PLL Components**

Mode	Symbol	Mode Pin	RESET	Output Word Rate Provides System-level 2X Oversampling?	CLKIN (kHz)	CLKOUT $f_{sin}$ (MHz)	DOUT $f_{sout}$ (kHz)	F (kHz)	$t_{dcD}^*$ (ns)
Clock Gen. 2	CLKG2 CLKG2 CLKG2	0 V	HIGH	NO	7.2 9.6 10.0 (max)	1.8432 2.4576 2.56	7.2 9.6 10.0	14.4 19.2 20.0	542.5 406.9 390.6
Clock Gen. 1	CLKG1 CLKG1 CLKG1	+5 V	HIGH	YES	14.4 19.2 20.0 (max)	1.8432 2.4576 2.56	14.4 19.2 20.0	14.4 19.2 20.0	542.5 406.9 390.6
Clock Override	CLKOR CLKOR CLKOR	-5 V	SYNC	YES	3686.4 4915.2 5120.0 (max)	1.8432 2.4576 2.56	14.4 19.2 20.0	14.4 19.2 20.0	N/A N/A N/A
CSZ5316	CSZ5316	FSYNC	LOW	YES	5120.0 (max)	2.56	20.0	20.0	N/A

\*  $t_{dcD}$  - Delay from CLKIN rising to DOUT falling = 1 CLKOUT cycle

**Table 1. Mode Comparisons**

The second PLL mode is termed *Clock Generation 2* (CLKG2) which generates its 5.12 MHz clock from a 10 kHz external sampling signal. Again, output samples are available at the system sampling rate set by CLKIN, typically 10 kHz. For the full-rated 10 kHz clock CLKG2 still sets the filter's 3 dB point at 5 kHz. Therefore, CLKG2 provides no oversampling beyond the Nyquist requirement at the system level (10 kHz : 5 kHz) and its internal digital filter provides little anti-aliasing value. The CLKG2 mode is initiated by grounding the MODE pin.

The CS5317 features a third operating mode called *Clock Override* (CLKOR). Initiated by tying the MODE pin to -5V, CLKOR allows the 5.12 MHz master clock to be driven directly into the CLKIN pin. The CS5317 then processes samples updating its output register at  $f_{clk}/256$ . Since all clocking is generated internally, the CLKOR mode includes a *Reset* capability which allows the output samples of multiple CS5317's to be synchronized.

The CS5317 also has a CSZ5316 compatible mode, selected by tying  $\overline{RST}$  low, and using MODE (pin 7) as the FSYNC pin. See the CSZ5316 data sheet for detailed timing information.

## Analog Design Considerations

### DC Characteristics

The CS5317 was designed for signal processing. Its analog modulator uses CMOS amplifiers resulting in offset and gain errors which drift over temperature. If the CS5317 is being considered for low-frequency (< 10 Hz) measurement applications, Crystal Semiconductor recommends the CS5501, a low-cost, d.c. accurate, delta-sigma ADC featuring excellent 60 Hz rejection and a system-level calibration capability.

### The Analog Input Range and Coding Format

The input range of the CS5317 is nominally  $\pm 3V$ , with  $\pm 250$  mV possible gain error. Because of this gain error, analog input levels should be kept below  $\pm 2.75V$ . The converter's serial output appears MSB-first in 2's complement format.

### Antialiasing Considerations

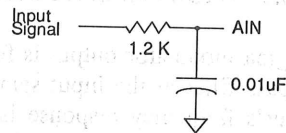
In applying the CS5317, aliasing occurs during both the initial sampling of the analog input at  $f_{sin}$  (~2.5 MHz) and during the digital decimation process to the 16-bit output sample rate,  $f_{sout}$ .

### Initial Sampling

The CS5317 samples the analog input, AIN, at one-half the master clock frequency (~2.5 MHz max). The input sampling frequency,  $f_{\text{sin}}$ , appears at CLKOUT regardless of whether the master clock is generated on-chip (CLKG1 and CLKG2 modes) or driven directly into the CS5317 (CLKOR mode). The digital filter then processes the input signal at the input sample rate.

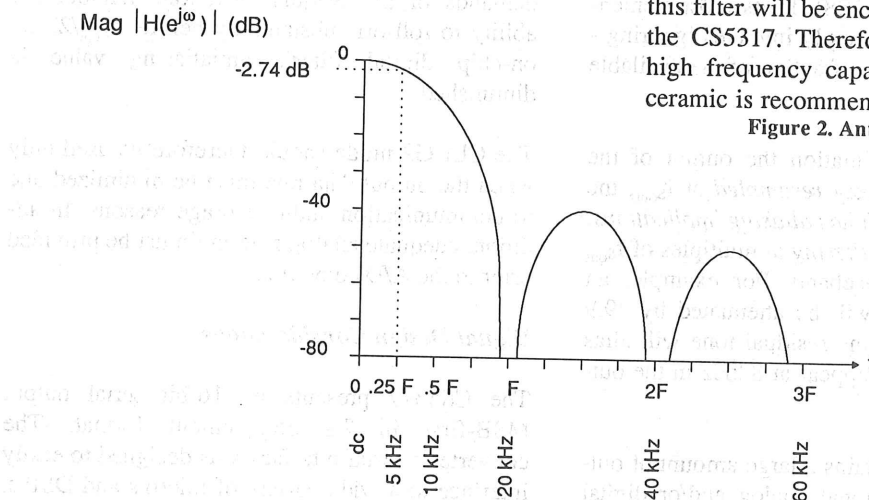
Like any sampled-data filter, though, the digital filter's passband spectrum repeats around integer multiples of the sample rate,  $f_{\text{sin}}$ . That is, when

the CS5317 is operating at its full-rated speed any noise within  $\pm 5$  kHz bands around 2.5 MHz, 5 MHz, 7.5 MHz, etc. will pass unfiltered and alias into the baseband. Such noise can only be filtered by analog filtering *before the signal is sampled*. Since the signal is heavily oversampled (2.5 MHz : 5 kHz, or 500 : 1), a single-pole passive RC filter can be used as shown in Figure 2.



Note: Any nonlinearities contributed by this filter will be encoded as distortion by the CS5317. Therefore a low distortion, high frequency capacitor such as NPO-ceramic is recommended.

Figure 2. Anti-alias Filter



$$\left| \left( \frac{\sin(128\pi fT)}{128\sin(\pi fT)} \right)^3 \right| = \text{Magnitude where: } T = 1/f_{\text{sin}}$$

$f_{\text{sin}}$  = input sampling frequency = CLKOUT frequency for all modes  
 = CLKIN/2 in CLKOR mode  
 = CLKIN\*128 in CLKG1 mode  
 = CLKIN\*256 in CLKG2 mode

$F = f_{\text{sin}}/128$  for all modes

$f$  = input frequency

$f_{\text{sout}} = f_{\text{sin}}/128$  = output data rate for CLKOR & CLKG1 =  $F$

$f_{\text{sout}} = f_{\text{sin}}/256$  = output data rate for CLKG2 =  $F/2$

Examples:

For  $f_{\text{sin}} = 2.56$  MHz at  $f = 5$  kHz: Magnitude is -2.74 dB

For  $f_{\text{sin}} = 2.56$  MHz at  $f = 10$  kHz: Magnitude is -11.8 dB

Figure 3. CS5317 Low-Pass Filter Response

## Decimation

Aliasing effects due to decimation are identical in the CLKOR and CLKG1 modes. Aliasing is different in the CLKG2 mode due to the difference in output sample rates (10 kHz vs. 20 kHz) and thus will be discussed separately.

### Aliasing in the CLKOR and CLKG1 Modes

The delta-sigma modulator output is fed into the digital low-pass filter at the input sampling rate,  $f_{s_{in}}$ . The filter's frequency response is shown in Figure 3. In the process of filtering the digitized signal the filter *decimates* the sampling rate by 128 (that is,  $f_{s_{out}} = f_{s_{in}}/128$ ). In its most elementary form, decimation simply involves ignoring - or selectively reading - a fraction of the available samples.

In the process of decimation the output of the digital filter is effectively *resampled* at  $f_{s_{out}}$ , the output word rate, *which has aliasing implications*. Residual signals *after filtering* at multiples of  $f_{s_{out}}$  will alias into the baseband. For example, an input tone at 28 kHz will be attenuated by 39.9 dB. If  $f_{s_{out}} = 20$  kHz, the residual tone will alias into the baseband and appear at 8 kHz in the output spectrum.

If the input signal contains a large amount of out-of-band energy, additional analog and/or digital antialias filtering may be required. If digital post-filtering is used to augment the CS5317's rejection above  $f_{s_{out}}/4$  (that is, above 5 kHz), the filtering will also reject residual quantization

noise from the modulator (see Appendix A). This will typically increase the converter's dynamic range to 88 dB. Further bandlimiting the digital output to  $f_{s_{out}}/8$  (2.5 kHz at full speed) will typically increase dynamic range to 90 dB.

### Aliasing in the CLKG2 Mode

Aliasing effects in the CLKG2 mode can be modeled exactly as those in the CLKG1 mode with the output decimated by two (from 20 kHz to 10 kHz). This is most easily achieved by ignoring every other sample. In the CLKG2 mode the ratio of the output sampling rate to the filter's -3 dB point is two, with no oversampling beyond the demands of the Nyquist criterion. Without the ability to roll-off substantially before  $f_{s_{out}}/2$ , the on-chip digital filter's antialiasing value is diminished.

The CLKG2 mode should therefore be used only when the output data rate must be minimized due to communication and/or storage reasons. In addition, adequate analog filtering must be provided prior to the A/D converter.

### Digital Design Considerations

The CS5317 presents its 16-bit serial output MSB-first in 2's complement format. The converter's serial interface was designed to easily interface to a wide variety of micro's and DSP's. Appendix A offers several hardware interfaces to industry-standard processors.

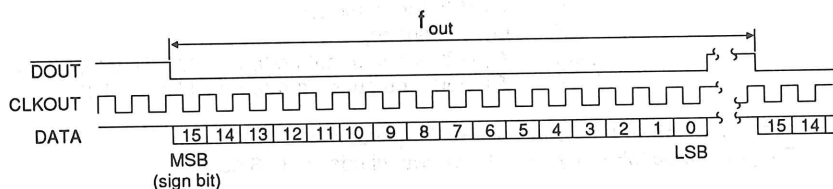


Figure 4. Data Output

### Data Output Characteristics & Coding Format

As shown in Figure 4, the CS5317 outputs its 16-bit data word in a serial burst. The data appears at the DATA pin on the rising edge of the same CLKOUT cycle in which DOUT falls. Data changes on the rising edge of CLKOUT, and can be latched on the falling edge. The CLKOUT rate is set by the CLKIN input ( $f_{clk}/2$  in the CLKOR mode;  $f_{clk} \cdot 128$  in the CLKG1 mode; and  $f_{clk} \cdot 256$  in the CLKG2 mode). DOUT returns high after the last bit is transmitted. After transmitting the sixteen data bits, DATA will remain high until DOUT falls again, initiating the next data output cycle.

A 3-state capability is available for bus-oriented applications. The 3-state control input is termed Data Output Enable,  $\overline{DOE}$ , and is asynchronous with respect to the rest of the CS5317. If  $\overline{DOE}$  is taken high at any time, even during a data burst, the DATA,  $\overline{DOUT}$  and CLKOUT pins go to a high impedance state. Any data which would be output while DOE is high is lost.

### Power Supplies

Since the A/D converter's output is digitally filtered in the CS5317, the device is more forgiving and requires less attention than conventional 16-bit A/D converters to grounding and layout arrangements. Still, care must be taken at the design and layout stages to apply the device properly. The CS5317 provides separate analog and digital power supply connections to isolate digital noise from its analog circuitry. Each supply pin should be decoupled to its respective ground, AGND or DGND. Decoupling should be accomplished with  $0.1 \mu F$  ceramic capacitors. If significant low frequency noise is present in the supplies,  $10 \mu F$  tantalum capacitors are recommended in parallel with the  $0.1 \mu F$  capacitors.

*The positive digital power supply of the CS5317 must never exceed the positive analog supply by more than a diode drop or the chip could be per-*

*manently damaged.* If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. Figure 1 shows a decoupling scheme which allows the CS5317 to be powered from a single set of  $\pm 5V$  rails. The digital supplies are derived from the analog supplies through  $10 \Omega$  resistors to prevent the analog supply from dropping below the digital supply.

### PLL Characteristics

A phase-locked loop is included on the CS5317 and is used to generate the requisite high frequency A/D sampling clock. A functional diagram of the PLL is shown in Figure 5. The PLL consists of a phase detector, a filter, a VCO (voltage-controlled oscillator), and a counter/divider. The phase detector inputs are CLKIN ( $\theta_1$ ) and a sub-multiple of the VCO output signal ( $\theta_2$ ). The inputs to the phase detector are positive-edge triggered and therefore the duty cycle of the CLKIN signal is not significant. With this type of phase detector, the lock range of the PLL is equal to the capture range and is independent of the low pass filter. The output of the phase detector is input to an external low pass filter. The filter characteristics are used to determine the transient response of the loop. The output voltage from the filter functions as the input control voltage to the VCO. The output of the VCO is then divided in frequency to provide an input to the phase detector. The clock divider ratio is a function of the PLL mode which has been selected.

### Phase Detector Gain ( $K_d$ )

A properly designed and operating phase-locked loop can be described using steady state linear analysis. Once in frequency lock, any phase difference between the two inputs to the phase detector cause a current output from the detector during the phase error. While either the  $+50 \mu A$  or the  $-50 \mu A$  current source may be turned on, the average current flow is:

$$i_{out\ avg} = K_d (\theta_1 - \theta_2) \approx (-50\mu A/2\pi) (\theta_1 - \theta_2)$$

where  $\theta_1$  is the phase of IN1,  $\theta_2$  is the phase of IN2 and  $K_d$  is the phase detector gain. The factor  $2\pi$  comes from averaging the current over a full CLKIN cycle.  $K_d$  is in units of micro-amperes/radian.

### VCO Gain ( $K_o$ )

The output frequency from the VCO ranges from 1.28 MHz to 5.12 MHz. The frequency is a function of the control voltage input to the VCO. The VCO has a negative gain factor, meaning that as the control voltage increases more positively the output frequency decreases. The gain factor units are Megaradians per Volt per Second. This is equivalent to  $2\pi$  Megahertz per volt. Changes in output frequency are given by:

$$\Delta\omega_{VCO} = K_o \Delta V_{COIN} \quad [K_o \text{ is typ. } -10\text{Mrad/Vs.}]$$

### Counter/Divider Ratio

The CS5317 PLL multiplies the CLKIN rate by an integer value. To set the multiplication rate, a counter/divider chain is used to divide the VCO

output frequency to develop a clock whose frequency is compared to the CLKIN frequency in the phase detector. The binary counter/divider ratio sets the ratio of the VCO frequency to the CLKIN frequency. As illustrated in Figure 5, the VCO output is always divided by two to yield the CLKOUT signal which is identical in frequency to the delta-sigma modulator sampling clock. The CLKOUT signal is then further divided by either 128 in the CLKG1 mode or by 256 in the CLKG2 mode. When the divide by two stage is included, the divider ratio ( $N$ ) for the PLL in the CLKG1 mode is effectively 256. In the CLKG2 mode the divider ratio ( $N$ ) is 512.

### Loop Transfer Function

As the phase-locked loop is a closed loop system, an equation can be determined which describes its closed loop response. Using the gain factors for the phase detector and the VCO, the filter arrangement and the counter/divider constant  $N$ , analysis will yield the following equation which describes the transfer function of the PLL:

$$\frac{\theta_2}{\theta_1} = \frac{\frac{K_o K_d R}{N} s + \frac{K_o K_d}{NC}}{s^2 + \frac{K_o K_d R}{N} s + \frac{K_o K_d}{NC}}$$

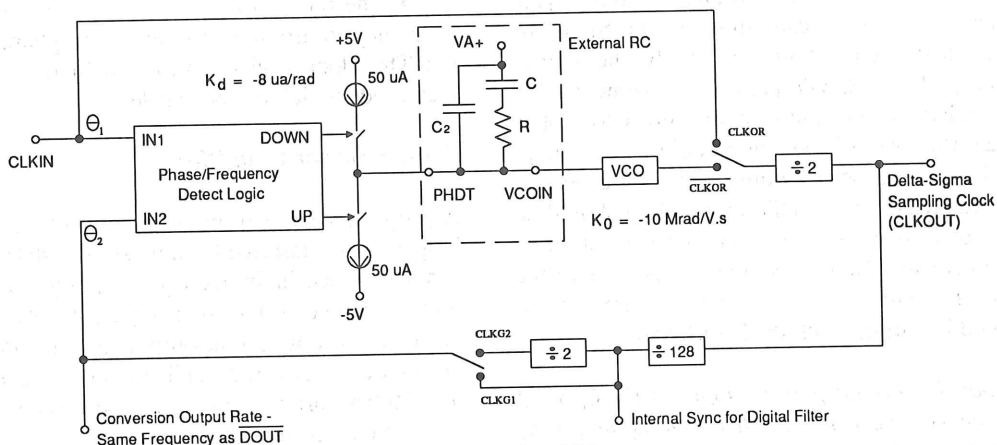


Figure 5. PLL Functional Diagram

This equation may be rewritten such that its elements correspond with the following characteristic form in which the damping factor,  $\zeta$ , and the natural frequency,  $\omega_n$ , are evident:

$$\frac{\theta_2}{\theta_1} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Both the natural frequency and the damping factor are particularly important in determining the transient response of the phase-locked loop when subjected to a step input of phase or frequency. A family of curves are illustrated in Figure 6 that indicate the overshoot and stability of the loop as a function of the damping factor. Each response is plotted as a function of the normalized time,  $\omega_n t$ . For a given  $\zeta$  and lock time,  $t$ , the  $\omega_n$  required can be determined. Alternatively, phase lock control loop bandwidth may be a specified parameter. In some systems it may be desirable to reduce the -3dB bandwidth of the PLL control loop to reduce the effects of jitter in the phase of the input clock. The 3 dB bandwidth of the PLL control loop is defined by the following equation:

$$\omega_{3dB} = \omega_n \sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}}$$

The equations used to describe the PLL and the 3 dB bandwidth are valid only if the frequency of

CLKIN is approximately 20 times greater than the 3 dB corner frequency of the control loop.

## Filter Components

Using the equations which describe the transfer function of the PLL system, the following external filter component equations can be determined:

$$C = \frac{K_o K_d}{N \omega_n^2}$$

$$R = 2\zeta\omega_n \frac{N}{K_o K_d}$$

The gain factors ( $K_o$ ,  $K_d$ ) are specified in the Analog Characteristics table. In the event the system calls for very low bandwidth, hence a corresponding reduction in loop gain, the phase detector gain factor  $K_d$  can be reduced. A large series resistor ( $R_1$ ) can be inserted between the output of the detector and the filter. Then the 50  $\mu$ A current sources will saturate to the supplies and yield the following gain factor:

$$K_d \approx \frac{-5V}{2\pi R_1}$$

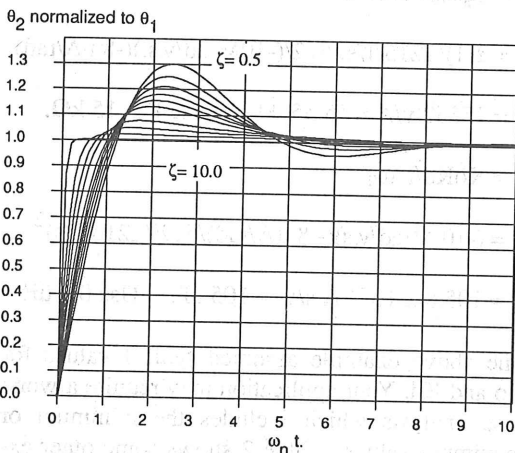


Figure 6A  $\theta_2$  Unit Step Response

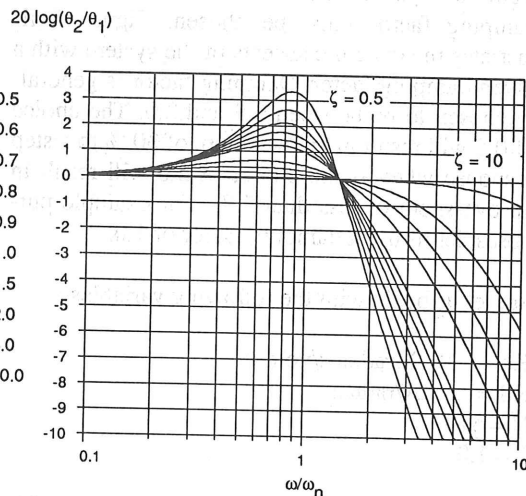


Figure 6B Second Order PLL Frequency Response



In some applications additional filtering may be useful to eliminate any jitter associated with the discrete current pulses from the phase detector. In this case a capacitor whose value is no more than 0.1 C can be placed across the RC filter network (C<sub>2</sub> in Figure 5).

## Filter Design Example

The following is a step by step example of how to derive the loop filter components. The CS5317 A/D sampling clock is to be derived from a 9600 Hz clock source. The application requires the signal passband of the CS5317 to be 4 kHz. The on-chip digital filter of the CS5317 has a 3 dB passband of CLKOUT/488.65 (see Note 4 in the data sheet specifications tables). The 4 kHz passband requirement dictates that the sample clock (CLKOUT) of the CS5317 be a minimum of  $4000 \times 488.65 = 1.954$  MHz. This requires the VCO to run at 3.908 MHz. The 3.908 MHz rate is 407 times greater than the 9600 Hz PLL input clock. Therefore the CS5317 must be set up in mode CLKG2 with N = 512. If the CLKG1 mode were used (N = 256), too narrow of a signal bandwidth through the A/D would result.

Once the operating mode has been determined from the system requirements, a value for the damping factor must be chosen. Figure 6 illustrates the dynamic aspects of the system with a given damping factor. Damping factor is generally chosen to be between 0.5 and 2.0. The choice of 0.5 will result in an overshoot of 30 % to a step response whereas the choice of 2.0 will result in an overshoot of less than 5 %. For example purposes, let us use a damping factor of 1.0.

So, let us begin with the following variables :

$$\begin{aligned} K_o &= -10 \text{ Mradians/volt.sec} \\ K_d &= -8 \text{ } \mu\text{A/radian} \\ N &= 512 \\ \zeta &= 1.0 \end{aligned}$$

To calculate values for the resistor R and capacitor C of the filter, we must first derive a value for  $\omega_n$ . Using the general rule that the sample clock should be at least 20 times higher frequency than the 3dB bandwidth of the PLL control loop:

$$\text{CLKIN} \geq 20 \omega_{3\text{dB}}$$

$$\text{where } \text{CLKIN} = 9600 \text{ Hz} = 2\pi \cdot 9600 \text{ radians/sec.}$$

$$\text{So: } \omega_{3\text{dB}} = 2\pi \cdot 9600/20 = 3016 \text{ radians/sec.}$$

Knowing  $\omega_{3\text{dB}}$  and the damping factor of 1.0, we can calculate the natural frequency,  $\omega_n$ , of the control loop:

$$\omega_n = \omega_{3\text{dB}} / \sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}}$$

$$\omega_n = 3016 / \sqrt{2(1)^2 + 1 + \sqrt{(2(1)^2 + 1)^2 + 1}}$$

$$\omega_n = 1215 \text{ 1/sec}$$

Once the natural frequency,  $\omega_n$ , is determined, values for R and C for the loop filter can be calculated:

$$R = 2\zeta\omega_n N / K_o K_d$$

$$R = 2(1)(1215 \text{ 1/s}) 512 / (-10 \text{ Mrad/v.s.})(-8 \text{ } \mu\text{A/rad})$$

$$R = 15552 \text{ v/A} = 15.55 \text{ k}\Omega. \text{ Use } R = 15 \text{ k}\Omega.$$

$$C = K_o K_d / N \omega_n^2$$

$$C = (-10 \text{ Mrad/v.s.})(-8 \text{ } \mu\text{A/rad}) / 512 (1215 \text{ 1/s})^2$$

$$C = 105.8 \times 10^{-9} \text{ A.s/v} = 105 \text{ nF. Use } 0.1 \text{ } \mu\text{F.}$$

The above example assumed typical values for  $K_o$  and  $K_d$ . Your application may require a worst case analysis which includes the minimum or maximum values. Table 2 shows some other example situations and R and C values.

CLKIN (Hz)	Mode	N	CLKOUT (MHz)	$\zeta$	$\omega_{dB}$	$\omega_n$	R * (k $\Omega$ )	C * (nF)
7200	CLKG2	512	1.8432	1.0	2262	911	11.6	187
9600	CLKG2	512	2.4576	1.0	3016	1215	15.5	106
14400	CLKG1	256	1.8432	1.0	4524	1822	11.6	94
19200	CLKG1	256	2.4576	1.0	6032	2430	15.5	52

\* The values for R and C are as calculated using the described method. Component tolerances have not been allowed for. Notice that Ko and Kd can vary over a wide range, so using tight tolerances for R and C is not justified. Use the nearest conveniently available value.

Table 2 Example PLL Loop Filter R and C values

### CS5317 PERFORMANCE

The CS5317 features 100% tested dynamic performance. The following section is included to illustrate the test method used for the CS5317.

#### FFT Tests and Windowing

The CS5317 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sine wave is applied to the CS5317 and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins". Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5317.

If sampling is not synchronized to the input sinewave it is highly unlikely that the time record will contain an exact integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, removing the discontinuities. The effect of the "window" in the frequency domain is to

convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used to test the CS5317 has a maximum side-lobe level of -92 dB.

Figure 7 shows an FFT plot of a typical CS5317 with a 1 kHz sinewave input generated by an "ultra-pure" sine wave generator and the output multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the

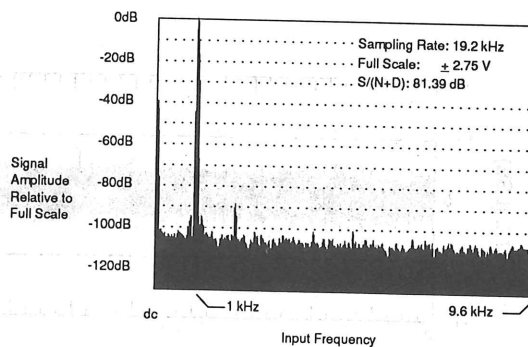


Figure 7. CS5317 Dynamic Performance

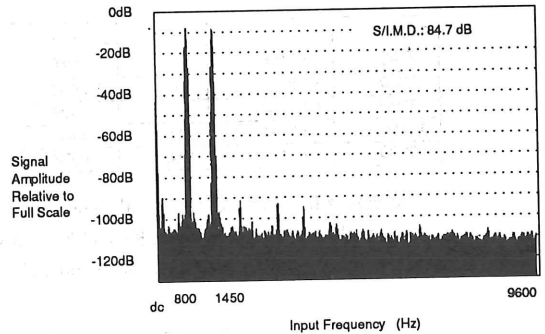
spectral variability that can arise from capturing finite time records, without disturbing the total energy outside the fundamental. All harmonics and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots.

Full - scale signal - to - noise - plus - distortion [S/(N+D)] is calculated as the ratio of the RMS power of the fundamental to the sum of the RMS power of the FFT's other frequency bins, which include both noise and distortion. For the CS5317, signal-to-noise-plus-distortion is shown to be better than 81 dB for an input frequency range of 0 to 9.6 kHz (fs/2).

Harmonic distortion characteristics of the CS5317 are excellent at 80 dB full scale signal to THD (typical), as are intermodulation distortion characteristics, shown in Figure 8. Intermodulation distortion results from the modulation distortion of two or more input frequencies by a non-linear transfer function.

#### *DNL Test*

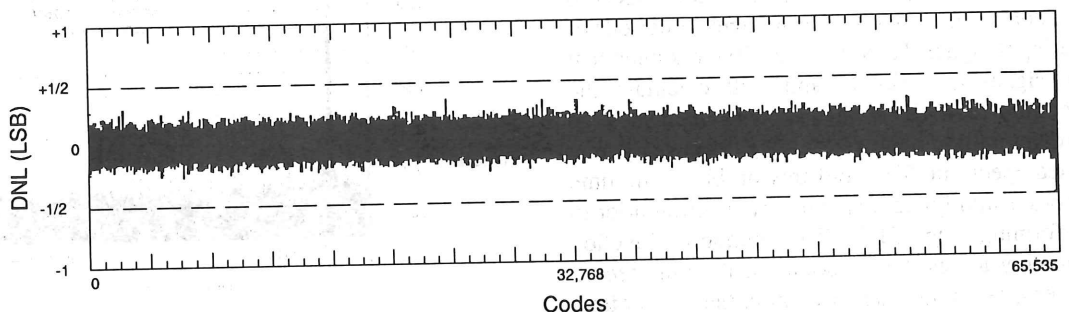
Figure 9 shows a plot of the typical differential non-linearity (DNL) of the CS5317. This test is done by taking a large number of conversion results, and counting the occurrences of each code. A perfect A/D converter would have all codes of equal size and therefore equal numbers



**Figure 8. CS5317 Intermodulation Distortion**

of occurrences. In the DNL test, a code with the average number of occurrences is considered ideal and plotted as DNL = 0 LSB. A code with more or less occurrences than average will appear as a DNL of greater than or less than zero. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

The plot below illustrates the typical DNL performance of the CS5317, and clearly shows the part easily achieves no missing codes.



**Figure 9. CS5317 DNL Plot**

### PIN DESCRIPTIONS (Pin numbers refer to the 18-pin DIP package)

#### 18 pin DIP Pinout

POSITIVE ANALOG POWER	VA+	1	18	VCOIN	VCO INPUT
POSITIVE DIGITAL POWER	VD+	2	17	PHDT	PHASE DETECT
DATA OUTPUT ENABLE	DOE	3	16	RST	RESET
DIGITAL GROUND	DGND	4	15	AGND	ANALOG GROUND
SERIAL CLOCK OUTPUT	CLKOUT	5	14	VA-	NEGATIVE ANALOG POWER
SERIAL DATA OUTPUT	DATA	6	13	NC	NO CONNECT
CLOCKING MODE SELECT	MODE	7	12	REFBUF	POSITIVE REFERENCE BUFFER
DATA OUTPUT READY	DOUT	8	11	AIN	ANALOG INPUT
CLOCK INPUT	CLKIN	9	10	VD-	NEGATIVE DIGITAL POWER

#### 20 pin SOIC pinout

POSITIVE ANALOG POWER	VA+	1	20	VCOIN	VCO INPUT
POSITIVE DIGITAL POWER	VD+	2	19	PHDT	PHASE DETECT
DATA OUTPUT ENABLE	DOE	3	18	RST	RESET
DIGITAL GROUND	DGND	4	17	AGND	ANALOG GROUND
NO CONNECT	NC	5	16	NC	NO CONNECT
SERIAL CLOCK OUTPUT	CLKOUT	6	15	NC	NO CONNECT
SERIAL DATA OUTPUT	DATA	7	14	VA-	NEGATIVE ANALOG POWER
CLOCKING MODE SELECT	MODE	8	13	REFBUF	POSITIVE REFERENCE BUFFER
DATA OUTPUT READY	DOUT	9	12	AIN	ANALOG INPUT
CLOCK INPUT	CLKIN	10	11	VD-	NEGATIVE DIGITAL POWER

#### Power Supplies

##### VD+ - Positive Digital Power, PIN 2.

Positive digital supply voltage. Nominally 5 volts.

##### VD- - Negative Digital Power, PIN 10.

Negative digital supply voltage. Nominally -5 volts.

##### DGND - Digital Ground, PIN 4.

Digital ground reference.

##### VA+ - Positive Analog Power, PIN 1.

Positive analog supply voltage. Nominally 5 volts.

##### VA- - Negative Analog Power, PIN 14.

Negative analog supply voltage. Nominally -5 volts.

##### AGND - Analog Ground, PIN 15.

Analog ground reference.

#### PLL/Clock Generator

##### CLKIN - Clock Input, PIN 9.

Clock input for both clock generation modes and the clock override mode (see MODE).

**MODE - Mode Set, PIN 7.**

Determines the internal clocking mode utilized by the CS5317. Connect to +5V to select CLKG1 mode. Connect to DGND to select CLKG2 mode. Connect to -5V to select CLKOR mode. This pin becomes equivalent to FSYNC in the CSZ5316 compatible mode.

**VCOIN - VCO Input, PIN 18.**

This pin is typically connected to PHDT. A capacitor and resistor in series connected between VA+ and this pin sets the filter response of the on-chip phase locked loop.

**PHDT - Phase Detect, PIN 17.**

This pin is typically connected to VCOIN. A capacitor and resistor in series connected between VA+ and this pin sets the filter response of the on-chip phase locked loop.

**Inputs****AIN - Analog Input, PIN 11.** **$\overline{\text{DOE}}$  - Data Output Enable, PIN 3.**

Three-state control for serial output interface. When low, DATA,  $\overline{\text{DOUT}}$ , and CLKOUT are active. When high, they are in a high impedance state.

 **$\overline{\text{RST}}$  - Sample Clock Reset, PIN 16.**

Sets phase of CLKOUT. Functions only in the clock override mode, CLKOR. Used to synchronize the output samples of multiple CS5317's. Must be kept high in CLKG1 or CLKG2 modes. Also, tying this pin low, with MODE not tied to - 5V, will place the CS5317 into CSZ5316 compatible mode.

**Outputs** **$\overline{\text{DOUT}}$  - Data Output Flag, PIN 8.**

The falling edge indicates the start of serial data output on the DATA pin. The rising edge indicates the end of serial data output.

**DATA - Data Output, PIN 6.**

Serial data output pin. Converted data is clocked out on this pin by the rising edge of CLKOUT. Data is sent MSB first in two's complement format.

**CLKOUT - Data Output Clock, PIN 5.**

Serial data output clock. Data is clocked out on the rising edge of this pin. The falling edge should be used to latch data. Since CLKOUT is a free running clock,  $\overline{\text{DOUT}}$  can be used to indicate valid data.

**REFBUF - Positive Voltage Reference Noise Buffer, PIN 12.**

Used to attenuate noise on the internal positive voltage reference. Must be connected to the analog ground through a 0.1 $\mu$ F ceramic capacitor.

## PARAMETER DEFINITIONS

**Resolution** - The number of different output codes possible. Expressed as N, where  $2^N$  is the number of available output codes.

**Dynamic Range** - The ratio of the largest allowable input signal to the noise floor.

**Total Harmonic Distortion** - The ratio of the rms sum of all harmonics to the rms value of the largest allowable input signal. Units in dB's.

**Signal to Intermodulation Distortion** - The ratio of the rms sum of two input signals to the rms sum of all discernible intermodulation and harmonic distortion products.

**Linearity Error** - The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in %FS.

**Differential Nonlinearity** - The deviation of a code's width from the ideal width. Units in LSB's.

**Positive Full Scale Error** - The deviation of the last code transition from the ideal, (VREF - 3/2 LSB). Units in mV.

**Positive Full Scale Drift** - The drift in effective, positive, full-scale input voltage with temperature.

**Negative Full Scale Error** - The deviation of the first code transition from the ideal, (-VREF + 1/2 LSB). Units in mV.

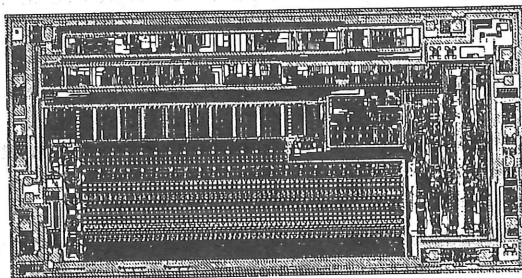
**Negative Full Scale Drift** - The drift in effective, negative, full-scale input voltage with temperature.

**Bipolar Offset** - The deviation of the mid-scale transition from the ideal. The ideal is defined as the middle transition lying on a straight line between actual positive full-scale and actual negative full-scale.

**Bipolar Offset Drift** - The drift in the bipolar offset error with temperature.

**Absolute Group Delay** - The delay through the filter section of the part.

**Passband Frequency** - The upper -3 dB frequency of the CS5317.

**DIE INFORMATION**

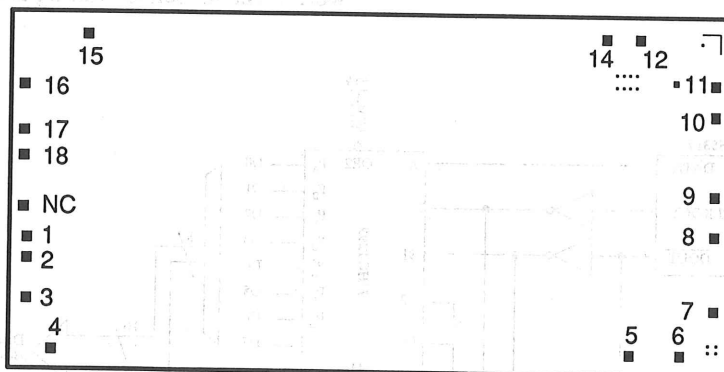
Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

**Assembly Information**

1. Die size shall be 0.135" by 0.269" ( $\pm 0.002$ ").
2. The die is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.
3. Die thickness shall be 0.0175"  $\pm 0.0035$ ". If tighter tolerances are required, contact the factory.
4. The maximum number of die per waffle pack carrier is 28.
5. The cavity dimensions for each die within the waffle pack are 0.180" by 0.330". Exterior waffle pack dimensions are 2.0" by 2.0".
6. The CS5317-YU requires no particular bonding sequence.
7. Each pin of the CS5317 is protected by ESD & latch-up prevention circuitry. Still, proper handling and in circuit application is recommended.
8. Technical constraints limit the viability of accurate performance measurements of precision analog IC's at wafer probe. Although high yield to the limits listed in the specification tables is anticipated, no guarantee is given for unpackaged die product.



### CS5317-YU



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1 -	VA+	10 -	VD-
2 -	VD+	11 -	AIN
3 -	DOE	12 -	REF BUF
4 -	DGND	13 -	NO CONNECT
5 -	CLKOUT	14 -	VA-
6 -	DATA	15 -	AGND
7 -	MODE	16 -	RST
8 -	DOUT	17 -	PHDT
9 -	CLKIN	18 -	VCOIN

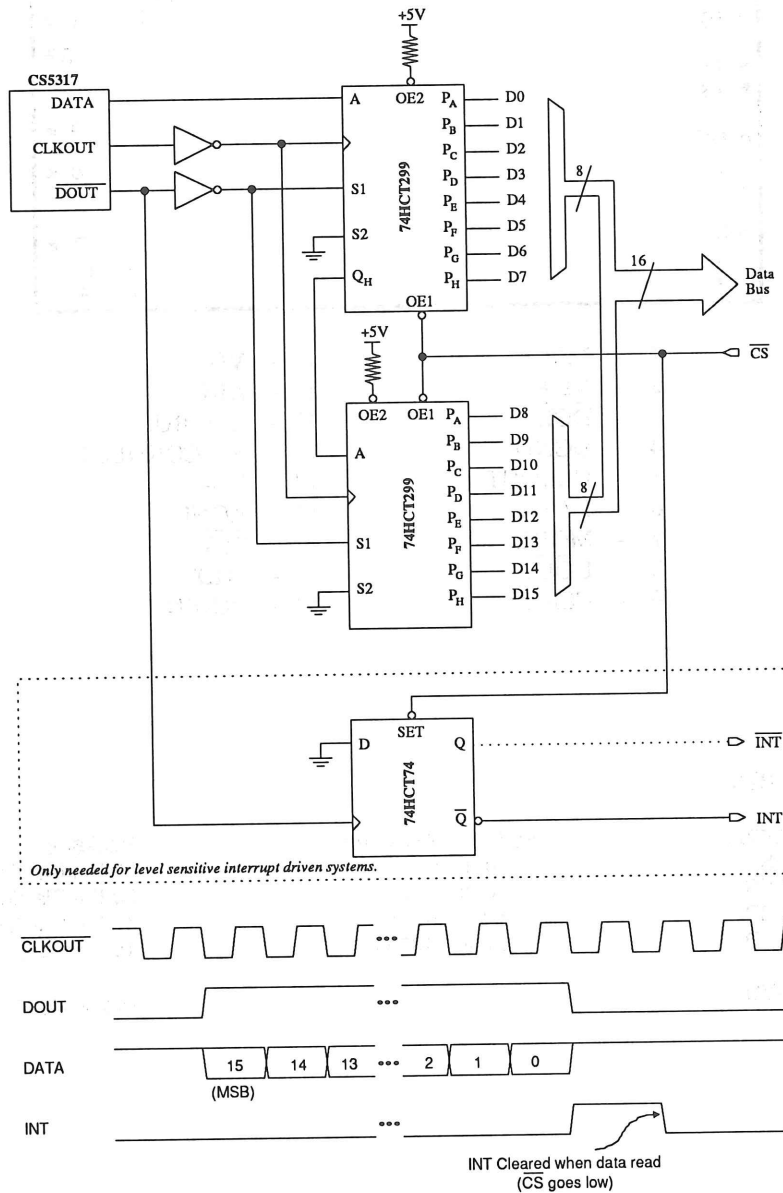
### ORDERING GUIDE

Model Number	Temperature Range	Package
CS5317-KP	0 to 70°C	18 Pin Plastic DIP
CS5317-KS	0 to 70°C	20 Pin Plastic SOIC
CS5317-BD	-40 to +85°C	18 Pin CerDIP
CS5317-TD	-55 to +125°C	18 Pin CerDIP
CS5317-YU		Unpackaged Die

**APPENDIX A**

**APPLICATIONS**

Figure A1 shows one method of converting the serial output of the CS5317 into 16-bit, parallel words. The associated timing is also shown.



**Figure A1. CS5317-to-Parallel Data Bus Interface**

Figure A2 shows the interconnection and timing details for connecting a CS5317 to a NEC  $\mu$ PD7730 DSP chip.

Figure A3 shows the interconnection and timing details for connecting a CS5317 to a Motorola DSP 56000.

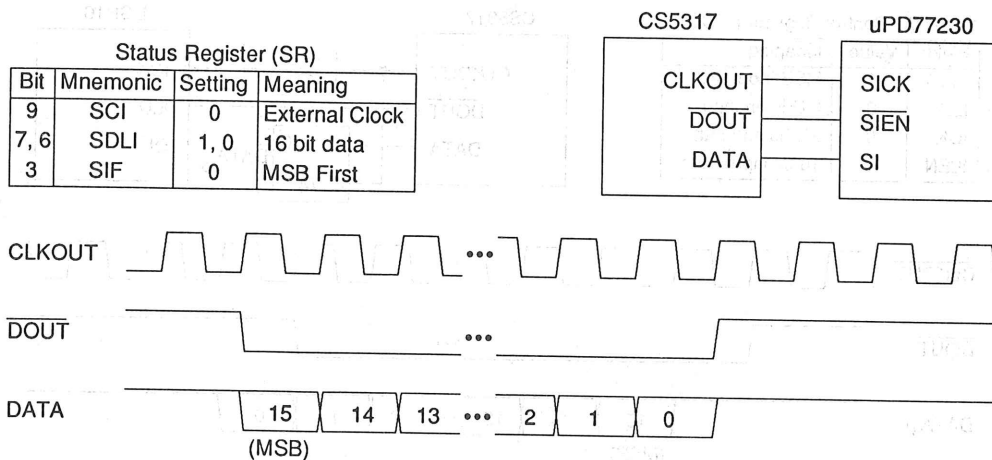


Figure A2. CS5317-to-NEC  $\mu$ PD77230 Serial Interface

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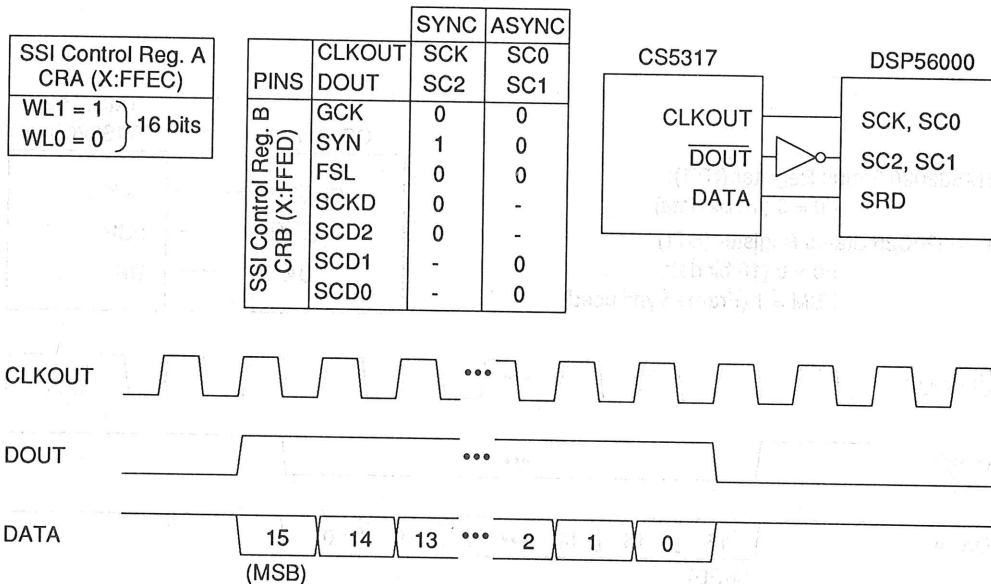
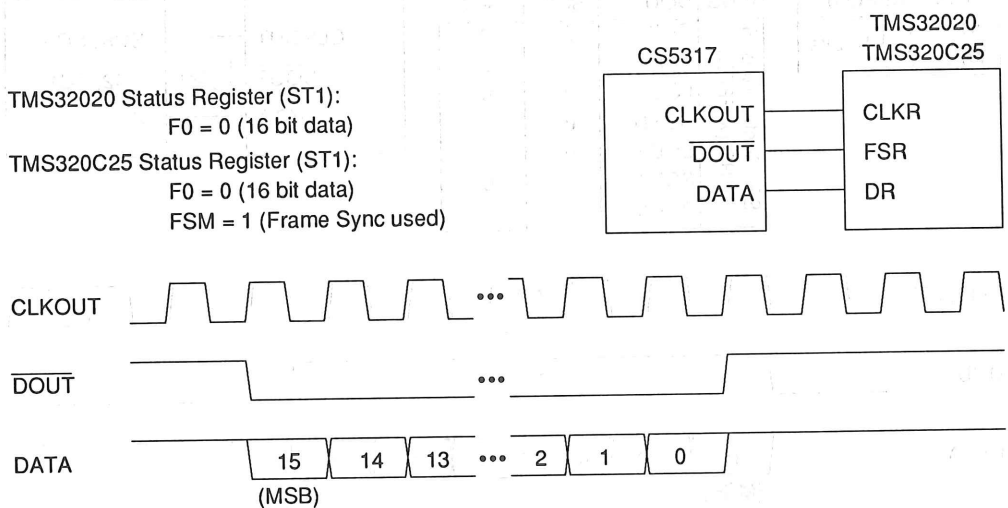
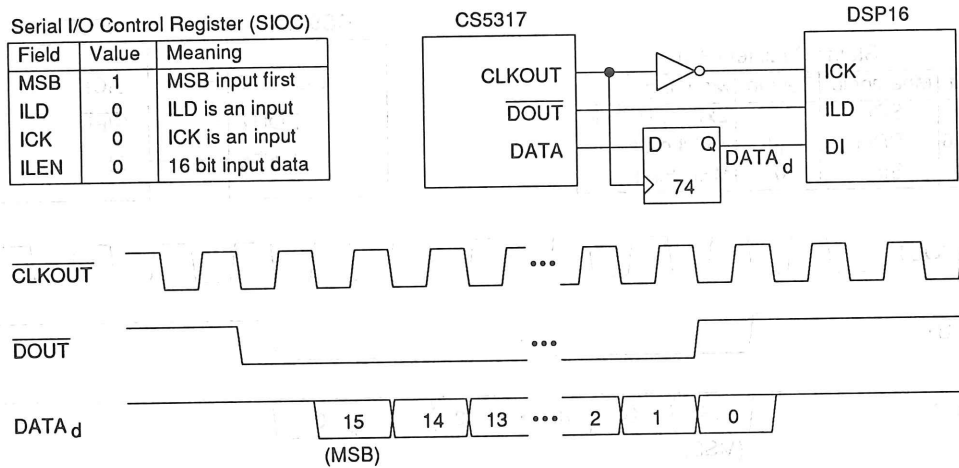


Figure A3. CS5317-to-Motorola DSP56000 Serial Interface

Figure A4 shows the interconnection and timing details for connecting a CS5317 to a WE DSP16 DSP chip.

Figure A5 shows the interconnection and timing details for connecting a CS5317 with TMS32020 and TMS320C25 DSP chips.



## CDB5317 Evaluation Board

## Features

- Easy to Use Digital Interface  
Parallel 16 Bits With Clock  
Serial Output With Clock
- Multiple Operating Modes  
Including Two PLL Modes
- IDC Header used to access Parallel  
Data, Serial Data, and Clock Input and  
Output

## General Description

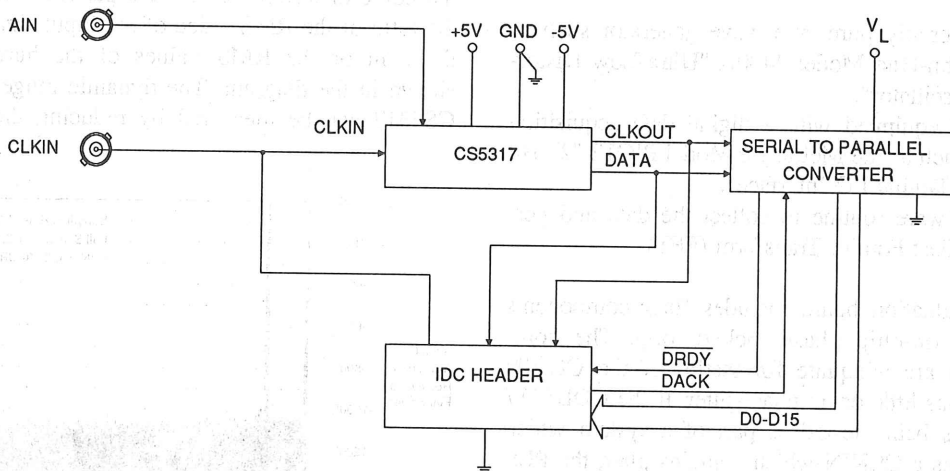
The CDB5317 Evaluation Board is designed to allow the user to quickly evaluate performance of the CS5317 Delta-Sigma Analog-to-Digital Converter. All that is required to use this board is an external power supply, a signal source, a clock source, and an ability to read either serial or parallel 16 bit data words.

**Ordering Information:** CDB5317

CDB5317

3

## Block Diagram



## GENERAL DESCRIPTION

The CDB5317 Evaluation Board is a stand-alone environment for easy lab evaluation of the CS5317 Delta-Sigma Analog-to-Digital Converter. Included on the board is a serial-to-parallel converter. The user can access output data in either parallel or serial form. When supplied with the necessary +5 V and -5 V power supplies, a CLKIN signal, and an analog signal source, the CDB5317 will provide converted data at the 40 pin header.

## SUGGESTED EVALUATION METHOD

An efficient evaluation of the CS5317 using the CDB5317 may be accomplished as described below.

The following equipment will be required for the evaluation:

- The CDB5317 Evaluation Board.
- A power supply capable of supplying +5V and -5V.
- A clock source as the CLKIN signal of the CS5317.
- A spectrally pure sine wave generator such as the Krohn-Hite Model 4400A "Ultra-Low Distortion Oscillator".
- A PC equipped with a digital data acquisition board such as the Metrabyte Model PIO12 "24 Bit Parallel Digital I/O Interface".
- A software routine to collect the data and perform a Fast Fourier Transform (FFT).

The evaluation board includes filter components for the on-chip phase locked loop. The components are adequate for testing if the CLKIN signal has little or no phase-jitter. If the CDB5317 board is being tested as part of a system which generates a CLKIN which contains jitter, the PLL filter components may need to be optimized for your system (see the CS5317 data sheet).

Set-up for evaluation is straightforward. First decide the operating mode and place the jumper on the board for the proper selection. Then decide whether the filter components for the phase locked loop are adequate or whether they should be changed for your evaluation. The PLL will lock on a steady clock input with the filter as it is. Connect the necessary 5 V (CMOS compatible) CLKIN signal for the application. Use the sine-wave generator to supply the analog signal to the CDB5317. Apply the analog input and CLKIN signals only when the evaluation board is powered up. Converted data will then appear at the header on the CDB5317. The header should be connected to the digital data acquisition board in the PC through an IDC 40 pin connector and cable. The software routine should collect the data from the CDB5317 and run a standard 1024 point Fast Fourier Transform (FFT). Such an analysis results in a plot similar to Figure 1. This plot resulted from using a 1kHz input signal and a Blackman-Harris window for the FFT.

The signal to noise and signal to total harmonic distortion characteristics of the CS5317 may be easily measured in this way. The signal to total harmonic distortion value for a particular input is the ratio of the RMS value of the input signal and the sum of the RMS values of the harmonics shown in the diagram. The dynamic range of the CS5317 can be measured by reducing the input

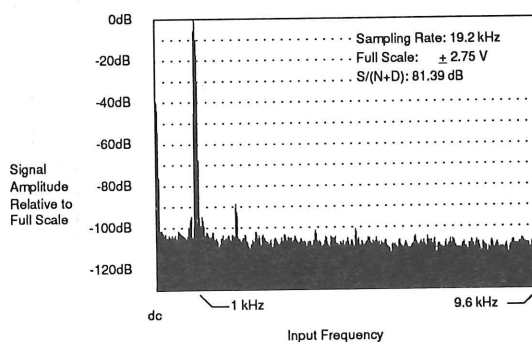


Figure 1. FFT Plot Example

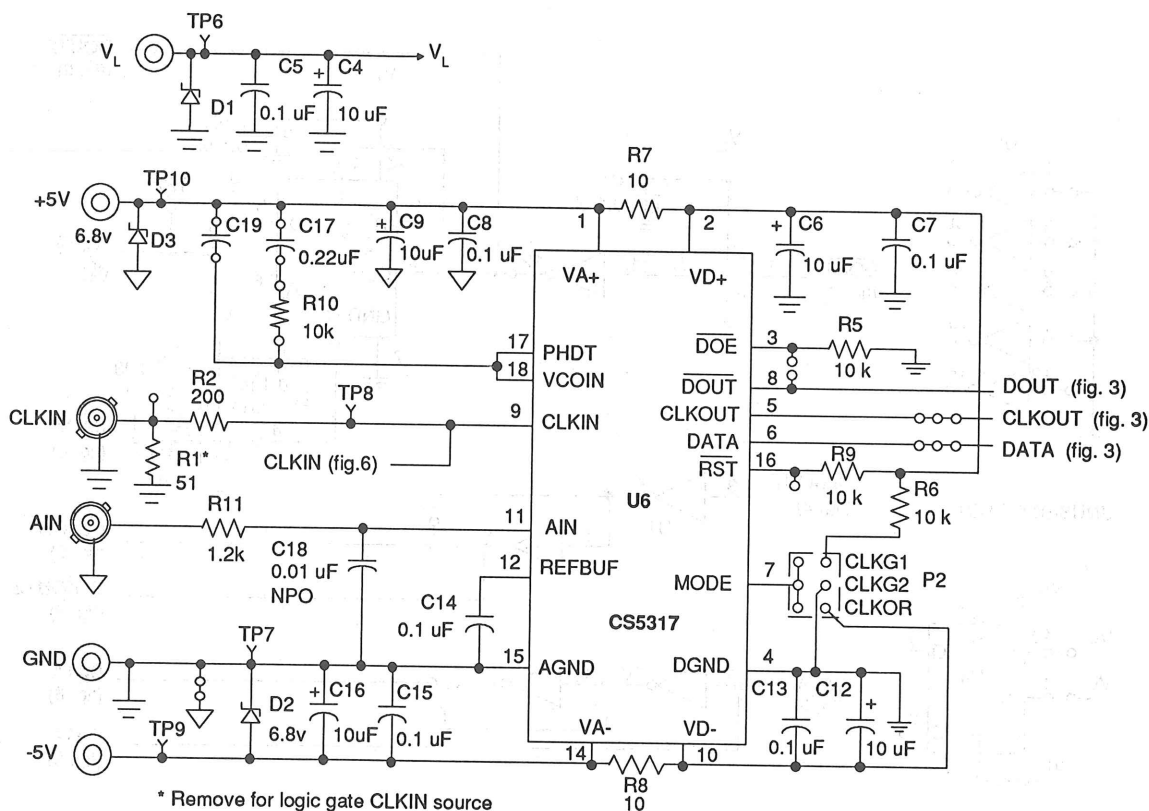
amplitude so that distortion products become negligible. This allows an accurate measurement of the noise floor.

More complex analysis such as intermodulation distortion measurements can be accomplished with the addition of another sine-wave generator.

### CIRCUIT DESCRIPTION

Figure 2 illustrates the CS5317 A/D converter IC circuit connections. The chip operates off of  $\pm 5V$ . These voltages are supplied from a power source external to the evaluation board. Binding posts

are supplied on the board to connect the +5, -5, and ground power lines. A good quality low ripple, low noise supply will give the best performance. The +5 V supply can also be used for VL and should be connected between the VL board jack and the power supply, as opposed to connecting the VL jack straight to the +5V jack. The +5V jack is the positive power source for the CS5317 IC whereas the VL jack supplies power to all the digital ICs. Care should be taken that noise is not coupled between VL and +5V; however, supply noise is generally not a problem with the CS5317 since the on-chip decimation filter will remove any interference outside of its passband. The +5 and -5 V supply lines are fil-



### Figure 2. Analog-to-Digital Converter



tered on the board and then connected to the  $V_A+$  and  $V_A-$  supply pins of the chip. The +5 V and -5V are then connected by means of ten  $\Omega$  resistors to the  $V_D+$  and  $V_D-$  pins respectively. Capacitive filtering is provided on all supply pins of the chip. In addition there is a 0.1  $\mu$ F filter capacitor connected from the REFBUF pin of the chip to the  $V_A-$  supply pin.

To properly operate, the CS5317 chip requires an external (5 V CMOS compatible) clock. A BNC connector labelled CLKIN is provided to connect the off-board clock signal to the board. The CLKIN signal is also available on the 40 pin header connector. The CLKIN signal is one input

to the phase detector of the on-chip phase locked loop of the CS5317.

Header connector P2 (see Figure 2) is provided to allow mode selection for the CS5317 chip. The mode selection works together with the CLKIN signal to set the sample rate and the output word rate of the CS5317. See the CS5317 data sheet for details on mode selection. Two of the available modes (CLKG1 and CLKG2) utilize the on-chip phase locked loop to step up the CLKIN frequency to obtain the necessary sample rate clock for the A/D converter. Another mode (the CLKOR mode) does not use the on-chip PLL but instead drives the sample function directly. The

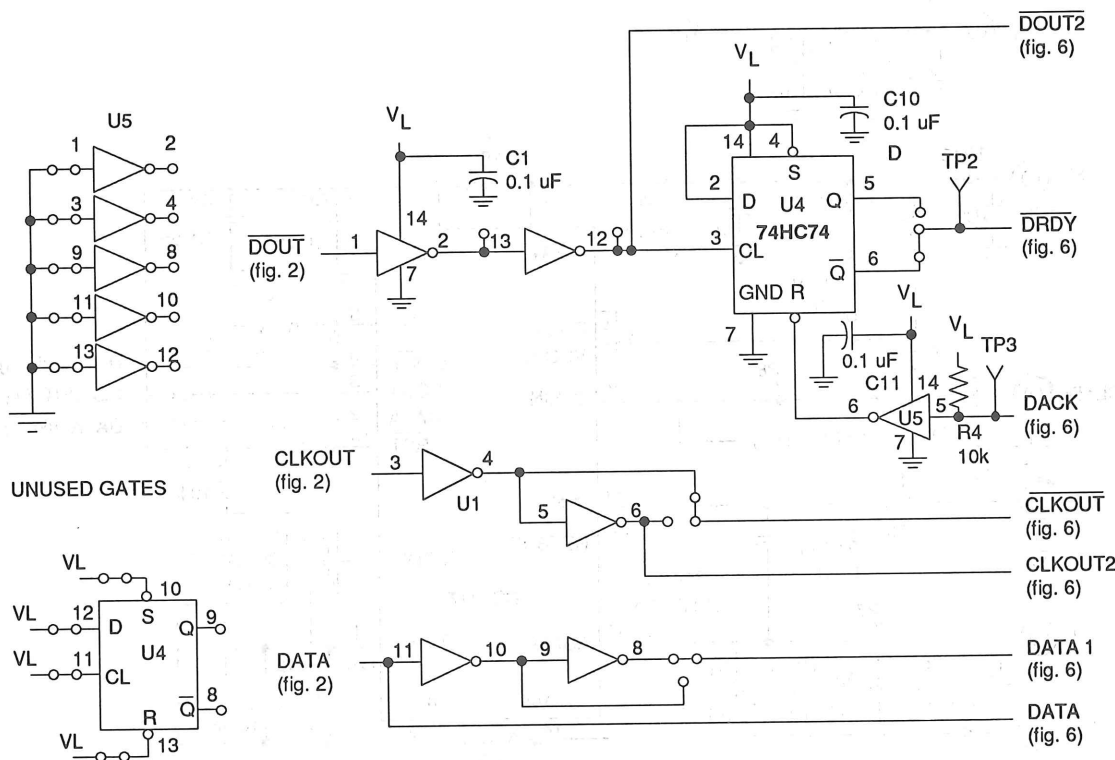
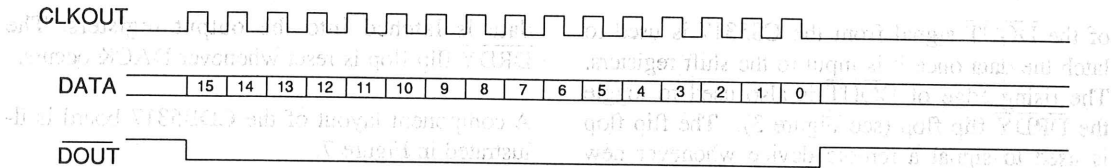


Figure 3. Buffers and Parallel Handshake Flip-Flop



Note: For a complete description of serial timing see the CS5317 Data Sheet

**Figure 4 Serial Data Timing**

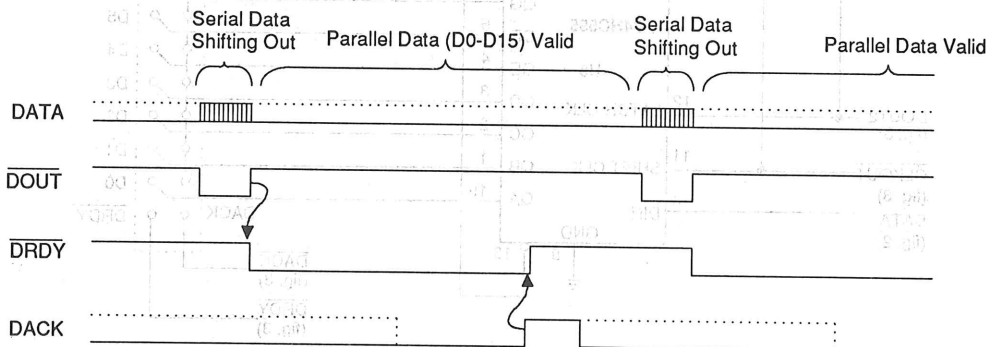
two modes which use the phase locked loop will require appropriate low pass filter components on the Evaluation Board. The low pass filter components help determine the PLL control loop response, including its bandwidth and stability and therefore directly affect the transient response of the PLL control loop. Appropriate filter components should be installed if a particular dynamic response to changes of the CLKIN signal is desired.

The filter components which are installed on the board have been chosen for the following parameters: MODE: CLKG2; CLKIN: 7,200; N=512; damping factor: 1.0; Control loop -3 dB bandwidth: 2262 radians/second. These parameters yield R as 10 k  $\Omega$  and C as 0.22  $\mu$ F for the filter components.

The analog signal to be digitized is input to the AIN BNC connector. The digital output words from the CS5317 are buffered by HEX inverters as shown in Figure 3. The buffered versions of the CLKOUT and DATA signals are available on the header connector P1 in Figure 6. The serial data signals out of the CS5317 are illustrated in Figure 4. If remote control of the  $\overline{\text{DOE}}$  line is desired, the trace on the PC Board can be opened and a wire connection can be soldered to the  $\overline{\text{DOE}}$  input line. Remote control of the  $\overline{\text{RST}}$  line of the CS5317 is also available if desired.

Figures 5 and 6 illustrate the serial to parallel shift registers including timing information. The DATA output signal from the CS5317 is input to the data input of the shift register. An inverted version of the CLKOUT signal is used to clock the DATA into the shift registers. The two 8-bit shift register ICs also include output latches. The rising edge

3



**Figure 5. Parallel Data Timing**

of the  $\overline{\text{DOUT}}$  signal from the CS5317 is used to latch the data once it is input to the shift registers. The rising edge of  $\overline{\text{DOUT}}$  is also used to toggle the  $\overline{\text{DRDY}}$  flip flop (see Figure 3). The flip flop is used to signal a remote device whenever new

data is latched into the output registers. The  $\overline{\text{DRDY}}$  flip flop is reset whenever DACK occurs.

A component layout of the CDB5317 board is illustrated in Figure 7.

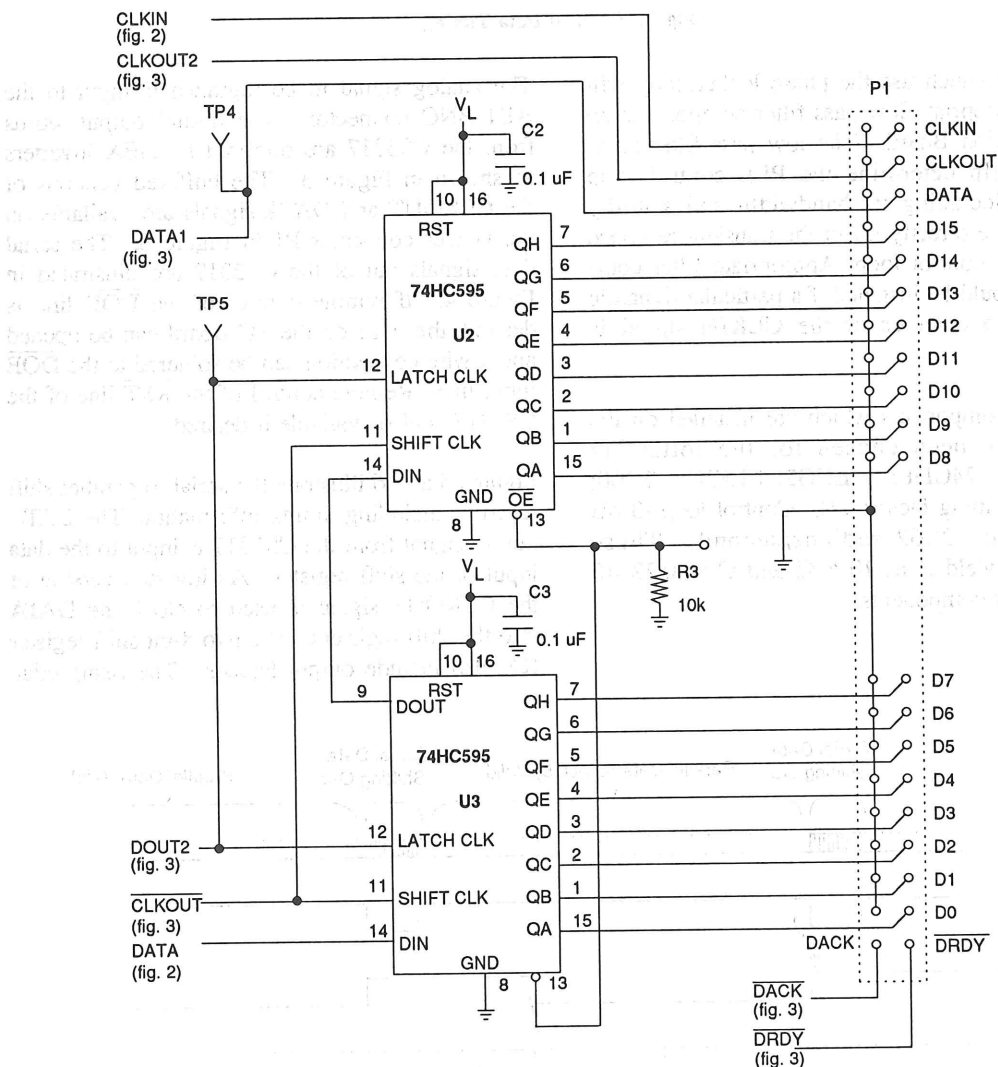


Figure 6.

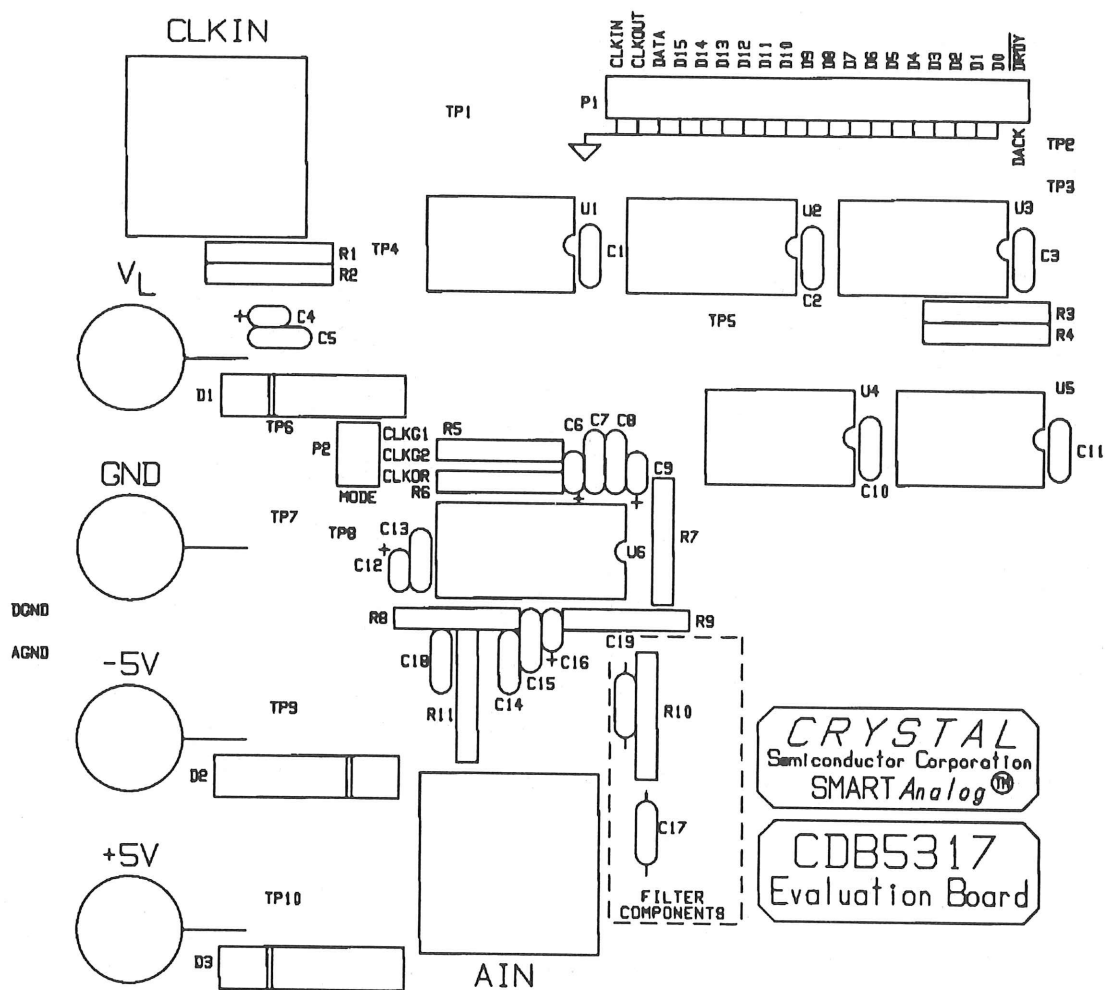


Figure 7. Bird's Eye View

# •Notes•



## 24-Bit Variable Bandwidth A/D Converter

### Features

- Monolithic CMOS A/D Converter
- Dynamic Range
  - 130dB @ 25 Hz Bandwidth
  - 120dB @ 411 Hz Bandwidth
- Delta-Sigma Architecture
  - Variable Oversampling: 64X to 4096X
  - Internal Track-and-Hold Amplifier
- Flexible Filter Chip
  - Hardware or Software Selectable Options
  - Seven Selectable Filter Corner (-3dB) Frequencies: 25, 51, 102, 205, 411, 824 and 1650 Hz
- Low Power Dissipation: < 100mW

### General Description

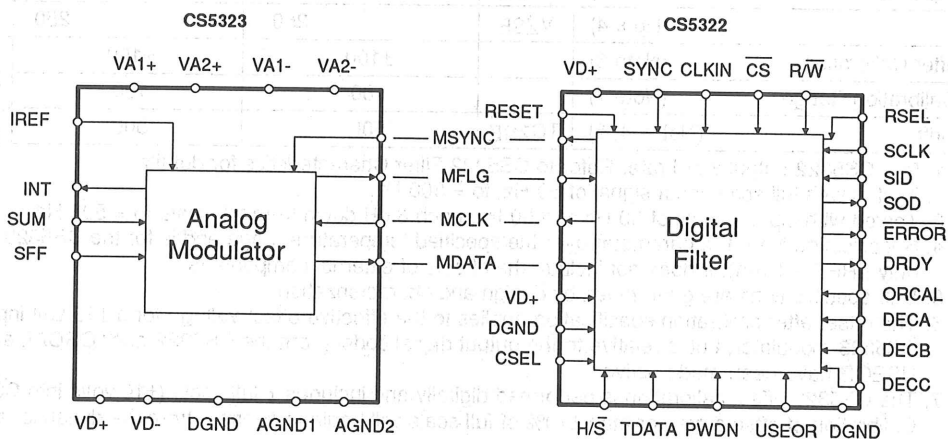
The CS5323 analog modulator and the CS5322 digital filter function together as a unique high resolution A/D converter intended for geophysical and other applications which require high dynamic range. The CS5323/CS5322 combination performs sampling, A/D conversion, and anti-alias filtering.

The pair use Delta-Sigma modulation to produce highly accurate conversions. The CS5323 oversamples, virtually eliminating the need for external anti-alias filters. The CS5322 linear-phase FIR digital filter decimates the output to any one of seven selectable update periods: 16, 8, 4, 2, 1, 0.5 and 0.25 milliseconds. Data is output from the digital filter in a 24-bit serial format.

The CMOS design of the CS5322/CS5323 achieves high reliability while minimizing power dissipation.

### ORDERING INFORMATION

CS5322-KL	0 to +70 °C	28-pin PLCC
CS5322-BL	-40 to +85 °C	28-pin PLCC
CS5323-KL	0 to +70 °C	28-pin PLCC
CS5323-BL	-40 to +85 °C	28-pin PLCC
CDB5322/3		Evaluation Board



### Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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DS70PP5  
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**ANALOG CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A-}$ ,  $V_{D-} = -5V$ ;  $V_{A+}$ ,  $V_{D+} = 5V$ ;  $AGND = 0V$ ;  $CLKIN = 1.024 MHz$ ; Device connected as shown in Figure 16; Logic 1 =  $V_{D+}$ , Logic 0 =  $0V$ ; unless otherwise specified.)

Parameter*	Symbol	CS5323-K			CS5323-B			Units
		Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range		0		+70	-40		+85	°C
<b>Dynamic Performance</b>								
Dynamic Range (Note 1)								
CLKIN = 1.024 MHz:								
fo = 4000 Hz	DR		103			103		dB
fo = 2000 Hz			118			118		dB
fo = 1000 Hz		116	121		116	121		dB
fo = 500 Hz			124			124		dB
fo = 250 Hz			127			127		dB
fo = 125 Hz			129			129		dB
fo = 62.5 Hz			130			130		dB
CLKIN = 512 kHz:								
fo = 2000 Hz	DR		99			99		dB
fo = 1000 Hz			121			121		dB
fo = 500 Hz			125			125		dB
fo = 250 Hz			127			127		dB
fo = 125 Hz			130			130		dB
fo = 62.5 Hz			132			132		dB
fo = 31.25 Hz			133			133		dB
Signal-to-Distortion: CLKIN = 1.024 MHz	SDR	100	110		100	110		dB
(Note 2) CLKIN = 512 kHz	SDR		120			120		dB
Intermodulation Distortion (Note 3)	IMD		110			110		dB
<b>dc Accuracy</b>								
Full Scale Error (Note 4)	FSE		4			4		%
Full Scale Drift (Notes 4, 5)	TCFS		0.005			0.005		%/°C
Offset (Note 4)	VZSE		250			250		mV
Offset after Calibration (Note 6)			±100			±100		μV
Offset Calibration Range (Note 7)			100			100		%F.S.
Offset Drift (Notes 4, 5)	TCZSE		500			500		μV/°C

- Notes:
1. fo = CS5322 output word rate. Refer to CS5322 Filter Characteristics for details.
  2. Tested with full scale input signal of 50 Hz; fo = 500 Hz.
  3. Tested with input signals of 30 Hz and 50 Hz, each 6 dB down from full scale fo = 500 Hz.
  4. Specification is for the parameter over the specified temperature range and is for the CS5323 device only (IREF = 1 mA). It does not include the effects of external components.
  5. Drift specifications are guaranteed by design and characterization.
  6. The offset after calibration specification applies to the effective offset voltage for a ±10 volt input to the CS5323 modulator, but is relative to the output digital codes from the CS5322 after ORCAL and USEOR have been made active.
  7. The CS5322 offset calibration is performed digitally and includes ± full scale (±10 volts into CS5323). Calibration of offsets greater than ±10% of full scale will begin to subtract from the dynamic range.

\* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.



## ANALOG CHARACTERISTICS (Continued)

Parameter*	Symbol	CS5323-K			CS5323-B			Units
		Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range		0		+70	-40		+85	°C
<b>Input Characteristics</b>								
Input Signal Frequencies (Note 8)	BW	dc		1500	dc		1500	Hz
Input Voltage Range (Note 9)	V <sub>IN</sub>	-10.0		+10.0	-10.0		+10.0	V
Input Overrange Voltage (Note 9)	I <sub>OVR</sub>			10			10	%F.S.
<b>Power Supplies</b>								
DC Power Supply Currents (Note 10)								
Positive Supplies (I <sub>A+</sub> and I <sub>D+</sub> )			7.0	10.0		7.0	10.0	mA
Negative Supplies (I <sub>A-</sub> and I <sub>D-</sub> )			8.4	10.0		8.4	10.0	mA
Power Consumption (Note 10)								
PWDN Low	P <sub>DN</sub>		77	100		77	100	mW
PWDN High	P <sub>DS</sub>		0.01	10		0.01	10	mW
Power Supply Rejection (Notes 11,12)								
(dc to f <sub>1</sub> Hz):								
VA+	PSR		60			60		dB
VA-			45			45		dB
VD+			45			45		dB
VD-			40			40		dB
(f <sub>1</sub> Hz to 128 kHz):								
VA+	PSR		60			60		dB
VA-			60			60		dB
VD+			60			60		dB
VD-			60			60		dB

- Notes:
- The upper bandwidth limit is determined by the CS5322 digital filter.
  - This input voltage range is for the configuration shown in Figure 16, the System Connection Diagram, and applies to signal from dc to f<sub>3</sub> Hz. Refer to CS5322 Filter Characteristics for the values of f<sub>3</sub>.
  - All outputs unloaded. All logic inputs forced to VA+ or GND respectively. Power down mode power consumption is with the signal source and the voltage reference source either grounded or floating.
  - Tested with a 100 mVp-p sine wave applied separately to each supply (VA1 and VA2 are considered as one input for this test).
  - Refer to CS5322 Filter Characteristics table for the values of f<sub>1</sub>.

\* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

**FILTER CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ;  $V_{D+} = 5V$ ;  $GND = 0V$ ;  $CLKIN = 1.024 MHz$ ; transfer function shown in Figure 2; unless otherwise specified.)

Output Word Rate $f_0$ (Hz)	Passband $f_1$ (Hz)	Passband Flatness $R_{PB}$ (dB)	-3dB Freq. $f_2$ (Hz)	Stopband $f_3$ (Hz) (Note 13)	Group Delay (ms)
4000	1500	0.2	1652.5	2000	7.25
2000	750	0.04	824.3	1000	14.5
1000	375	0.08	411.9	500	29
500	187.5	0.1	205.9	250	58
250	93.8	0.1	102.9	125	116
125	46.9	0.1	51.5	62.5	232
62.5	23.4	0.1	25.7	31.25	464

Note: 13.  $G_{SB} = -130$  dB for all Output Word Rates.

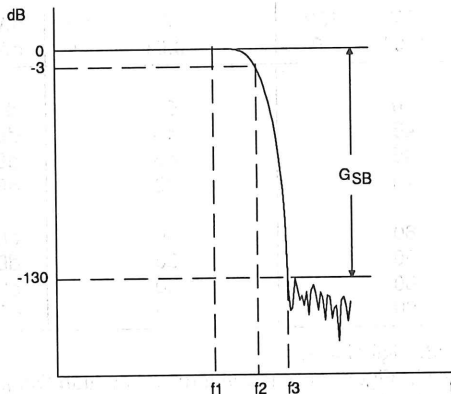


Figure 1. CS5322 Filter Response

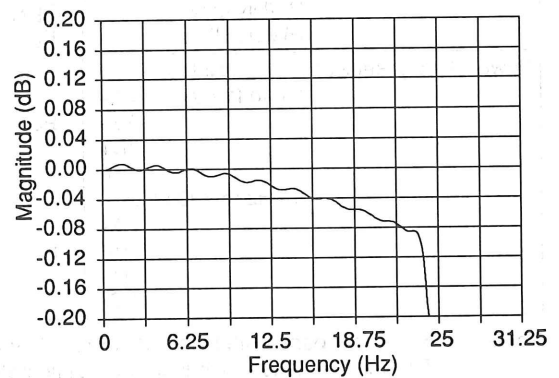


Figure 2. CS5322 Digital Filter Passband Ripple  
 $f_0 = 62.5$  Hz

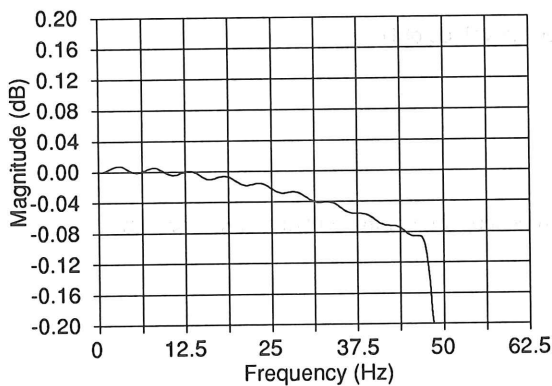


Figure 3. CS5322 Digital Filter Passband Ripple  
 $f_0 = 125$  Hz

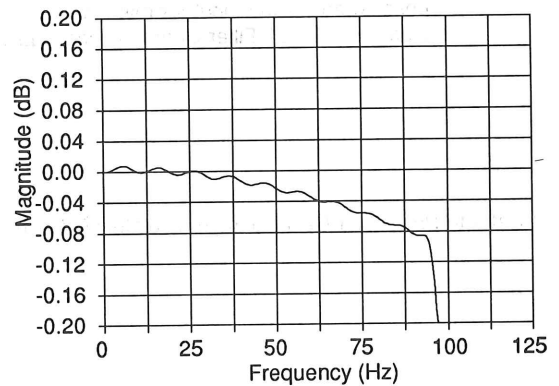
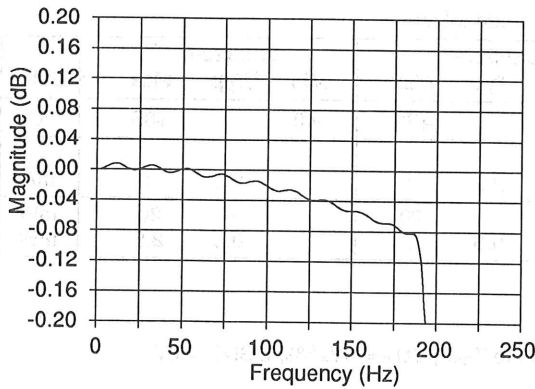
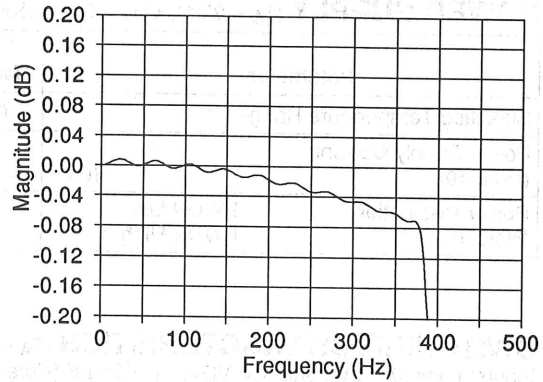


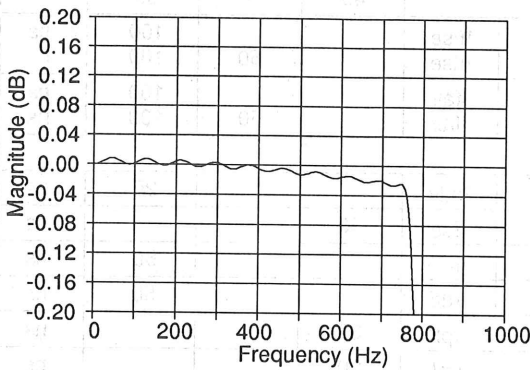
Figure 4. CS5322 Digital Filter Passband Ripple  
 $f_0 = 250$  Hz



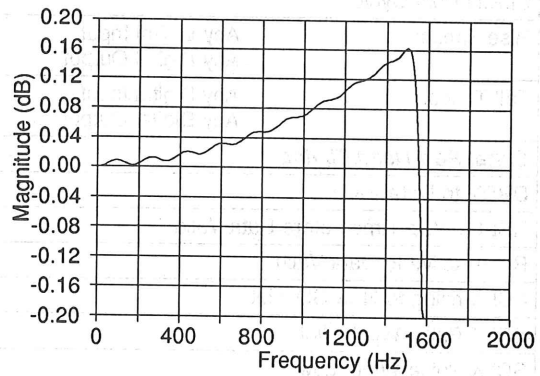
**Figure 5. CS5322 Digital Filter Passband Ripple**  
 $f_0 = 500 \text{ Hz}$



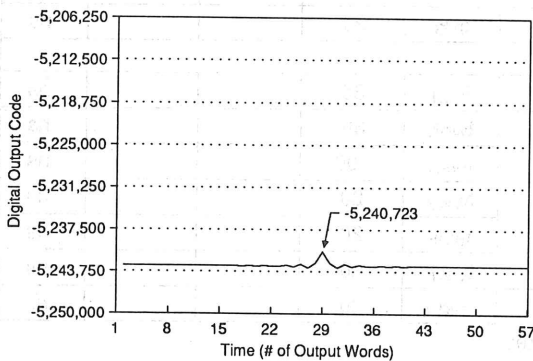
**Figure 6. CS5322 Digital Filter Passband Ripple**  
 $f_0 = 1000 \text{ Hz}$



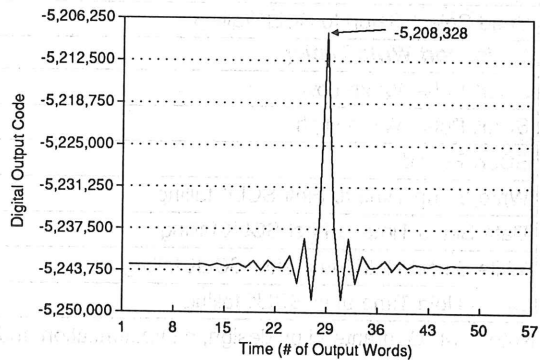
**Figure 7. CS5322 Digital Filter Passband Ripple**  
 $f_0 = 2000 \text{ Hz}$



**Figure 8. CS5322 Digital Filter Passband Ripple**  
 $f_0 = 4000 \text{ Hz}$



**Figure 9. CS5322 Impulse Response,  $f_0 = 62.5 \text{ Hz}$**



**Figure 10. CS5322 Impulse Response,  $f_0 = 1000 \text{ Hz}$**

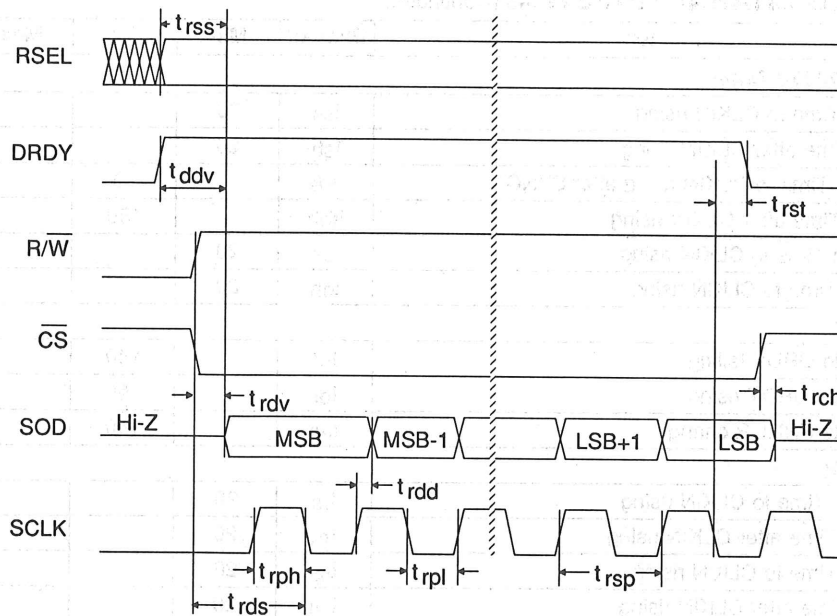
**POWER SUPPLY** ( $T_A = 25^\circ\text{C}$ ;  $V_{D+} = 5\text{V}$ ;  $\text{CLKIN} = 1.024\text{ MHz}$ )

Parameter	CS5322-K			CS5322-B			Units
	Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range	0		+70	-40		+85	$^\circ\text{C}$
Power Supply Current: (Note 10) ID+		2.2	4		2.2	4	mA
Power Dissipation: (Note 10)	PWDN Low	11	20	11	20		mW
	PWDN High	0.6	2.5	0.6	2.5		mW

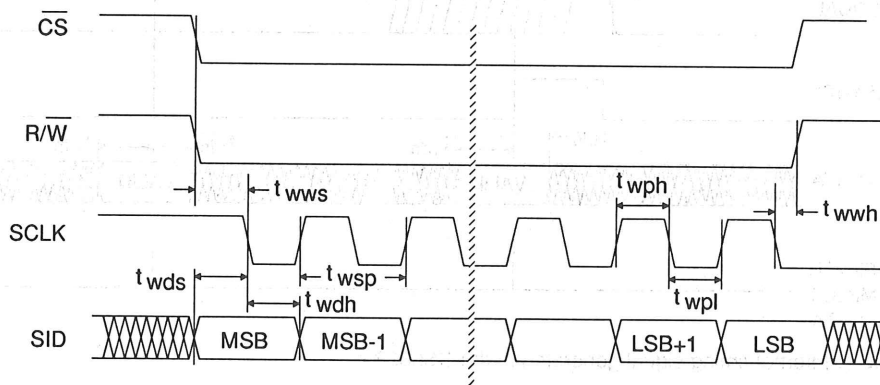
**SWITCHING CHARACTERISTICS** ( $T_A = T_{\min}$  to  $T_{\max}$ ;  $V_{D+} = 5\text{V} \pm 5\%$ ;  $\text{DGND} = 0\text{V}$ ;  
Inputs: Logic 0 = 0V Logic 1 =  $V_{D+}$ ;  $C_L = 50\text{ pF}$  (Note 14))

Parameter		Symbol	Min	Typ	Max	Units
CLKIN Frequency		$f_c$	0.512	1.024	1.1	MHz
CLKIN Duty Cycle			40		60	%
Rise Times:	Any Digital Input	$t_{rise}$			100	ns
	Any Digital Output	$t_{rise}$		50	100	ns
Fall Times:	Any Digital Input	$t_{fall}$			100	ns
	Any Digital Output	$t_{fall}$		50	100	ns
<b>Serial Port Read Timing</b>						
DRDY to Data Valid		$t_{ddv}$			25	ns
RSEL Setup Time before Data Valid		$t_{rss}$	50			ns
Read Active to Data Valid		$t_{rdv}$			50	ns
SCLK rising to New SOD bit		$t_{rdd}$			50	ns
SCLK Pulse Width High		$t_{rph}$	30			ns
SCLK Pulse Width Low		$t_{rpl}$	30			ns
SCLK Period		$t_{rsp}$	100			ns
SCLK falling to DRDY falling		$t_{rst}$			50	ns
CS High to Output Hi-Z		$t_{rch}$			20	ns
Read Select Setup to SCLK falling		$t_{rds}$	20			ns
<b>Serial Port Write Timing</b>						
SCLK Pulse Width Low		$t_{wpl}$	30			ns
SCLK Pulse Width High		$t_{wph}$	30			ns
SCLK Period		$t_{wsp}$	100			ns
Write Setup Time to First SCLK falling		$t_{wws}$	20			ns
Data Setup Time to First SCLK falling		$t_{wds}$	20			ns
Write Select Hold Time after SCLK falling		$t_{wwh}$	20			ns
DATA Hold Time after SCLK falling		$t_{wdh}$	20			ns

Note: 14. Guaranteed by design, characterization and/or test.



SERIAL PORT READ TIMING (R/W = 1, CS = 0, RSEL = 1  
 \* DRDY Does not toggle if reading status, RSEL = 0)

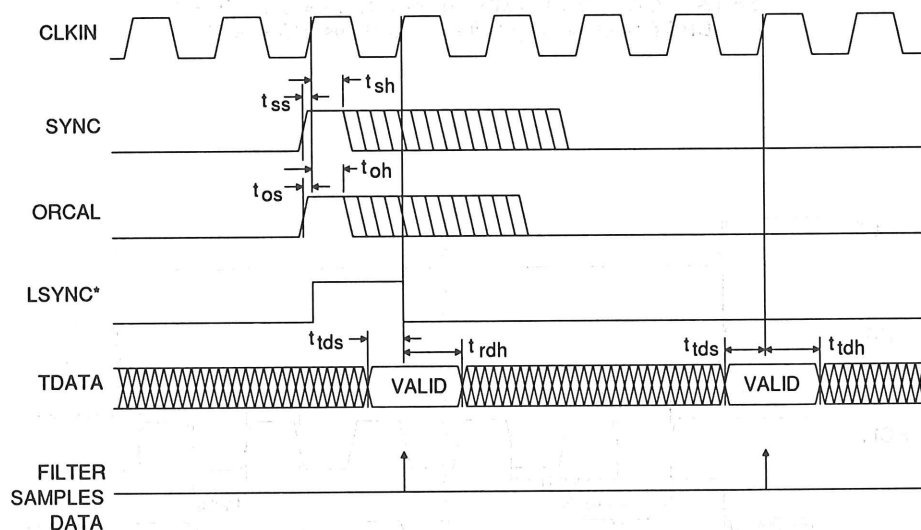


SERIAL PORT WRITE TIMING

Figure 11. CS5322 Serial Port

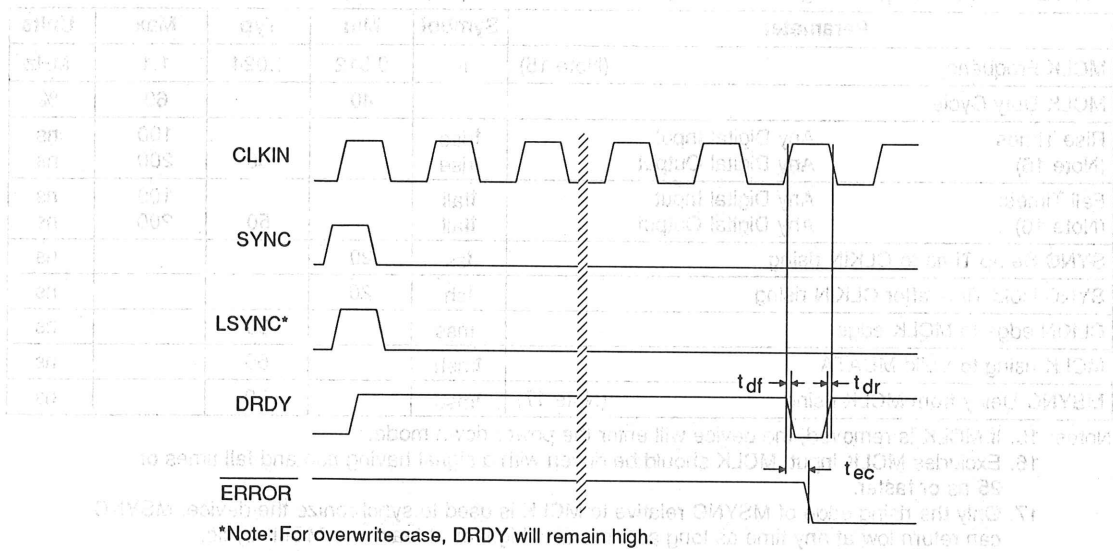
**SWITCHING CHARACTERISTICS (Continued)**

Parameter	Symbol	Min	Typ	Max	Units
<b>Test Data (TDATA) Timing</b>					
SYNC Setup Time to CLKIN rising	$t_{ss}$	20			ns
SYNC Hold Time after CLKIN rising	$t_{sh}$	20			ns
TDATA Setup Time to CLKIN rising after SYNC	$t_{tds}$		20		ns
TDATA Hold Time after CLKIN rising	$t_{tdh}$		150		ns
ORCAL Setup Time to CLKIN rising	$t_{os}$	20			ns
ORCAL Hold Time to CLKIN rising	$t_{oh}$	20			ns
<b>DRDY Timing</b>					
CLKIN rising to DRDY falling	$t_{df}$		140		ns
CLKIN falling to DRDY rising	$t_{dr}$		150		ns
CLKIN rising to ERROR change	$t_{ec}$		140		ns
<b>RESET Timing</b>					
RESET Setup Time to CLKIN rising	$t_{rs}$	20			ns
RESET Hold Time after CLKIN rising	$t_{rh}$	20			ns
SYNC Setup Time to CLKIN rising	$t_{ss}$	20			ns
SYNC Hold Time after CLKIN rising	$t_{sh}$	20			ns

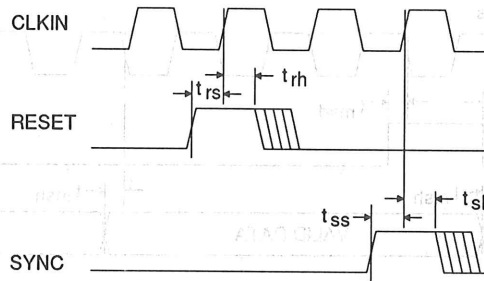


\* Note: Internal timing signal generated in the CS5322

**Figure 12. TDATA Setup/Hold Timing**



**Figure 13. DRDY Timing**



**Figure 14. RESET Timing**



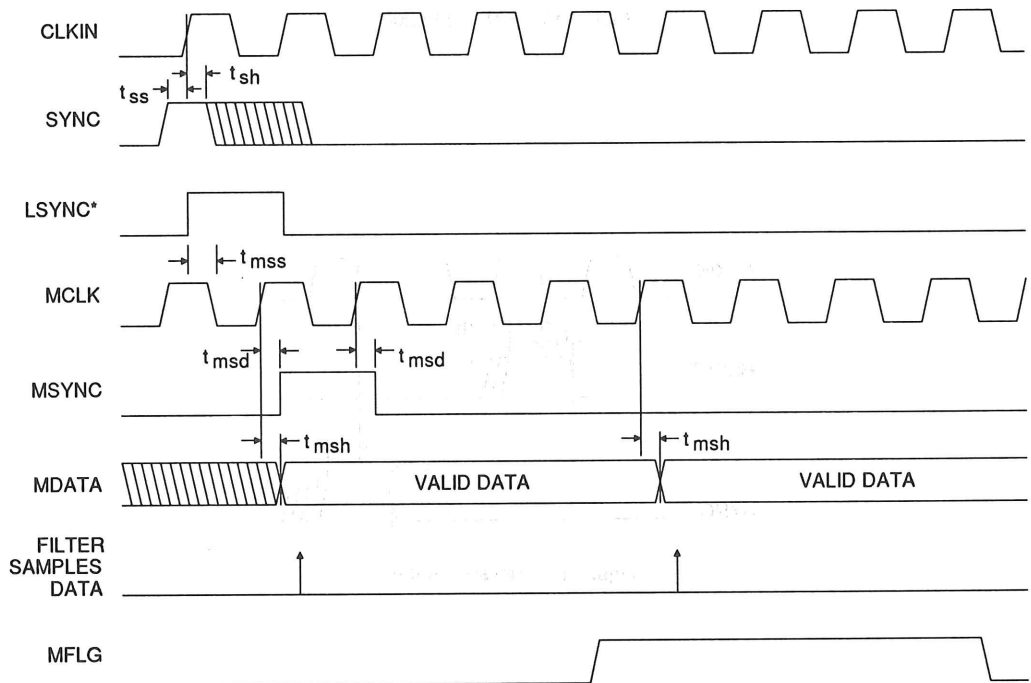
**SWITCHING CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ;  $V_{A+}$ ,  $V_{D+} = 5V \pm 5\%$ ;  $V_{A-}$ ,  $V_{D-} = -5V \pm 5\%$ ; Inputs: Logic 0 = 0V Logic 1 =  $V_{D+}$ ;  $C_L = 50$  pF (Note 14))

Parameter		Symbol	Min	Typ	Max	Units
MCLK Frequency	(Note 15)	$f_c$	0.512	1.024	1.1	MHz
MCLK Duty Cycle			40		60	%
Rise Times: (Note 16)	Any Digital Input	$t_{rise}$		50	100	ns
	Any Digital Output	$t_{rise}$			200	ns
Fall Times: (Note 16)	Any Digital Input	$t_{fall}$		50	100	ns
	Any Digital Output	$t_{fall}$			200	ns
SYNC Setup Time to CLKIN rising		$t_{ss}$	20			ns
SYNC Hold Time after CLKIN rising		$t_{sh}$	20			ns
CLKIN edge to MCLK edge		$t_{mss}$		30		ns
MCLK rising to Valid MDATA		$t_{msh}$		50		ns
MSYNC Delay from MCLK rising		$t_{msd}$		90		ns
		(Note 17)				

Notes: 15. If MCLK is removed, the device will enter the power down mode.

16. Excludes MCLK input. MCLK should be driven with a signal having rise and fall times of 25 ns or faster.

17. Only the rising edge of MSYNC relative to MCLK is used to synchronize the device. MSYNC can return low at any time as long as it remains high for at least one MCLK cycle.



\* Internal timing signal generated in the CS5322

**Figure 15. CS5322/CS5323 Interface Timing**

**DIGITAL CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ;  $V_{D+} = 5.0V \pm 5\%$ ;  $GND = 0V$ ; measurements performed under static conditions)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Drive Voltage	$V_{IH}$	$(V_{D+}) - 0.3$			V
Low-Level Input Drive Voltage	$V_{IL}$			0.3	V
High-Level Input Threshold (Note 18)		$(V_{D+}) - 1.0$			V
Low-Level Input Threshold (Note 18)				1.0	V
High-Level Output Voltage $I_{OUT} = -40 \mu A$ (Note 19)	$V_{OH}$	$(V_{D+}) - 0.6$			V
Low Level Output Voltage $I_{OUT} = +1.6 mA$ (Note 19)	$V_{OL}$			0.4	V
CS5322 $I_{OUT} = +40 \mu A$	$V_{OL}$			0.4	V
CS5323					
Input Leakage Current All pins except MFLG, SOD	$I_{LKG}$			$\pm 10$	$\mu A$
Three-State Leakage Current	$I_{OZ}$			$\pm 10$	$\mu A$
Digital Input Capacitance	$C_{IN}$		9		pF
Digital Output Capacitance	$C_{OUT}$		9		pF

Notes: 18. Device is intended to be driven with CMOS logic levels.

19. Device is intended to be interfaced to CMOS logic. Resistive loads are not recommended on these pins.

**RECOMMENDED OPERATING CONDITIONS** (Voltages with respect to  $GND = 0V$ )

Parameter	Symbol	Min	Typ	Max	Units
DC Supply: (Note 20)					
Positive Analog	$V_{A+}$	4.75	5.0	5.25	V
Negative Analog	$V_{A-}$	-4.75	-5.0	-5.25	V
Positive Digital	$V_{D+}$	4.75	5.0	5.25	V
Positive Digital	$V_{D-}$	-4.75	-5.0	-5.25	V
Ambient Operating Temperature -KL	$T_A$	0		+70	$^{\circ}C$
-BL	$T_A$	-40		+85	$^{\circ}C$

Notes: 20. The maximum voltage differential between the Positive Supply of the CS5323 and the Positive Digital Supply of the CS5322 must be less than 0.25V.

**ABSOLUTE MAXIMUM RATINGS\*** (Voltages with respect to  $GND = 0V$ )

Parameter	Symbol	Min	Typ	Max	Units
DC Supplies: (Note 20)					
Positive Analog	$V_{A+}$	-0.3		6.0	V
Negative Analog	$V_{A-}$	0.3		-6.0	V
Positive Digital	$V_{D+}$	-0.3		$(V_{A+}) + 0.3$	V
Positive Digital	$V_{D-}$	0.3		-6.0	V
Input Current, Any Pin Except Supplies (Note 21)	$I_{in}$			$\pm 10$	mA
Digital Input Voltage CS5322	$V_{IND}$	-0.3		$(V_{D+}) + 0.3$	V
CS5323	$V_{IND}$	-0.3		$(V_{A+}) + 0.3$	V
Storage Temperature	$T_{stg}$	-65		150	$^{\circ}C$

Notes: 21. Transient currents of up to 100 mA will not cause SCR latch up.

\*WARNING: Operation beyond these limits may result in permanent damage to the device.

## GENERAL DESCRIPTION

The CS5322 is a monolithic digital Finite Impulse Response (FIR) filter with programmable decimation. The CS5323 is a monolithic CMOS A/D converter designed specifically for very high resolution measurement of signals between dc and 1500 Hz. The CS5322 and CS5323 are intended to be used together to form a unique high resolution A/D system.

The CS5323 utilizes a fourth order oversampling architecture to achieve high resolution A/D conversion. The modulator consists of a 1-bit A/D

converter embedded in a negative feedback loop. The first stage of the fourth order modulator uses discrete components external to the chip to maximize signal to noise. The modulator provides an oversampled serial bit stream at 256 Kbits per second ( $CLKIN = 1.024$  MHz) to the CS5322 FIR decimation filter.

The CS5322 provides the digital anti-alias filter for the CS5323 modulator output. The CS5322 consists of: A multi-stage FIR filter, four registers (status, data, offset, and configuration), a flexible serial input and output port, and a 2-channel input data multiplexer that selects data

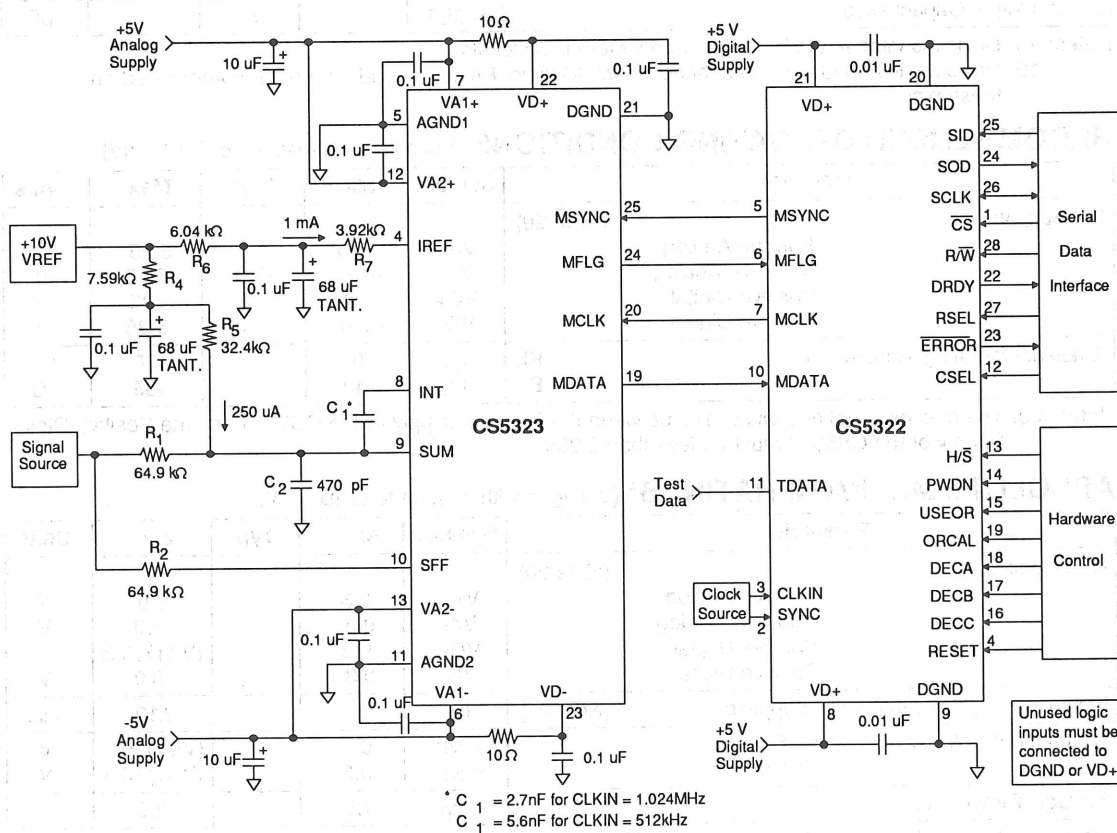


Figure 16. System Connection Diagram

from the CS5323 (MDATA) or user test data (TDATA). The CS5322 decimates (64X to 4096X) the output to any of seven selectable update periods: 16, 8, 4, 2, 1, 0.5 and 0.25 milliseconds. Data is output from the digital filter in a 24-bit serial format. Figure 17 illustrates the CS5322 Block Diagram.

### CS5323 Signal Input and Current Reference

The CS5323 uses a number of external discrete components to achieve maximum rated performance. Figure 16 illustrates the recommended circuit configuration for the current reference and signal input components.

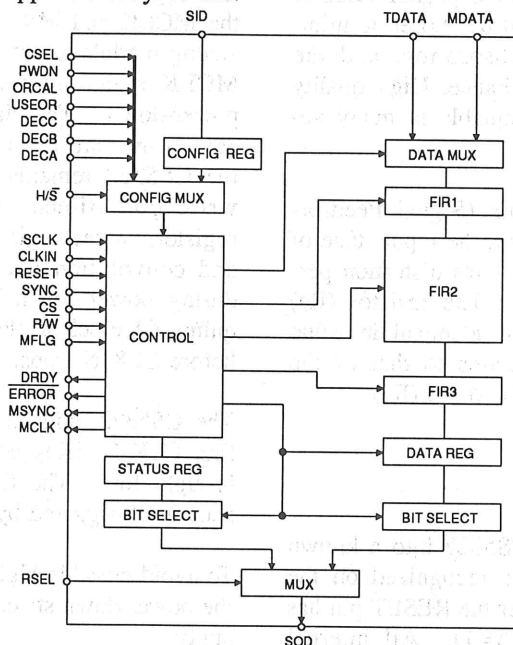
The CS5323 is designed to use a current reference of 1 mA into the IREF pin. A current reference rather than a voltage reference was chosen to achieve better noise performance. For optimum performance the dc source impedance at the IREF pin should be approximately 10 k $\Omega$ .

This calls for a 10 volt reference source driving the 10 k $\Omega$  ( $R_6 + R_7$ ) resistor to achieve the desired 1 mA current source. The IREF input sets the full scale gain of the A/D converter.

A current source 1/4 the size of the IREF input current must be sourced into the integrator summing junction at the SUM pin. This requires a 40 k $\Omega$  resistance ( $R_4 + R_5$ ) be placed from the 10 volt reference to the SUM pin.

The 1 mA IREF current and the 250  $\mu$ A sources have capacitive filtering to aid in reducing the broadband current noise from the voltage reference. These capacitors should be of quality construction. Particular attention should be paid to leakage current variation over the desired operating temperature, as this leakage will affect the system gain.

The signal input pin (SUM) of the CS5323 is the summing junction of the input integrator stage.



**Figure 17. CS5322 Block Diagram**

This integrator is designed to use an external input resistor ( $R_1$ ) and integrating capacitor ( $C_1$ ). In addition, a capacitor ( $C_2$ ) is required at this node for proper compensation of the integrator. The size of the input resistor ( $R_1$ ) is determined by the magnitude of the signal current. With a maximum input voltage onto the resistor, the integrator input current must be set equal to approximately 0.15 the current value injected into the IREF pin. With a 1 mA IREF current, the full scale signal current should be about 150  $\mu$ A. Additionally, to minimize current noise into the summing junction, the value of the effective input resistor should be above 8 k $\Omega$ . Using the 64.9 k $\Omega$  resistor for  $R_1$  sets the full scale input voltage onto the integrating resistor to a value near 10 volts. The input signal then spans 20 V<sub>p-p</sub>.

The integrator resistor and capacitor combination should yield a frequency ( $f=1/(2\pi R_1 C_1)$ ) between 850 and 950 Hz to achieve maximum performance. This results in a capacitor value of 2.7 nF. The capacitor should be chosen to minimize leakage, dielectric absorption, and the voltage coefficient of capacitance. High quality film capacitors may be acceptable in many applications.

The signal into the SFF pin (Signal Feedforward) of the CS5323 bypasses the input stage of the input integrator and improves distortion performance in the passband. The resistor ( $R_2$ ) used at this input should be identical in value and performance characteristics to that of the resistor on the input of the SUM pin ( $R_1$ ).

### RESET Operation

The RESET pin puts the CS5322 into a known initialized state. RESET is recognized on the next CLKIN rising edge after the RESET pin has been brought high (RESET=1). All internal logic is initialized when RESET is active.

Normal device operation begins on the second CLKIN rising edge after RESET is brought low. The CS5322 will remain in an idle state, not performing convolutions, until triggered by a SYNC event.

A RESET operation clears memory, sets the data output register, offset register, and status flags to all zeroes, and sets the configuration register to the state of the corresponding hardware pins (PWDN, ORCAL, DECC, DECB, DECA, USEOR, and CSEL). The reset state is entered on power on, independent of the RESET pin. If RESET is low, the first CLKIN will exit the power on reset state.

### Power-down Operation

The PWDN pin puts the CS5322 into the power-down state. The power-down state is entered on the first CLKIN rising edge after the PWDN pin is brought high. While in the power-down state, the MCLK and MSYNC signals to the CS5323 analog modulator are held low. The loss of the MCLK signal to the modulator causes it to power-down. The signals on the MDATA and MFLG pins are ignored. The serial interface of the CS5322 remains active allowing read and write operations. Information in the data register, offset register, configuration register, and convolution data memory are maintained during power-down. The internal controller requires 64 clock cycles after PWDN is asserted before CLKIN stops.

The CS5322 exits the power-down state on the first CLKIN rising edge after the PWDN pin is brought low. The CS5322 then enters an idle state until triggered by a SYNC event.

To avoid possible high current states while in the power down state, the following conditions apply:

1. CLKIN must be active for at least 64 clock cycles after PWDN entry.
2. CSEL and TDATA must not both be asserted high.

### SYNC Operation

The SYNC pin is used to start convolutions and synchronize the CS5322 and CS5323 to an external sampling source or timing reference. The SYNC event is recognized on the first CLKIN rising edge after the SYNC pin goes high. SYNC may remain high indefinitely. Only the sequence of SYNC rising followed by CLKIN rising generates a SYNC event.

The SYNC event aligns the output sample and causes the filter to begin convolutions. The first SYNC event causes an immediate DRDY provided DRDY is low. Subsequent data ready events will occur at a rate determined by the decimation rate inputs DECC, DECB, and DECA. Multiple SYNC events can be applied with no effect on operation if they are perfectly timed according to the decimation rate. Any SYNC event not in step with the decimation rate will cause a re-alignment and loss of data.

### Serial Read Operation

Serial read is used to obtain status or conversion data. The  $\overline{CS}$ ,  $R/\overline{W}$ , SCLK, RSEL, and SOD pins control the read operation. The serial read operation is activated with the  $\overline{CS}$  pin low ( $\overline{CS}=0$ ) and the  $R/\overline{W}$  pin high ( $R/\overline{W}=1$ ). The RSEL pin selects between conversion data (data register) or status information (status register). The selected serial bit stream is output on the SOD (Serial Output Data) pin.

On read select, SCLK can either be high or low, the first bit appears on the SOD pin and should be latched on the falling edge of SCLK. After the first SCLK falling edge, each SCLK rising

edge shifts out a new bit. Status reads are 16 bits, and data reads are 24 bits. Both streams are supplied as MSB first, LSB last.

In the event more SCLK pulses are supplied than necessary to clock out the requested information, trailing zeroes will be output for data reads and trailing LSB's for status reads. If the read operation is terminated before all the bits are read, the internal bit pointer is reset to the MSB so that a re-read will give the same data as the first read, with one exception. The status error flags are cleared on read and will not be available on a re-read.

The status error flags must be read before entering the powerdown state. If an error has occurred before entering powerdown and the status bit (ERROR) has not been read, the status bits (ERROR, OVERWRITE, MFLG, ACC1 and ACC2) may not be cleared on status reads. Upon exiting the powerdown state and entering normal operation, the user may be flagged that an error is still present.

The SOD pin floats when read operation is deactivated. This enables the SID and SOD pins to be tied together to form a bi-directional serial data bus. There is an internal nominal 100k $\Omega$  pull-up resistor on the SOD pin.

### Serial Write Operation

Serial write is used to write data to the configuration register. The  $\overline{CS}$ ,  $R/\overline{W}$ , SCLK and SID pins control the serial write operation. The serial write operation is activated with the  $\overline{CS}$  pin low ( $\overline{CS}=0$ ) and the  $R/\overline{W}$  pin low ( $R/\overline{W}=0$ ).

Serial input data on the SID pin is sampled on the falling edge of SCLK. The input bits are stored in a temporary buffer until either the write operation is terminated or 8 bits have been received. The data is then parallel loaded into the configuration register. If fewer than 8 bits are

input before the write termination, the other bits may be indeterminant.

The serial bit stream is received MSB first, LSB last. The order of the input control data is PWDN first, followed by ORCAL, USEOR, CSEL, Reserved, DECC, DECB, and DECA. The configuration data bits are defined in Table 1. The configuration data controls device operation when only in the software mode, i.e., the H/S pin is low ( $H/\bar{S}=0$ ). The Reserved configuration data bit must always be written low.

### Offset Calibration Operation

The offset calibration routine computes the offset produced by the CS5323 modulator and stores this value in the offset register. The USEOR pin determines if the offset register data is to be used to correct output words.

To start an offset calibration, the CS5323 analog input must represent the offset value. With the ORCAL pin of the CS5322 high (ORCAL=1), the CS5322 must be RESET, and then a SYNC signal applied. The filter settles on the input value in 56 output words. The output word rate is determined by the state of the the decimation rate control pins, DECC, DECB, and DECA. On the 57th output word, the CS5322 issues the ORCALD status flag, outputs the offset data

sample, and internally loads the offset register. During calibration, the offset register value is not used.

If USEOR is high (USEOR=1), subsequent samples will have the offset subtracted from the output. The state of USEOR must remain high for the complete duration of the convolution cycle. If USEOR is low (USEOR=0), the output word is not corrected, but the offset register retains its value for later use. The results of the last calibration will be held in the offset register until the end of a new calibration, or until the CS5322 is reset using the RESET pin. USEOR does not alter the offset register value, only its usage.

To restart a calibration, ORCAL and SYNC must be taken low. Then the CS5322 must be RESET. The calibration will restart on the next SYNC event that follows ORCAL being brought high. If the ORCAL pin remains in a high state, a single calibration will start on the first SYNC signal.

### Status Bits

The Status Register is a 16-bit register which allows the user to read the flags and configuration settings of the CS5322. Table 2 documents the data bits of the Status Register.

Input Bit #	Equivalent Hardware Function	Description
1 (MSB)	PWDN	Standby mode
2	ORCAL	Self-offset calibration
3	USEOR	Use Offset Register
4	CSEL	Channel Select
5	Reserved	Factory use only
6	DECC	Filter BW selection
7	DECB	Filter BW selection
8 (LSB)	DECA	Filter BW selection

**Table 1. Configuration Data Bits**



Output Bit #	Function	Description
1 (MSB)	ERROR	Detects one of the errors below
2	OVERWRITE Error	Overwrite Error
3	MFLG Error	Modulator Flag Error
4	ACC1 Error	Accumulator 1 Error
5	ACC2 Error	Accumulator 2 Error
6	DRDY	Data Ready
7	1SYNC	First sample after SYNC
8	ORCALD	Offset calibration done
9	PWDN	Standby Mode
10	ORCAL	Self-offset calibration
11	USEOR	Use Offset Register
12	CSEL	Channel Select
13	Reserved	Factory use only
14	DECC	Bandwidth Selection Status
15	DECB	Bandwidth Selection Status
16	DECA	Bandwidth Selection Status

**Table 2. Status Data (from the SOD Pin)**

The ERROR flag, ERROR, is the OR'ed result of OVERWRITE, MFLG, ACC1, and ACC2. The ERROR bit is active high whenever any of the four error bits are set due to a fault condition. The ERROR output has a nominal 100K $\Omega$  internal pull-up resistor.

The OVERWRITE bit is set when new conversion data is ready to be loaded into the data register, but the previous data was not completely read out. This can occur on either of two conditions: a read operation is in progress or a read operation was started, then aborted, and not completed. These two conditions are data read attempts. The attempt is identified by the first SCLK low edge (MSB read) of a data register read. If a data register read is not attempted, the CS5322 assumes that data is not wanted and does not assert OVERWRITE, and the old data is over-written by the new data. On an OVERWRITE condition, the old partially read data is preserved, and the new data word is lost.

Status reads have no effect on OVERWRITE assert operations. The OVERWRITE bit is cleared on a status register read or RESET.

The MFLG error bit reflects the CS5323 MFLG signal. Any high level on the CS5322 MFLG pin will set the MFLG status bit. The bit is cleared on a status register read or RESET operation, only if the MFLG pin on the CS5322 has returned low. A internal nominal 100K $\Omega$  pull-down resistor is on the MFLG pin.

The accumulator error bits, ACC1 and ACC2, indicate that an underflow or overflow has occurred in the FIR1 filter for ACC1, or the FIR2 and FIR3 filters for ACC2. Both errors are cleared on a status read, provided the error conditions are no longer present. In normal operation the ACC1 error will only occur when the input data stream to FIR1 is all 1's for more than 32 bits. The ACC2 error cannot occur in normal operation.

The DRDY bit reflects the state of the DRDY pin. DRDY rising edge indicates that a new data

word has been loaded into the data register and is available for reading. DRDY will fall after the SCLK falling edge that reads the data register LSB. If no data read attempt is made, DRDY will pulse low for 1/2 CLKIN cycle, providing a positive edge on the new data availability. In the OVERWRITE case, DRDY remains high because new data is not loaded at the normal end of conversion time.

The 1SYNC status bit provides an indication of the filter group delay. It goes high on the second output sample after SYNC and is valid for only that sample. For repetitive SYNC operations, SYNC must run at one fourth the output word rate or slower to avoid interfering with the 1SYNC operation. With these slower repetitive SYNC's or non-periodic SYNC's separated by at least three output words, 1SYNC will occur on the second output sample after SYNC.

ORCALD indicates that calibration of the offset register is complete and the offset sample is available in the output register. This flag is high only during that sample and is otherwise low.

The remaining eight status bits (PWDN, ORCAL, USEOR, CSEL, Reserved, DECC, DECB, AND DECA) provide configuration readback for the user. These bits echo the con-

trol source for the CS5322 such that in the hardware mode ( $H/\bar{S}=1$ ), they follow the corresponding input pins. In host mode ( $H/\bar{S}=0$ ) they follow the corresponding configuration bits.

A brief explanation of the eight bits are as follows:

**PWDN** - When high, indicates that the CS5322 is in the power-down state.

**ORCAL** - When high, indicates a potential calibration start.

**USEOR** - When high, indicates the Offset Register is used. During calibration, this bit will read zero indicating the offset register is not being used during calibration.

**CSEL** - When high, TDATA is selected as the filter source. When low, the MDATA output signal from the CS5323 is selected as the input source to the filter.

**Reserved** - Always reads low.

**DECC, DECB, and DECA** - Indicate the decimation rate of the filter and are defined in Table 3.

DECC	DECB	DECA	Output Word Rate (Hz)	Clocks Filter Output
0	0	0	62.5	16384
0	0	1	125	8192
0	1	0	250	4096
0	1	1	500	2048
1	0	0	1000	1024
1	0	1	2000	512
1	1	0	4000	256
1	1	1	Reserved	-

**Table 3. Bandwidth Selection: Truth Table**

### Digital Output and Data Format

For proper operation the CS5322 must be provided with a CMOS-compatible clock into the CLKIN pin. The normal operating frequency is 1.024 MHz. This clock determines the input sample rate. The sample rate is CLKIN/4 while the output word rate is determined by the status of the DECC, DECB, and DECA input pins or configuration bits; depending whether in the hardware mode or host mode.

The CS5322 computes a serial 24-bit output word in two's complement format. The output codes range from decimal -5242880 to +5242879 for a  $\pm 10V$  sine wave input into the CS5323 modulator as shown in Table 4.

Modulator Input Signal	Digital Filter Output Code	
	HEX	Decimal
approx. +16 V †	7FEFFF	+8384511
approx. +11 V	57FFFF	+5767167
approx. +10 V	4FFFFF	+5242879
0 V	000000	0
approx. -10 V	B00000	-5242880
approx. -11 V	A00000	-5767168
approx. -16 V †	800000	-8388608

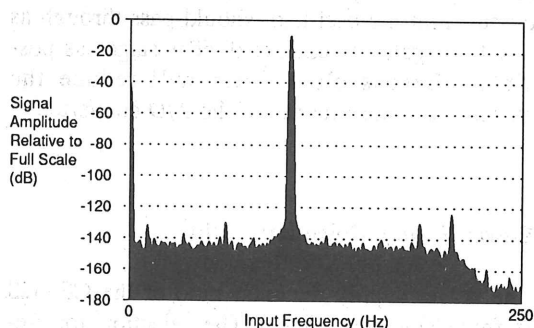
† This is an overrange condition

**Table 4. Output Coding for the CS5322 and CS5323 combination**

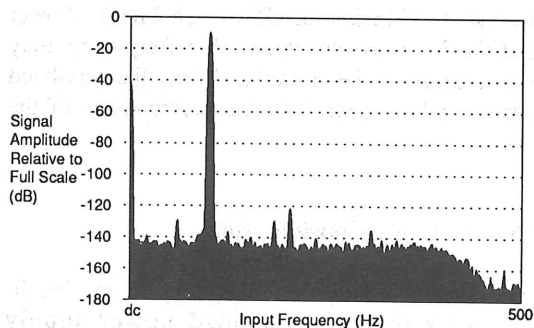
### Performance

The CS5322/23 A/D converter is intended for use in seismic and passive sonar applications. These applications require particularly high dynamic range capability. The CS5322/23 offers high dynamic range without compromising spectral purity. The CS5322/23 typically achieves 120 dB of dynamic range, while maintaining signal/distortion at 110 dB.

An A/D converter system using the CS5322/23 A/D converter as its core was tested using Fast Fourier Transform techniques. Data was collected from the CS5322/23 serially via a UART interface to a PC-compatible computer. The output from the CS5322 was submitted to a windowing algorithm and then to the FFT algorithm. Figure 18 illustrates the performance of the CS5322/23 when tested with a full scale 100 Hz signal for the 2 ms filter selection. The CS5322/23 exhibits some second harmonic but no third harmonic. The test frequency of 100 Hz was selected, as this was the center frequency of a bandpass filter constructed to reject harmonics and line frequencies present at the output of the signal generator. Figure 19 illustrates the perfor-



**Figure 18. 1024 Point FFT Plot with Full Scale Input, 100 Hz.**



**Figure 19. 1024 Point FFT Plot with Full Scale Input, 100 Hz.**

mance of the CS5322/23 (100 Hz input signal) for the 1 ms filter selection. Note that the performance of the CS5322/23 will generally exceed the capability of most available sine wave test generators for frequencies between 2-500 Hz. The excess noise is due to the signal source.

### Clock Source Considerations

To obtain maximum performance from the CS5322/CS5323 chip set requires a CLKIN signal with a very low level of clock jitter, i.e., less than 10 picoseconds of jitter. A well designed crystal-based clock is preferred. The clock oscillator should have a well-regulated supply, with local bypass capacitors at the oscillator. The output from the oscillator should pass through a few logic gates or counter-divider stages as possible. Excess clock jitter will reduce the signal/noise performance of the A/D converter.

### Power Supply Rejection Ratio

The power supply rejection ratio of the CS5323 is frequency dependent. The rejection for frequencies between dc and  $f_1$  Hz (CLKIN=1.024 MHz) is nearly constant. Above  $f_1$  Hz, the CS5322 digital filter will aid in rejecting interference until the frequencies near CLKIN/21.3 (above 48 kHz for CLKIN=1.024 MHz). Power supply interference above this frequency may cause noise to be modulated into the passband (dc to  $f_1$  Hz), degrading the performance of the A/D.

### Power Supply Considerations

The system connection diagram, Figure 16, illustrates the recommended power supply arrangements. The CS5323 has two positive analog supply pins and two negative analog supply pins. Multiple pins are used to minimize

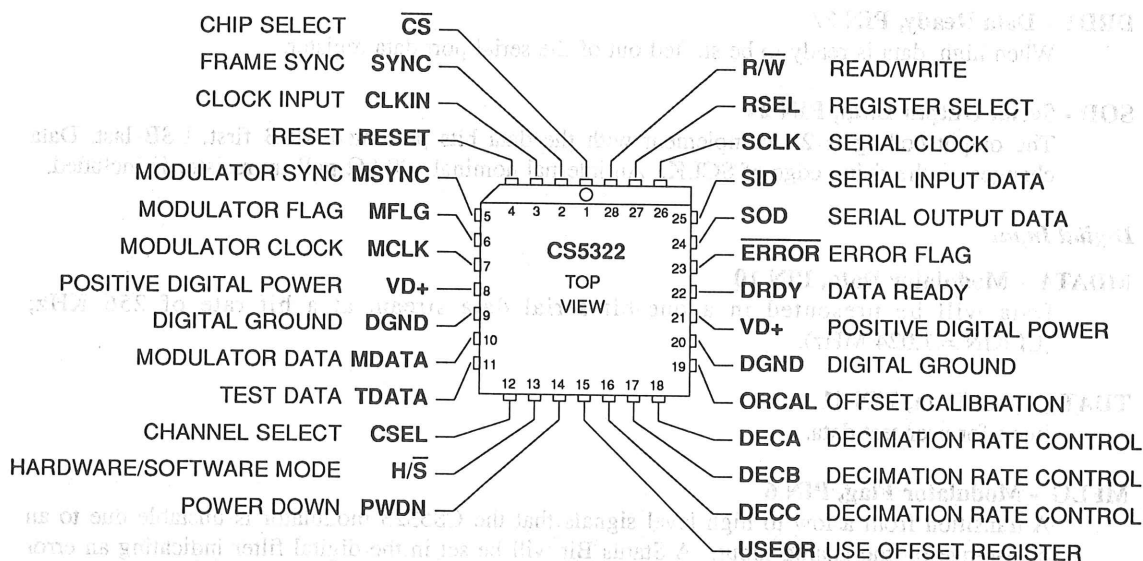
the possibility of noise coupling on the chip. All six power supply pins should be decoupled to their respective grounds, with a 0.1  $\mu$ F capacitor located near the device. The digital supplies are decoupled from the analog supplies with a 10 $\Omega$  resistors to minimize the effects of digital noise in the converter.

*The positive digital power supply of the CS5323 must never exceed either positive analog supply by more than a diode drop, or the CS5323 could experience permanent damage.* If separate supplies are used for the analog and digital sections of the chip, care must be taken that the analog supply comes up first at power-up. Additionally, the power supplies to the CS5323 should be active before the reference current generator supplies the IREF input current.

The maximum voltage differential between the positive digital supply of the CS5323 and the positive digital supply of the CS5322 must be less than 0.25V. Operation beyond this constraint may result in loss of analog performance in the CS5322 and CS5323 chip set.

Many seismic or sonar systems are battery powered, and utilize dc-dc converters to generate the necessary supply voltages for the system. To minimize the effects of power supply interference, it is desirable to operate the dc-dc converter at a frequency which is rejected by the digital filter.

To achieve maximum performance, the dc-dc converter operating frequency should be located below 48 kHz (see Power Supply Rejection). A synchronous dc-dc converter, whose operating frequency is derived from the 1.024 MHz clock used to drive the CS5322, will minimize the potential for "beat frequencies" appearing in the dc to  $f_1$  Hz passband.



3

## CS5322 PIN DESCRIPTIONS

### Power Supplies

#### VD+ – Positive Digital Power, PIN 8,21

Positive digital supply voltage. Nominally +5 volts.

#### DGND – Digital Ground, PIN 9,20

Digital ground reference.

### Digital Outputs

#### MCLK – Modulator Clock Output, PIN 7

A CMOS-compatible clock output (nominally 1.024 MHz) that provides the necessary clock for operation of the modulator.

#### MSYNC – Modulator Sync, PIN 5

The transition from a low to high level on this output will re-initialize the CS5322.

#### ERROR - Error Flag, PIN 23

This signal is the output of an open pull-up NOR gate with a nominal 100 k $\Omega$  pull-up resistor to which the error status data (OVERWRITE error, MFLG error, ACC1 error and ACC2 error) are inputs. When low, it notifies the host processor that an error condition exists. The ERROR signal can be wire OR'd together with other filters' outputs. The value of the internal pull-up resistor is 100 k $\Omega$ .

**DRDY - Data Ready, PIN 22**

When high, data is ready to be shifted out of the serial port data register.

**SOD - Serial Output Data, PIN 24**

The output coding is 2's complement with the data bits presented MSB first, LSB last. Data changes on the rising edge of SCLK. An internal nominal 100 k $\Omega$  pull-up resistor is included.

**Digital Inputs****MDATA – Modulator Data, PIN 10**

Data will be presented in a one-bit serial data stream at a bit rate of 256 KHz; (CLKIN = 1.024 MHz).

**TDATA - Test Data, PIN 11**

Input for user test data.

**MFLG – Modulator Flag, PIN 6**

A transition from a low to high level signals that the CS5323 modulator is unstable due to an over-range on the analog input. A Status Bit will be set in the digital filter indicating an error condition. An internal nominal 100 k $\Omega$  pull-down resistor included on the input pin.

**RESET - Filter Reset, PIN 4**

Performs a hard reset on the chip, all registers and accumulators are cleared. All signals to the device are locked out except CLKIN. The error flags in the Status Register are set to zero and the Data Register and Offset Register are set to zero. The configuration register is set to the values of the corresponding input pins. SYNC must be applied to resume convolutions after RESET deasserts.

**CLKIN - Clock Input, PIN 3**

A CMOS-Compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation the modulator and filter.

**SYNC - Frame Sync, PIN 2**

Conversion synchronization input. This signal synchronizes the start of the filter convolution. More than one SYNC signal can occur with no effect on filter performance, providing the SYNC signals are perfectly timed at intervals equal to the output sample period.

**CSEL - Channel Select, PIN 12**

When high, information on the TDATA pin is presented to the digital filter. A low causes data on the MDATA input to be presented to the digital filter.

**PWDN - Powerdown, PIN 14**

Powers down the filter when taken high. Convolution cycles in the digital filter and the MCLK signal are stopped. The registers maintain their data and the serial port remains active. SYNC must be applied to resume convolutions after PWDN deasserts.

**DECA - Decimation Rate Control , PIN 18**

See Table 3.

**DECB - Decimation Rate Control , PIN 17**

See Table 3.

**DECC - Decimation Rate Control, PIN 16**

See Table 3.

**H/S - Hardware/Software Mode Select, PIN 13**

When high, the device pins control device operation; when low, the value entered by a prior configuration write controls device operation.

**CS - Chip Select, PIN 1**

When high, all signal activity on the SID, R/W and SCLK pins is ignored. The DRDY and ERROR signals indicate the status of the chip's internal operation.

**R/W - Read/Write, PIN 28**

Used in conjunction with CS such that when both signals are low, the filter inputs data from the SID pin on the falling edge of SCLK. If CS is low and R/W is high, the filter outputs data on the SOD pin on the rising edge of SCLK. R/W low floats the SOD pin allowing SID and SOD to be tied together, forming a bidirectional serial data bus.

**SCLK - Serial Clock, PIN 26**

Clock signal generated by host processor to either input data on the SID input pin, or output data on the SOD output pin. For write, data must be valid on the SID pin on the falling edge of SCLK. Data changes on the SOD pin on the rising edge of SCLK.

**SID - Serial Data Input, PIN 25**

Data bits are presented MSB first, LSB last. Data is latched on the falling edge of SCLK.

**RSEL - Register Select, PIN 27**

Selects conversion data when high, or status data when low.

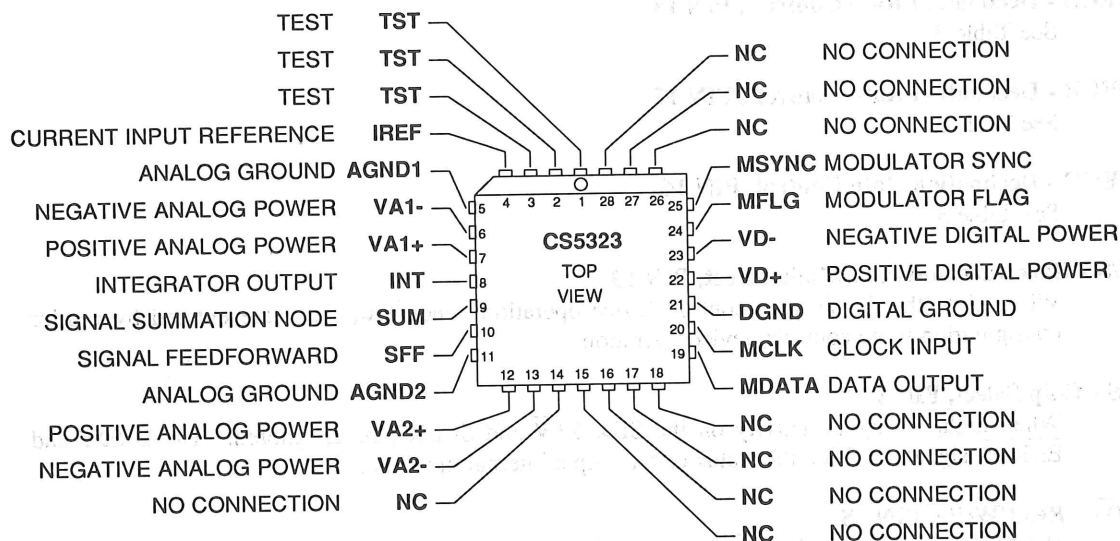
**USEOR - Use Offset Register, PIN 15**

Use offset register value to correct output words when high. Output words will not be offset corrected when low.

**ORCAL - Offset Register Calibrate, PIN 19**

Initiates an offset calibration cycle when ORCAL is high when SYNC goes high after a RESET. The offset value is output on the 57th word following SYNC. Subsequent words will have their offset correction controlled by USEOR.





## CS5323 PIN DESCRIPTIONS

### Power Supplies

#### VA1+, VA2+ – Positive Analog Power, PINS 7, 12

Positive analog supply voltage. Nominally +5 Volts.

#### VA1-, VA2- – Negative Analog Power, PINS 6, 13

Negative analog supply voltage. Nominally -5 Volts.

#### AGND1, AGND2 – Analog Ground, PINS 5, 11

Analog ground reference.

#### VD+ – Positive Digital Power, PIN 22

Positive digital supply voltage. Nominally +5 Volts.

#### VD- – Negative Digital Power, PIN 23

Negative digital supply voltage. Nominally -5 Volts.

#### DGND – Digital Ground, PIN 21

Digital ground reference.

**Analog Inputs****IREF – Current Input Reference Node, PIN 4**

This node accepts a 1 mA reference current to set the signal gain of the A/D converter.

**SFF – Signal Feedforward, PIN 10**

The input signal is fed forward around the integrator input stage by means of this input pin. This maximizes signal performance.

**SUM – Signal Summation node, PIN 9**

This is the input integrator virtual ground summing junction. The external integrator input resistor and integrating capacitor are connected to this node, along with a 250  $\mu$ A bias current network.

**INT – Integrator Output, PIN 8**

Output pin of the input integrator stage. The external integrating capacitor is connected to this pin for proper operation.

**Digital Inputs****MCLK – Clock Input, PIN 20**

A CMOS-compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation of the modulator, digital filter and data output portions of the A/D converter.

**MSYNC – Modulator Sync, PIN 25**

A transition from a low to high level on this input will re-initialize the CS5323. MSYNC resets a divide-by-four counter to align the output bit stream from the CS5323 for proper input to the CS5322.

**Digital Outputs****MDATA – Modulator Data Output, PIN 19**

Data will be presented in a one-bit serial data stream at a bit rate of 256 kHz.

**MFLG – Modulator Flag, PIN 24**

A transition from a low to high level signals that the CS5323 modulator is unstable due to an over-range on the analog input. A Status Bit will be set in the digital filter indicating an error condition.

**Miscellaneous****TST – Test, PINS 1,2,3**

Reserved for production test facility. Should be tied to DGND for normal operation.

**NC – No Connection, PINS 14,15,16,17,18,26,27,28**

No internal connection. Tie to ground for optimum operation.

## **PARAMETER DEFINITIONS**

### **Dynamic Range**

The ratio of the full-scale (rms) signal to the broadband (rms) noise signal. Broadband noise is measured with the input grounded within the bandwidth of 1 Hz to  $f_3$  Hz. Units in dB.

### **Signal-to-Distortion**

The ratio of the full-scale (rms) signal to the rms sum of all harmonics up to  $f_3$  Hz. Units in dB.

### **Intermodulation Distortion**

The ratio of the rms sum of the two test frequencies (50 and 70 Hz) which are each 6 dB down from full-scale to the rms sum of all intermodulation components within the the bandwidth of dc to  $f_3$  Hz. Units in dB.

### **Full Scale Error**

The ratio of the difference between the value of the voltage reference and analog input voltage to the full scale span (two times the voltage reference value). This ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted. Measurement of this parameter uses the circuitry illustrated in the System Connection Diagram. Units in %.

### **Full Scale Drift**

The change in the Full Scale value with temperature. Units in  $\%/^{\circ}\text{C}$ .

### **Offset**

The difference between the analog ground and the analog voltage necessary to yield an output code from the CS5323/22 of 000000(H). Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in mV.

### **Offset Drift**

The change in the Offset value with temperature. Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in  $\mu\text{V}/^{\circ}\text{C}$ .

## Evaluation Board for CS5322 & CS5323

### Features

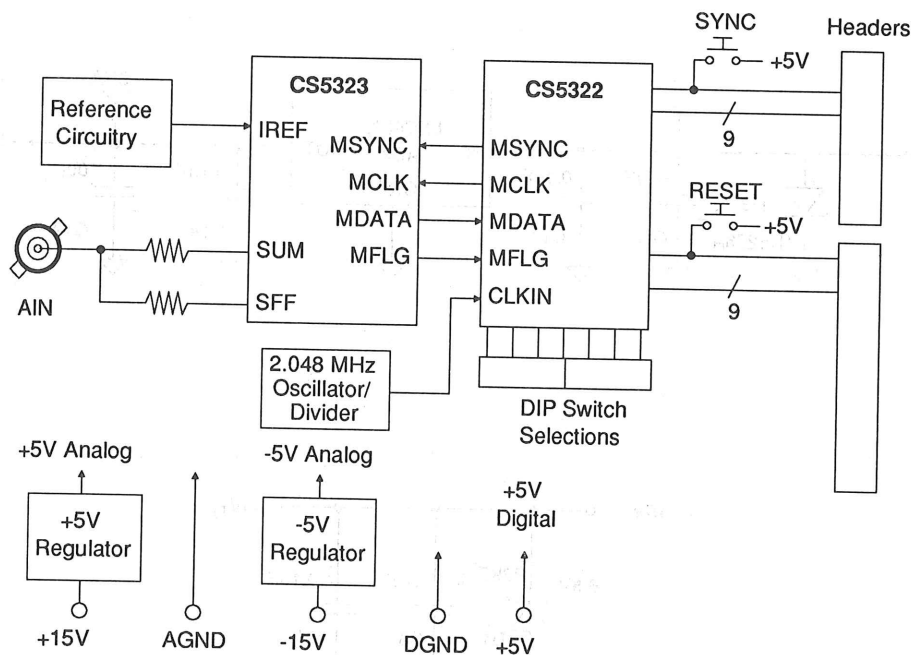
- DIP switch control of all CS5322 logic pins
- Header control of all CS5322 logic pins
- Supports manual operation of RESET and SYNC

### General Description

The CDB5322/3 is an evaluation board that allows laboratory characterization of the CS5322/CS5323 A/D converter chip-set. The chip-set supports seven different selectable word rates: 4 kHz, 2 kHz, 1 kHz, 500 Hz, 250 Hz, 125 Hz and 62.5 Hz. Input to the board is 20 volts peak-to-peak. Output is via header connections to the CS5322 serial interface.

Ordering Information: CDB5322/3

3



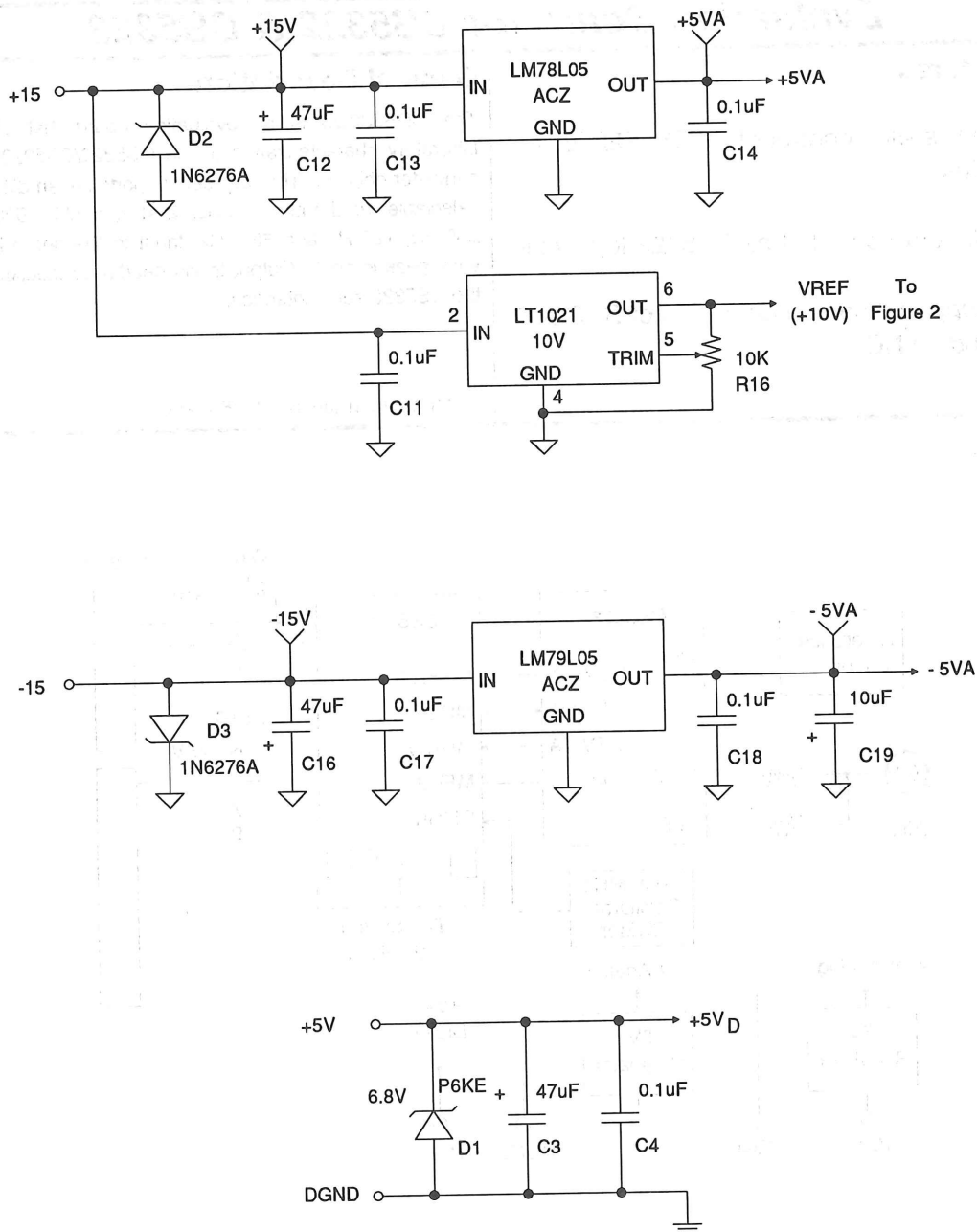


Figure 1. Power Supplies



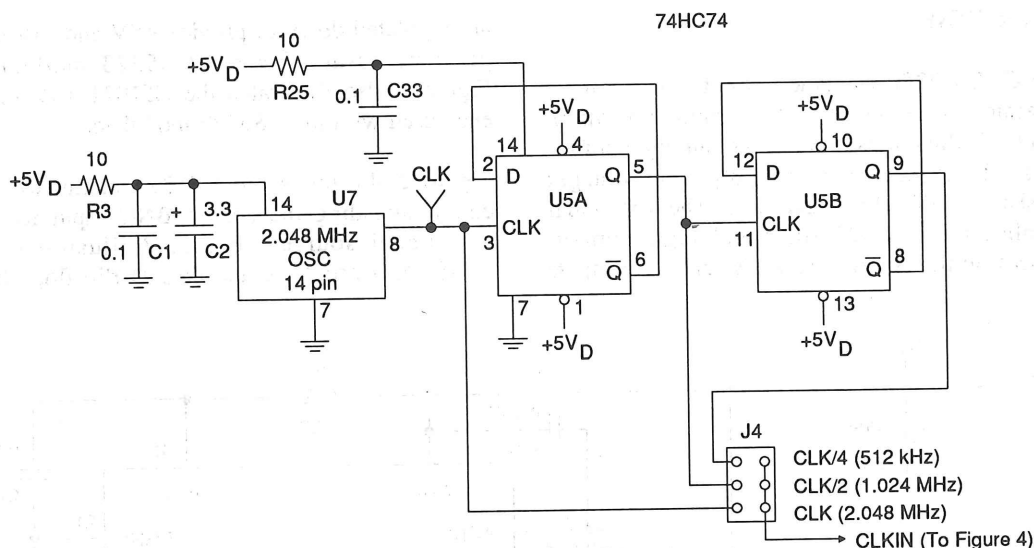


Figure 3. Oscillator / Divider

divider. Note that both the oscillator and the divider are separately decoupled from the +5V supply to reduce clock jitter which can be introduced from noisy supplies. Jumper J4 should be set in the CLK/2 position to source 1.024 MHz to the CS5322 chip for normal operation. If operation from 512 kHz clock is desired, the J4 jumper should be changed to the CLK/4 position. The board can be tested at 512 kHz without modification. In production applications, the CS5323 integrator capacitor (C24) should be doubled to 5.6 nF for 512 kHz operation to achieve optimum performance.

The digital interface pins to the CS5322 filter chip are all available on the header connectors J1, J2, and J3 as shown in Figures 4, and 5. Note that one row of pins on each of the headers is ground. It is advised that any connections made to control lines be done with twisted pair ribbon cable; with each twisted pair containing one signal and one ground connection. This minimizes radiated noise.

### CAUTION!

Caution is advised when interfacing the evaluation board to any circuitry powered from another source. For example, when interfacing to a computer I/O card be sure that the evaluation board and the computer are both powered up before connecting to the evaluation board headers. Always disconnect header connections when powering down the board but not the computer. Failure to follow this advice may cause damage to either the computer I/O or to the CS5322, because the computer outputs try to power the CDB5322/23 board.

Tables 1 and 2 illustrate the DIP switch positions of switches S3 and S4. The switch positions with asterisks indicate preferred settings for driving the interface of Figure 6.





USEOR	ON*	Do not use offset register
	OFF	Use offset register
ORCAL	ON*	Disable offset register calibration
	OFF	Enable offset register calibration
SID	ON	Sets SID to Logic 0
	OFF*	Allows pull-up on SID line
ERR	ON	Sets ERR to logic 0
	OFF*	Allows CS5322 ERROR output
RSEL	ON	Select status register
	OFF*	Select conversion data register
CS	ON*	Chip select active
	OFF	Chip select inactive
R/W	ON	Enables write mode via SID pin
	OFF*	Enables read mode via SOD pin

OFF = OPEN = 1

\*Default to use Figure 6 interface.

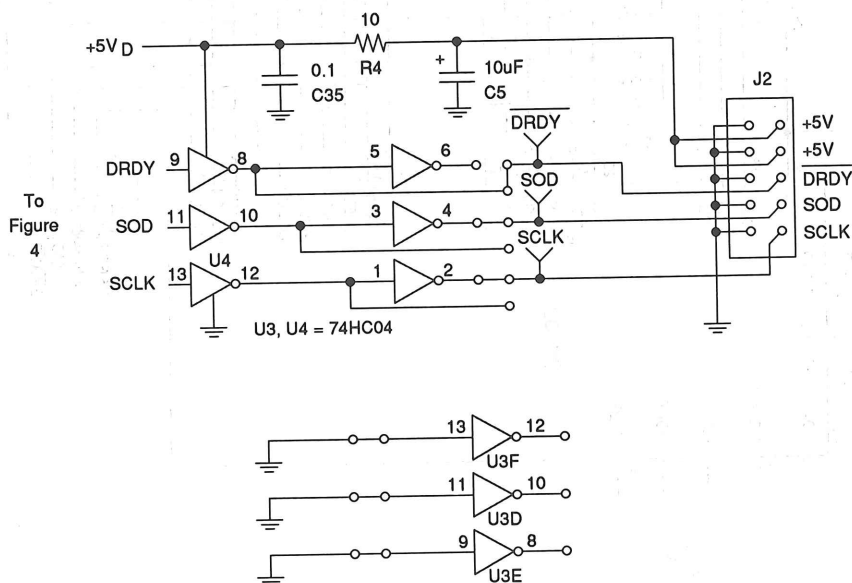
DECA	ABC	Output Word Rate
DECB	0 0 0	62.5
	1 0 0	125
	0 1 0	250
	1 1 0	500
DECC	0 0 1	1000
	1 0 1	2000
	0 1 1	4000
PWDN	ON*	Normal Operation
	OFF	Power down active
H/S	ON	Selects configuration register for operating mode
	OFF*	Select hardware pins for operating mode
CSEL	ON*	Selects MDATA from modulator
	OFF	Selects TDATA as filter input
TDATA	ON*	Sets TDATA input to logic 0
	OFF	Enables TDATA from J1 header

OFF = OPEN = 1

\*Default to use Figure 6 interface.

**Table 1. S3 DIP Switch Selections**

**Table 2. S4 DIP switch selections**



**Figure 5. Serial Latch Interface**

Figure 5 illustrates the logic used to drive connections at header J2.

By using the signals at header J2, the evaluation board can be set up to output its conversion words into three 74HC595 serial to parallel registers. This provides 24-bit parallel data. Figure 6 illustrates the circuitry which can be interfaced to the J2 connections to provide an isolated digital interface to three 74HC595 registers (the circuitry of Figure 6 is not provided on the board). Signals from connector J2 (+5 volts, GND, SCLK, SOD, and DRDY) are interfaced to the GND1 side of the opto-isolated interface. The 74HC595 registers require SCLK rising to latch data bits and DRDY rising to parallel latch data. Jumpers must be placed to select the proper phase of these signals as the CS5322 provides data bits to be latched by the falling edge of SCLK and causes DRDY to fall when the last data bit is clocked out. A flip-flop is used to delay DRDY by one-half SCLK cycle before it is used to latch the parallel latch. Jumper J6 (CLK) is used to connect the 1.024 MHz clock as the SCLK signal to clock serial data from the chip. A second isolated +5 volts should be provided to the GND2 side of the interface. Opto-isolation eliminates any ground loop between the board and the computer interface.

The CS5322 filter should be set up for hardware mode ( $H/\bar{S}$  on switch S4 open). DIP switch S4 can then be used to select the desired output word rate. After the selection on the DECA, DECB, and DECC positions of the S4 DIP switch, the S2 RESET switch must be activated, followed by the S1 SYNC switch (unless these signals are controlled via the J1 and J3 header signals).

Figure 7 illustrates the component layout of the board while figures 8 and 9 illustrate the board layout (not to scale).

## Using the Evaluation Board

Connect the appropriate power supplies to the binding posts of the board. Twist the +5V digital supply lead with the digital ground lead from the board to the supply. Also twist the supply leads for the analog voltages. Use a high quality power supply which is low in noise and line frequency(50/60 Hz) interference.

Power up the supplies. Then connect a coaxial cable from the analog BNC to the signal source. Note that the performance of the A/D converter chip set will exceed the capability of most signal generators, especially with respect to noise and line frequency interference.

Once power has been applied to the board, connect the ribbon cable to the appropriate headers (J1, J2, and/or J3). The reset and the sync signals to the CS5322 must be applied before normal operation can commence. This can be done by using the S2 RESET switch and the S1 SYNC switch or by interfacing to these signals via the J1 and J3 headers.

3

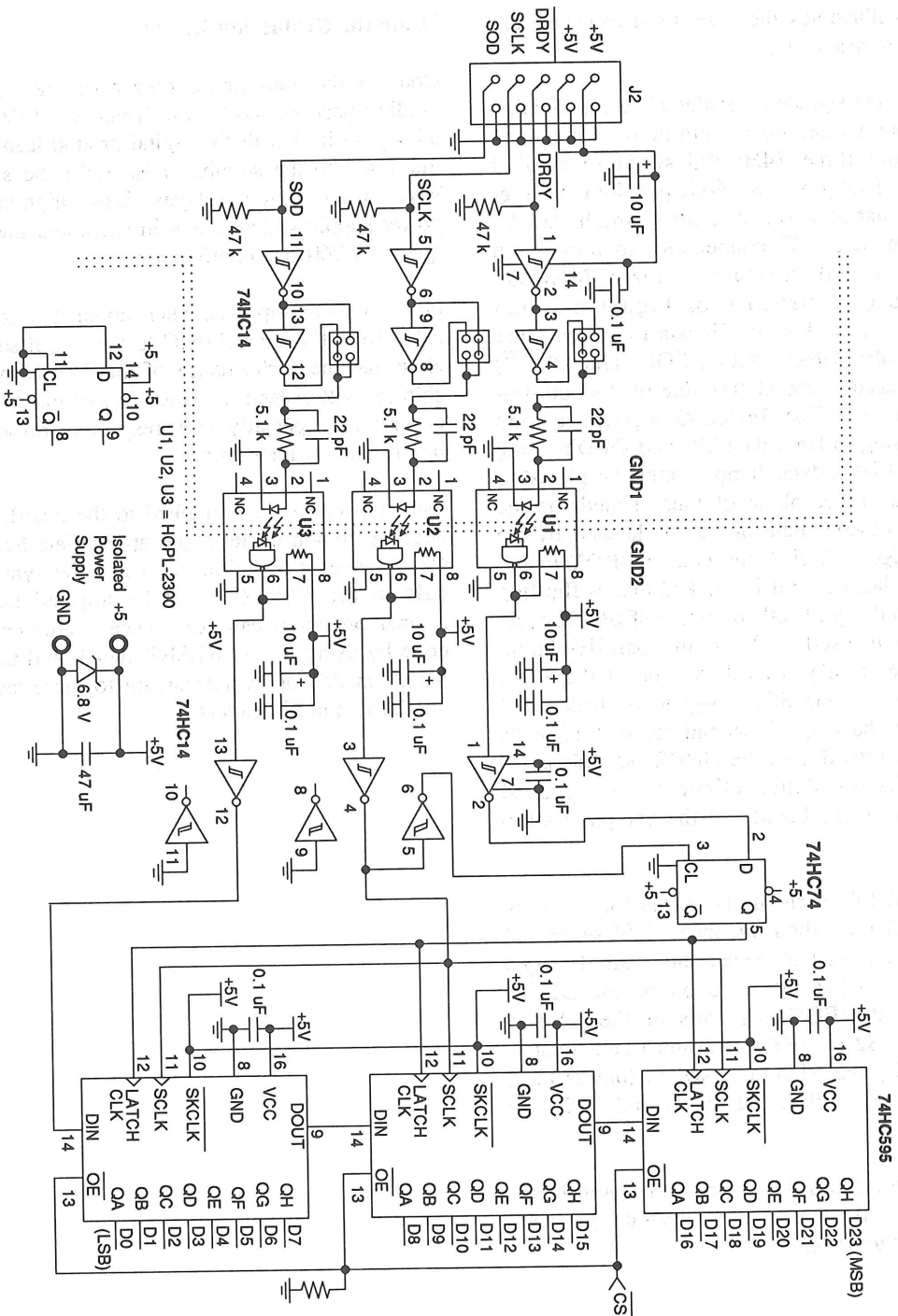


Figure 6. Suggested Opto-coupled Interface Between A/D and Serial-to-parallel Registers (Not Provided)

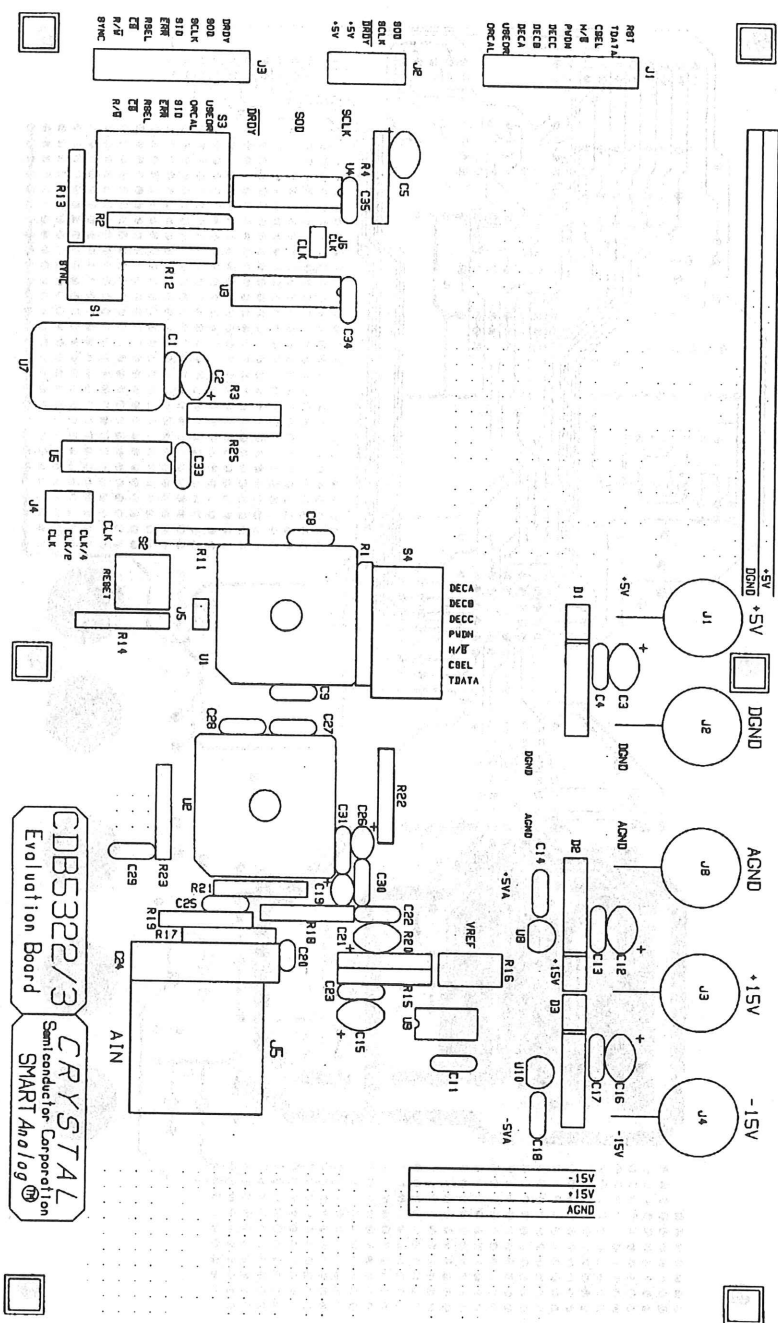


Figure 7. CDB5322 Component Layout (Not to Scale)

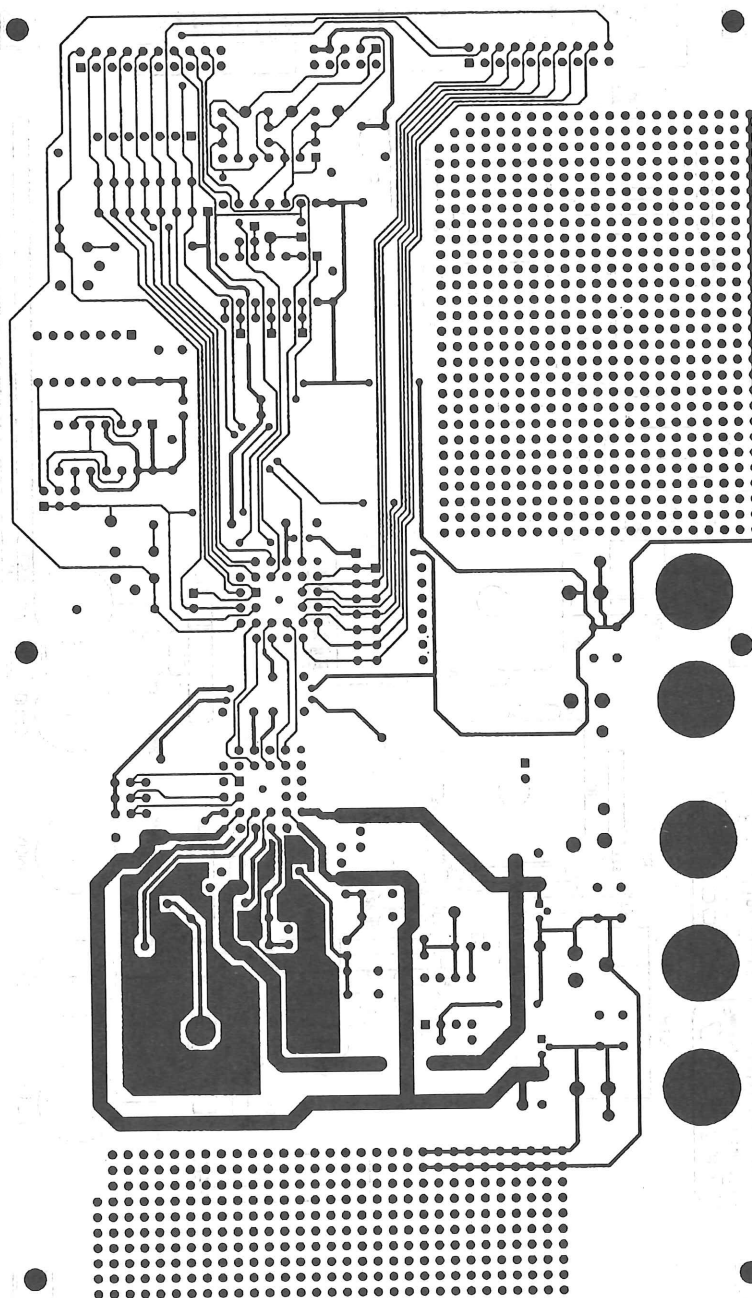


Figure 8. CDB5322/3 Solder Trace Layer (Not to Scale)

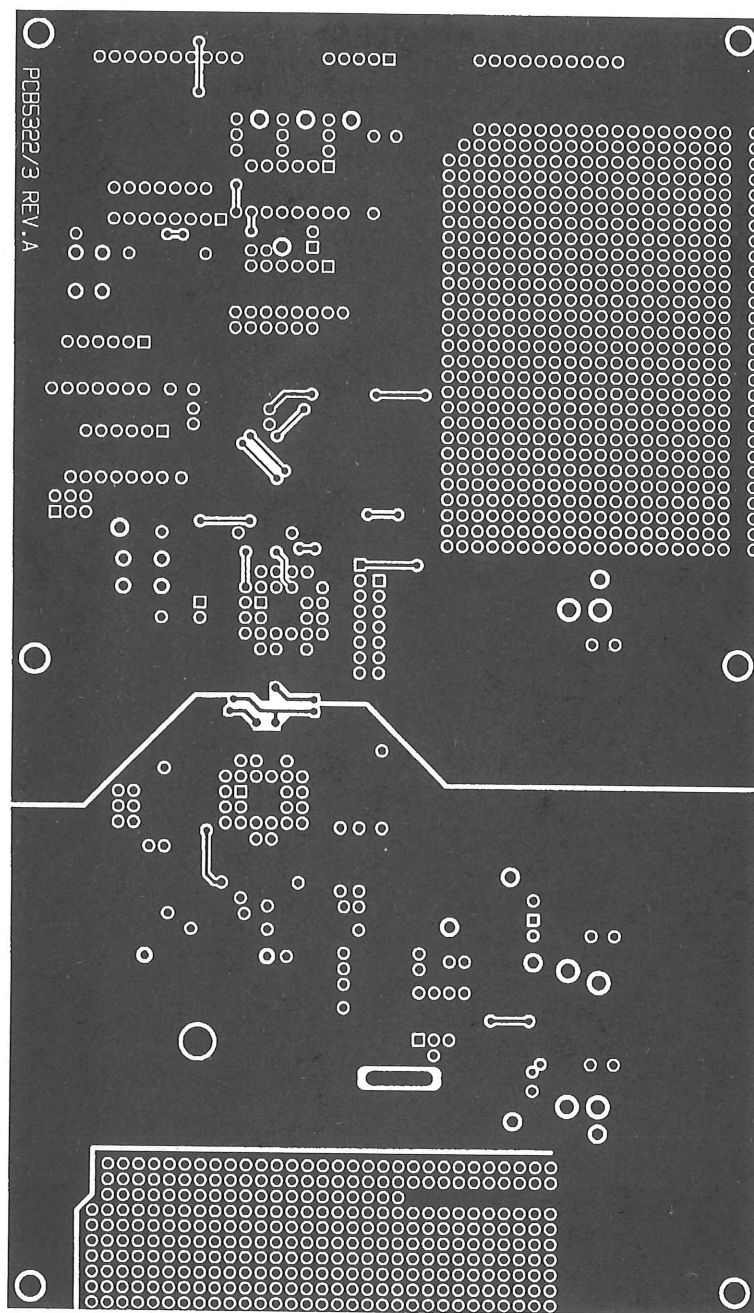


Figure 9. CDB5322/3 Ground Plane Layer (Not to Scale)



**•Notes•**

# 120 dB, 500 Hz Oversampling A/D Converter

## Features

- Monolithic CMOS A/D converter
- 120dB Dynamic Range
- dc-500 Hz Bandwidth
- 110 dB Total Harmonic Distortion
- Internal Track-and-Hold Amplifier
- Delta-Sigma Architecture
  - 256X Oversampling
  - Linear Phase Digital Filter
  - Output Word Rate 32 kHz
- Low Power Dissipation: 150 mW
- Evaluation Board Available

## General Description

The CS5324 analog to digital converter is a unique, very high resolution A/D converter intended for geophysical and sonar applications. It is a complete analog front end to a Digital Signal Processor and provides the DSP with a low distortion digital input suitable for precision signal analysis. The CS5324 performs sampling, A/D conversion, and anti-alias filtering.

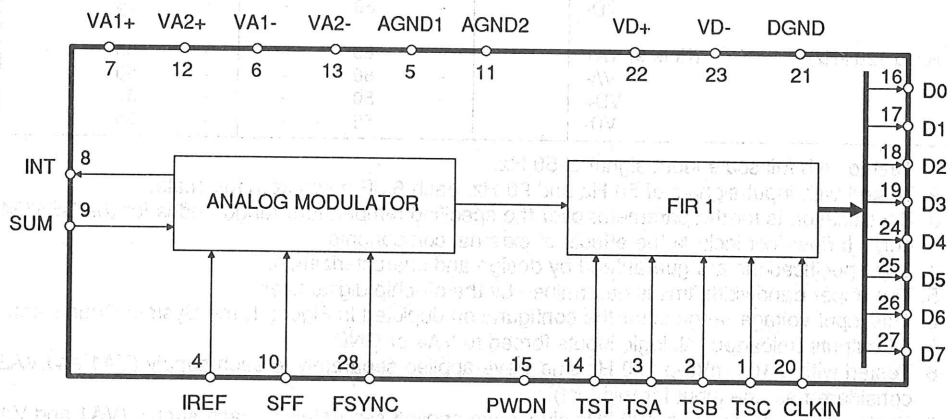
The CS5324 uses delta-sigma modulation to produce highly accurate conversions. The device oversamples at 256X, virtually eliminating the need for external anti-aliasing filters. An on-chip linear-phase FIR digital filter decimates the output to a 32 kHz output word rate. Data is transmitted to the DSP as two, 8-bit bytes. An additional FIR filter in the DSP further decimates the signal to achieve 120 dB dynamic range over 500 Hz bandwidth with signal-to-distortion of 110 dB.

The CMOS design of the CS5324 ensures high reliability and power dissipation of less than 180 mW.

### ORDERING GUIDE:

CS5324-KL	0° to 70°C	28-pin PLCC
CS5324-BL	-40° to +85°C	28-pin PLCC
CDB5324	Evaluation Board	

## Block Diagram



### Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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(512) 445-7222 Fax: (512) 445-7581

August '91  
DS36PP3  
3-175

**ANALOG CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ;  $V_A = -5\text{V}$ ;  $V_A = 5\text{V}$ ;  $\text{AGND} = 0\text{V}$ ;  $\text{CLKIN} = 1.024\text{ MHz}$  Device is connected as shown in Figure 1, the System Connection Diagram. Output data is further processed using off-chip filtering described in Appendix 1.)

Parameter	Symbol	CS5324-K			CS5324-B			Units
		Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range		0	-	+70	-40	-	+85	$^\circ\text{C}$
<b>Dynamic Performance</b>								
Dynamic Range	DR	116	120	-	116	120	-	dB
Signal-to-Distortion (Note 1)	SDR	100	110	-	100	110	-	dB
Intermodulation Distortion (Note 2)		-	110	-	-	110	-	dB
<b>dc Accuracy</b>								
Full Scale Error (Note 3)		-	-	2	-	-	2	%
Full Scale Drift (Note 3, 4)		-	0.003	0.006	-	0.003	0.006	$\% / ^\circ\text{C}$
Offset (Note 3)		-	-	250	-	-	250	mV
Offset Drift (Note 3, 4)		-	500	750	-	500	750	$\mu\text{V} / ^\circ\text{C}$
<b>Input Characteristics</b>								
Input Signal Frequencies (Note 5)	BW	dc	-	500	dc	-	500	Hz
Input Voltage Range (Note 6)	$V_{\text{in}}$	-10.0	-	+10.0	-10.0	-	+10.0	V
<b>Power Supplies</b>								
DC Power Supply Currents (Note 7)		-	12.5	18	-	12.5	18	mA
Positive Supplies		-	14.5	18	-	14.5	18	mA
Negative Supplies		-	14.5	18	-	14.5	18	mA
Power Dissipation (Note 7)		-	150	180	-	150	180	mW
PWDN Low		-	5	10	-	5	10	mW
PWDN High		-	5	10	-	5	10	mW
Power Supply Rejection (dc to 500 Hz) (Note 8)	$V_A+$	-	55	-	-	55	-	dB
	$V_A-$	-	45	-	-	45	-	dB
	$V_D+$	-	48	-	-	48	-	dB
	$V_D-$	-	38	-	-	38	-	dB
(500 Hz to 128 kHz) (Note 9)	$V_A+$	-	60	-	-	60	-	dB
	$V_A-$	-	60	-	-	60	-	dB
	$V_D+$	-	50	-	-	50	-	dB
	$V_D-$	-	55	-	-	55	-	dB

- Notes:
1. Tested with full scale input signal of 50 Hz.
  2. Tested with input signals of 50 Hz and 90 Hz, each 6 dB down from full scale.
  3. Specification is for the parameter over the specified temperature range and is for the CS5324 device only. It does not include the effects of external components.
  4. Drift specifications are guaranteed by design and characterization.
  5. The upper bandwidth limit is determined by the off-chip digital filter.
  6. This input voltage range is for the configuration depicted in Figure 1, the System Connection Diagram.
  7. All outputs unloaded. All logic inputs forced to  $V_A+$  or GND.
  8. Tested with a 100 mVp-p 120 Hz sine wave applied separately to each supply ( $V_A1$  and  $V_A2$  are considered as one input for this test).
  9. Tested with a 100 mVp-p 120 kHz sine wave applied separately to each supply ( $V_A1$  and  $V_A2$  are considered as one input for this test).

\* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

# SWITCHING CHARACTERISTICS

( $T_A = T_{min}$  to  $T_{max}$ ;  $V_{A+}, V_{D+} = 5V \pm 5\%$ ;  $V_{A-}, V_{D-} = -5V \pm 5\%$ ;  
Inputs: Logic 0 = 0V Logic 1 =  $V_{D+}$ ;  $C_L = 50pF$ . See Note 13.)

Parameter	Symbol	Min	Typ	Max	Units
CLKIN Frequency (Note 10)	$f_c$	0.9	1.024	1.1	MHz
CLKIN Duty Cycle		40	-	60	%
CLKIN Jitter		-	-	5	ps
Rise Times: Any Digital Input (Note 11)	$t_{rise}$	-	-	1.0	us
Any Digital Output (Note 11)		-	50	200	ns
Fall Times: Any Digital Input (Note 11)	$t_{fall}$	-	-	1.0	us
Any Digital Output (Note 11)		-	50	200	ns
CLKIN Rising edge to FSYNC Rising (Note 12)	$t_{cf}$	70	-	-	ns
FSYNC Rising to CLKIN Falling Edge	$t_{fc}$	150	-	-	ns
Output Data Delay: CLKIN Rising to Valid Data	$t_{dd}$	-	200	TBD	ns
Output Float Delay: CLKIN Rising to Hi-Z	$t_{fd}$	-	150	TBD	ns

Notes: 10. If CLKIN is removed the device will enter the power down mode.

11. Excludes CLKIN input. CLKIN should be driven with a signal having rise and fall times of 25ns or faster

12. Only the rising edge of FSYNC relative to CLKIN is used to synchronize the device. FSYNC can return low at any time as long as it remains high for at least one CLKIN cycle.

13. Guaranteed by design, characterization and/or test.

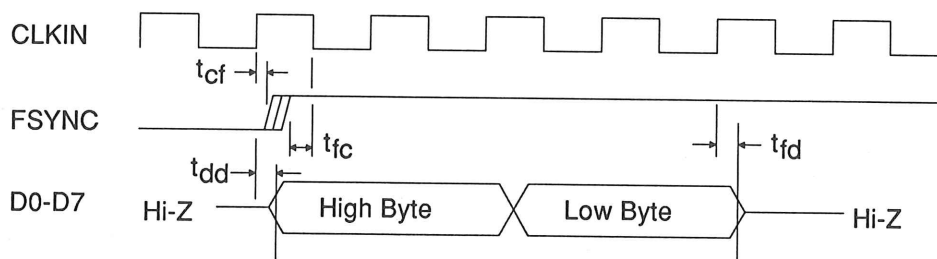
# DIGITAL CHARACTERISTICS

( $T_A = T_{min}$  to  $T_{max}$ ;  $V_{A+}, V_{D+} = 5V \pm 5\%$ ;  $V_{A-}, V_{D-} = -5V \pm 5\%$ )

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	$V_{IH}$	$(V_{D+}) - 1.0V$	-	-	V
Low-Level Input Voltage	$V_{IL}$	-	-	1.0	V
High-Level Output Voltage $I_{OUT} = -600 \mu A$ (Note 14)	$V_{OH}$	$(V_{D+}) - 0.4V$	-	-	V
Low-Level Output Voltage $I_{OUT} = 800 \mu A$ (Note 14)	$V_{OL}$	-	-	0.4	V
Input Leakage Current	$I_{LKG}$	-	-	$\pm 10$	$\mu A$
Tri-State Leakage Current	$I_{OZ}$	-	-	$\pm 10$	$\mu A$
Digital Output Pin Capacitance	$C_{OUT}$	-	9	-	pF

Notes: 14. The device is designed for low current output drive to minimize induced noise. CMOS interfacing is highly recommended.



Digital Timing Relationships

**RECOMMENDED OPERATING CONDITIONS** (DGND=0V; AGND=0V. All voltages measured with respect to ground.)

Parameter	Symbol	Min	Typ	Max	Units
DC Supply					
Positive Analog	VA+	4.75	5.0	5.25	V
Negative Analog	VA-	- 4.75	- 5.0	- 5.25	V
Positive Digital	VD+	4.75	5.0	5.25	V
Negative Digital	VD-	- 4.75	- 5.0	- 5.25	V

**ABSOLUTE MAXIMUM RATINGS** (DGND=0V; AGND=0V. All voltages measured with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supplies:				
Positive Digital	VD+	- 0.3	(VA+) + 0.3	V
Negative Digital	VD-	0.3	- 6.0	V
Positive Analog	VA+	- 0.3	6.0	V
Negative Analog	VA-	0.3	- 6.0	V
Input Current, Any Pin Except Supplies ( Note 15)	I <sub>in</sub>	-	±10	mA
Digital Input Voltage	V <sub>IND</sub>	- 0.3	(VA+) + 0.3	V
Ambient Operating Temperature	T <sub>A</sub>	- 55	125	°C
Storage Temperature	T <sub>stg</sub>	- 65	150	°C

Note: 15. Transient currents up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

### General Description

The CS5324 is a monolithic CMOS A/D converter designed specifically for very high resolution measurement of signals between dc and 500 Hz. The device consists of a fourth-order delta-sigma modulator followed by an on-chip digital decimation filter.

The modulator of the CS5324 samples the analog input signal at a 256X oversampling rate. This high oversampling rate, along with subsequent digital filtering, enables the CS5324 to achieve a dynamic range which exceeds 120dB. To achieve optimum performance, the CS5324 uses off-chip circuitry to develop the reference and operating currents necessary to set the gain and offset of the modulator portion of the A/D converter. Discrete components are also used for the first stage integrator input resistor and integration capacitor.

The CS5324 performs conversions continuously and outputs twelve data bits for further data decimation by an off-chip digital filter. A separate DSP chip can be utilized to perform the off-chip filtering. A single DSP chip can perform the filter function for several CS5324 devices. For this reason, the CS5324 was designed to output its data in a simple time-division multiplexing (TDM) format. This TDM architecture allows up to eight CS5324 devices to share the same data bus.

### Theory of Operation

The CS5324 utilizes a fourth order oversampling delta-sigma architecture to achieve high-resolution A/D conversion. The converter consists of an analog modulator, along with an on-chip digital decimation filter. The modulator consists of a 1-bit A/D converter embedded in a negative feedback loop. The first stage of the fourth order modulator uses discrete components external to the chip to maximize signal performance relative to noise.

The modulator samples at 256 kHz (CLKIN = 1.024 MHz) which is 256X oversampling above two times the maximum signal frequency of 500 Hz. The modulator output is followed by a decimate by 8, fourth-order (sinx)/x filter. The result from this filter is a 12-bit word which is output from the chip at a 32 kHz rate. The 12-bit data is then further filtered by means of an off-chip digital filter. The off-chip filter can be implemented by either a DSP chip or an ASIC designed for this purpose. The exact characteristics of the on-chip filter and some recommended off-chip digital filters are discussed under the Filter Characteristics section of the data sheet. Upon reduction with the off-chip filtering, the data results in resolution which exceeds 20-bits. The final result yields a dynamic range exceeding 120 dB.

The architecture of the CS5324 was chosen to maximize performance. The input integrator uses off-chip discrete components. The chip is designed to use a current-source type reference, rather than a voltage source to minimize noise. In addition, the amount of on-chip digital filtering is minimized to reduce the possibility of the digital noise of the filter coupling into the analog sections of the chip. Configuring the chip to use additional off-chip digital filtering also allows the user maximum flexibility in implementing a filter appropriate to his system requirements.

### Signal Input and Current Reference

The CS5324 uses a number of external discrete components to achieve maximum performance. Figure 1 illustrates the recommended circuit configuration for the current reference components and for the signal input components.

The CS5324 is designed to use a current reference of 2 mA into the IREF pin. A current reference rather than a voltage reference was chosen to achieve better noise performance. For optimum performance the dc source impedance at the IREF pin should be approximately 5 kΩ. This

calls for a 10 volt source driving the 5 k $\Omega$  (R6+R7) resistor to achieve the desired 2 mA current source. The IREF input sets the full scale gain of the A/D converter.

To properly bias the input integrator to a midrange operating point, a current source 1/4 the size of the IREF input current must be sourced into the integrator summing junction at the SUM pin. This

requires a 20 k $\Omega$  resistance (R4+R5) be placed from the 10 V reference to the SUM pin.

Both the 2 mA IREF current and the 500  $\mu$ A sources have capacitive filtering to aid in reducing the broadband current noise from the voltage reference. These capacitors should be of quality construction. Particular attention should be paid to leakage current variation over the desired

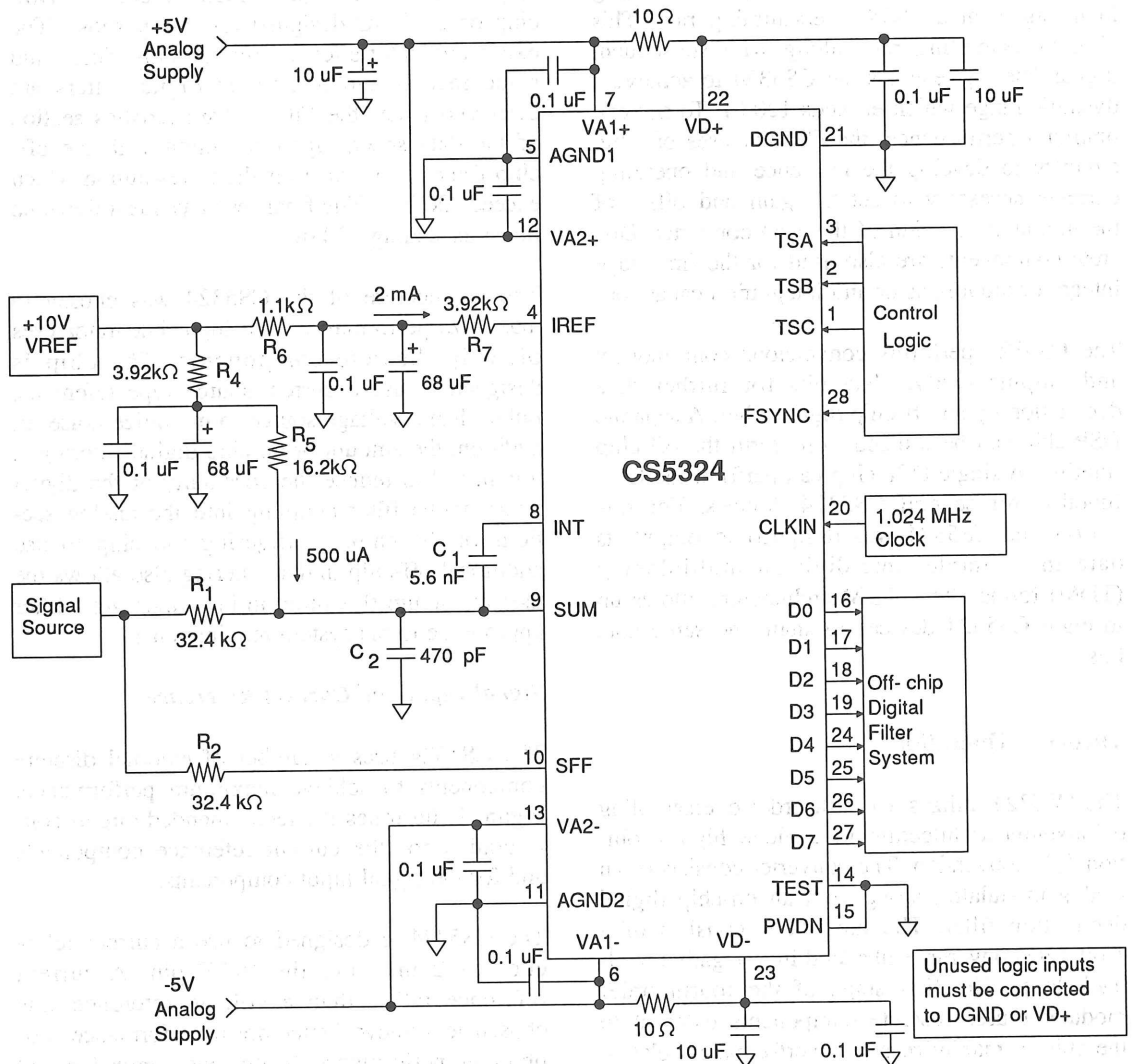


Figure 1. System Connection Diagram



operating temperature, as this leakage will affect the system gain.

The signal input pin (SUM) of the CS5324 is the summing junction of the input integrator stage. This integrator is designed to use an external input resistor (R<sub>1</sub>) and integrating capacitor (C<sub>1</sub>). In addition, a capacitor (C<sub>2</sub>) is required at this node for proper phase compensation. The size of the input resistor (R<sub>1</sub>) is determined by the magnitude of the signal current. With a maximum input voltage into the resistor, the integrator input current must be set equal to approximately 0.15 the current value injected into the IREF pin. With a 2 mA IREF current, the full scale signal current should be about 300  $\mu$ A. Additionally, to minimize current noise into the summing junction, the value of the effective input resistance should be above 8 k $\Omega$ . Using a 32.4 k $\Omega$  resistor for R<sub>1</sub> sets the full scale input voltage into the integrating resistor to a value near 10 volts. The input signal then spans 20 V<sub>p-p</sub>.

Once the integrator input resistor is chosen, the integrator capacitor can be determined. The resistor and capacitor combination should yield a frequency ( $f = 1/(2\pi R_1 C_1)$ ) between 800 and 900 Hz to achieve maximum performance. This yields a capacitor value near 5.6 nF. The capacitor should be chosen for minimum leakage, minimum dielectric absorption, and minimum voltage coefficient of capacitance. While a teflon foilwrap capacitor is preferred, high quality film capacitors may be acceptable in many applications.

The CS5324 has a second signal input pin called the Signal Feedforward (SFF) pin. The signal into this pin bypasses the input stage of the input integrator, improving signal performance in the passband. The resistor (R<sub>2</sub>) used at this input should be identical in value and performance characteristics to the input resistor (R<sub>1</sub>).

### Digital Output and Data Format

For proper operation the CS5324 must be provided with a CMOS-compatible clock into the CLKIN pin. The normal operating frequency is 1.024 MHz. This clock determines the input sample rate and the output word rate of the converter. The sample rate is CLKIN/4 while the output word rate is at CLKIN/32.

The CS5324 will compute a 12-bit output word at a 32 kHz rate (CLKIN = 1.024 MHz). The data is output from Data Output pins D7-D0 in the form of two eight bit bytes. The first byte is the high order byte with the MSB in the D7 position. The second 8-bit byte is the low order byte, and includes three status bits and an unused bit. The data is in two's complement format. Figure 2 illustrates the format of the output data.

For 12-bit two's complement data the codes range from -2048 to +2047. The output codes from the CS5324 will range from approximately -1280 to +1280 for a full scale sine wave input into the converter as shown in Table 1. There may be typically  $\pm 50$  codes of noise (p-p) on the data in the 12-bit data output. Off-chip digital filtering is required to achieve the full dynamic range capability of the CS5324.

	D7	D6	D5	D4	D3	D2	D1	D0
Hi Byte	B11	B10	B9	B8	B7	B6	B5	B4
Lo Byte	B3	B2	B1	B0	0	OF	UF	ORST

Data is 2's complement with B11 as sign bit

Figure 2. Output Data Format

Input Signal	Output Code
approx. +16 V	0111 1111 1111
+F.S. - 1.5 LSB (approx. +10 V)	0101 0000 0000
0V	0000 0000 0000
-F.S. + 0.5 LSB (approx. -10 V)	1011 0000 0000
approx. -16 V	1000 0000 0000

- Notes: 1. Output codes from the on-chip digital filter will typically exhibit  $\pm 50$  LSB's of noise (p-p).  
 2. Table depicts output codes for circuit configuration of Figure 9.

**Table 1. Output Coding**

## Status Bits

Three status bits are output from the CS5324. The three status bits are overflow, underflow, and oscillation reset. The overflow and underflow status bits indicate whenever the digital filter accumulator results in an overflow or underflow condition. With the present on-chip digital filter, the underflow condition will never occur. The overflow bit will go high indicating an accumulator overflow only if the input signal to the converter exceeds positive full scale by approximately 1.6X. Upon overflow, the accumulator will contain the value +2047 (or 2048 after underflow). The oscillation reset status bit indicates that output data may be in error. An oscillation detection circuit monitors the modulator loop to see if it is operating within its stable operating range. If the modulator is operating outside its normal operating range the output data may be corrupted. The ORST status bit may go high as a result of power-up, or, if the input signal exceeds the specified full scale input value. If ORST does occur, it will remain high for a total of four update cycles (of 32 kHz) to the output port, while the modulator and the digital filter are reset. Once ORST goes back low, output data will not be valid until the modulator and the digital filter(s) settle.

## Initialization and Output Data Sequencing

The CS5324 updates its output register at a 32 kHz rate (CLKIN = 1.024 MHz). Between updates 32 CLKIN cycles occur. The CS5324 is designed such that eight data output time slots occur during these 32 CLKIN cycles. Each time slot lasts for 4 CLKIN cycles. The CS5324 is designed to allow eight devices to share the same 8-bit data bus when each device is set-up to output its data in an individual time slot. The exact time the CS5324 will output data is determined by the TSA, TSB, TSC, and FSYNC inputs. After power is applied to the devices, the FSYNC input must be brought high. When FSYNC is brought high (within the required timing specifications), each chip will be assigned to a data output time slot according to the logic levels of its TSA, TSB, and TSC inputs. Table 2 tabulates the decoding of these inputs.

If all the CS5324s in the system are initialized with the same FSYNC signal, they will all compute filter results in phase with each other and update their output registers at the same time. Only the time slot in which the data is output from the devices is different.

The FSYNC signal used to initialize the CS5324 need only be activated once after power up. In some systems, it may be preferable to have this

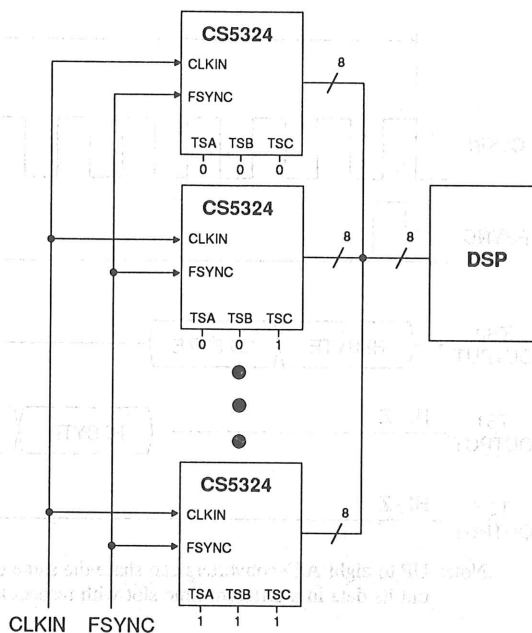
TSA	TSB	TSC	Time Slot
0	0	0	TS0
0	0	1	TS1
0	1	0	TS2
0	1	1	TS3
1	0	0	TS4
1	0	1	TS5
1	1	0	TS6
1	1	1	TS7

**Table 2. Time - Slot Decoding**

signal occur every 32 CLKIN cycles. Only the occurrence of the rising edge of FSYNC is significant in determining the system initialization. Figure 3 illustrates a system configuration using multiple CS5324s interfaced to the same DSP chip.

Four cycles of CLKIN occur during each time slot. During the time slot designated for a CS5324 to output its data, the high-order byte will be output for the first two CLKIN cycles of the time slot. The second byte will be output during the last two CLKIN cycles of the period.

If four or less CS5324's share the same data bus, it is preferable to use alternate time slots (i.e. TS0, TS2, TS4, TS6) to minimize the possibility of bus contention problems. Slight timing differences between chips may result in timing overlap if adjacent time slots are used.



**Figure 3. Multiple CS5324 to DSP Interface.**

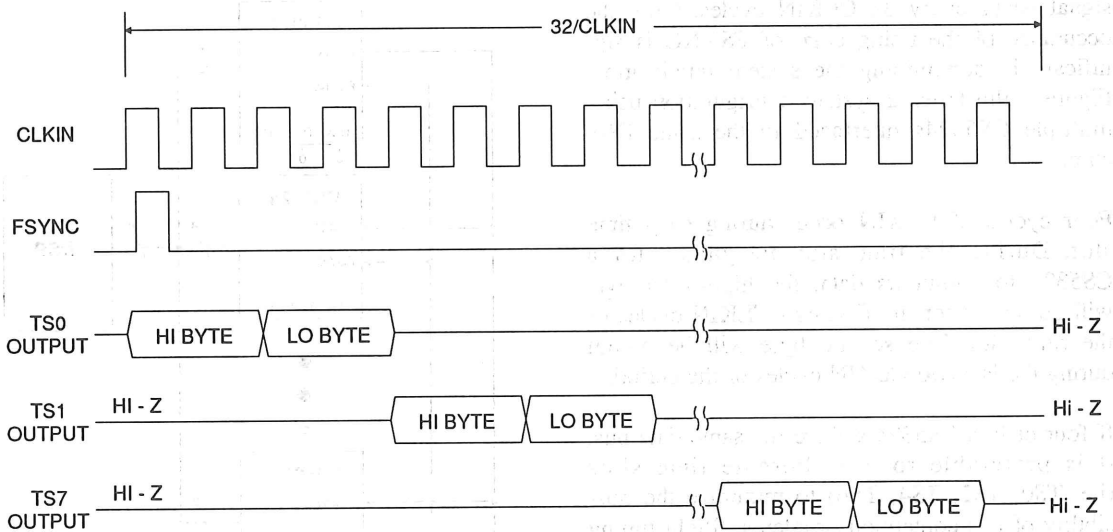
### Filter Characteristics

The CS5324 utilizes a fourth-order delta-sigma modulator which has superb linearity. The full capability of the A/D conversion block can be obtained with an appropriate digital filter. Many applications, (seismic applications in particular) require the A/D conversion function to accurately reproduce the pulse shape of the input signal waveform, not just the spectral content. To accurately digitize the shape of the input signal requires a linear phase response in the signal processing system. Any non-linearities in the phase response of the signal processing system will corrupt the true waveshape information. For this reason, the design of the digital filtering to be used with the CS5324 should include particular attention to the phase characteristics of the filter function.

While the on-chip filter is fixed in its characteristics, the off-chip filter will be defined by the system requirements of the particular application. A low pass filter specification to be used with the

CS5324 will include the following parameters: Passband ripple (or flatness); group delay or phase characteristics; transition band rolloff; stop band rejection; and filter complexity. All of these parameters are interrelated in any given filter design. There is no one particular solution to be used with the CS5324.

The CS5324 samples the input signal at 256 kHz (CLKIN = 1.024 MHz). With a signal bandwidth of 500 Hz, the output data rate from the A/D system (including the off-chip digital filtering) need only be 1 kHz to adequately represent the input signal. For this reason, it is desirable to decimate the 256 kHz sample rate to 1 kHz. To accomplish this while also providing the necessary low-pass filtering, three stages of filtering are utilized. The first of these is the on-chip filter. This filter is a decimate-by-8 function, and reduces the output word rate from the CS5324 chip to 32 kHz. Two



Note: UP to eight A/D converters can share the same digital output bus as long as each converter is assigned to put out its data in a different time slot with respect to all other converters on the bus.

**Figure 4. Data Output Sequence for Multiple CS5324s.**

additional filtering stages are to be implemented off-chip with either a DSP, a dedicated ASIC, or another computing device. The first off-chip stage is a decimate-by-8 function, which reduces the output word rate to 4 kHz. The last stage will be a decimate-by-4 function, which will reduce the word rate to 1 kHz. The filter stages are designed so that the first filter has zeroes in its transfer function, such that it rejects the aliased components, due to the first decimate-by-8. The second stage has zeroes such that it rejects the aliased components due to the second decimate-by-8. Neither the on-chip filter, nor the first off-chip stage really affect the passband, but instead, these two stages reduce the output data rate, while at the same time providing anti-alias filtering. The third stage provides the low-pass filtering function.

The CS5324 includes an on-chip 29th-order linear phase FIR (finite-impulse-response) filter and decimator. The response of this filter is illustrated in Figure 5. The filter coefficients are

listed in Table 3. The filter performs a fourth-order sinc function, and has a monotonic rolloff in the passband. Attenuation at 500 Hz is 0.0137 dB. The minimum attenuation in the  $(n \times 32 \text{ kHz}) \pm 500 \text{ Hz}$  bands is 147 dB. The data output from the on-chip filter has been described in the Data Output and Data Format section above. Data is output at a 32 kHz rate.

The two proposed off-chip filter stages are as follows: The first off-chip stage is a 43rd-order modified sinc FIR filter. Its coefficients are listed in Appendix 1, along with a plot of its transfer function. Attenuation at 500 Hz ( $\text{CLKIN} = 1.024 \text{ MHz}$ ) is 1.47 dB. The minimum attenuation in the  $(n \times 4 \text{ kHz}) \pm 500 \text{ Hz}$  bands is 132 dB.

The second off-chip filter stage is a 301st-order FIR filter that performs the necessary low-pass function, with less than 0.00016 dB ripple in the dc-400 Hz band. Attenuation in the region from 500 Hz to 2 kHz is typically greater than 130 dB. The coefficients for the second off-chip filter

$$X(z) = \sum_{n=0}^{28} h(n+1) z^n$$

Coefficient	Value
h(1) = h(29)	1.00
h(2) = h(28)	4.00
h(3) = h(27)	10.00
h(4) = h(26)	20.00
h(5) = h(25)	35.00
h(6) = h(24)	56.00
h(7) = h(23)	84.00
h(8) = h(22)	120.00
h(9) = h(21)	161.00
h(10) = h(20)	204.00
h(11) = h(19)	246.00
h(12) = h(18)	284.00
h(13) = h(17)	315.00
h(14) = h(16)	336.00
h(15)	344.00

Table 3. On-chip Filter Coefficients

stage are listed in Appendix 1, along with a plot of its transfer function. An alternate final stage filter is also listed in Appendix 1. It is a 201st-order FIR filter and allows more passband ripple (0.07 dB).

If more ripple or less stop band rejection is acceptable, the off-chip filter complexity can be reduced. The filter examples given have been illustrated only as possible filters which can be

utilized with the CS5324 to achieve quality performance from the A/D.

### CS5324 Performance

The CS5324 A/D converter is intended for use in seismic and passive sonar applications. These applications require particularly high dynamic range capability. The CS5324 offers high dynamic range without compromising spectral purity. The CS5324 typically achieves 120 dB of dynamic range, while maintaining signal/distortion at 110 dB.

An A/D converter system using the CS5324 A/D converter as its core was tested using Fast Fourier Transform techniques. The CS5324 was connected using the components as shown in the system connection diagram, Figure 9. Data was collected from the CS5324 with the use of a parallel I/O card in a PC-compatible computer. Software was used to implement the two stage digital filtering function. The output from the digital filtering software was submitted to a windowing algorithm and then to the FFT algorithm. Figure 6 illustrates the performance of the CS5324 when tested with a full scale 113 Hz signal. The CS5324 exhibits some second harmonic but no third harmonic. The test frequency of 113 Hz was selected, as this was the center frequency of a bandpass filter, constructed to reject harmonics and line frequencies present at the output of the signal generator. Note that the performance of the CS5324 will generally exceed the capability of most available sine wave test generators for frequencies between 2-500 Hz, as is the case in Figure 6. The excess noise, in this case, is due to the signal source. Figure 7 illustrates the performance of the CS5324 with a -60 dB 100 Hz input signal. The CS5324 is capable of converting with minimal intermodulation distortion as depicted in Figure 8.

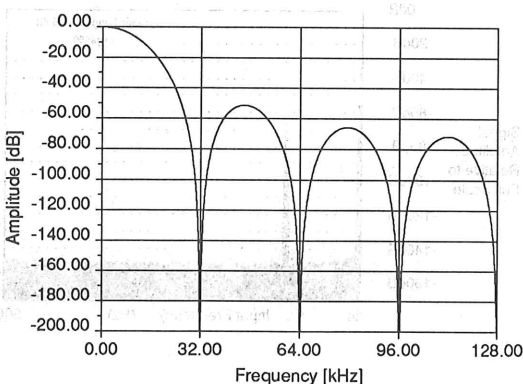


Figure 5. On-chip Filter Response

### Clock Source Considerations

To obtain maximum performance from the CS5324 requires a CLKIN signal which has a low level of clock jitter, i.e., less than 5 picoseconds of jitter. A well-designed crystal-based clock is preferred. The clock oscillator should have a well-regulated supply, with local bypass capacitors at the oscillator. The output from the oscillator should pass through as few logic gates or counter-divider stages as possible, as these can add jitter. Excess clock jitter will reduce the signal/noise performance of the A/D converter.

### Power Supply Rejection Ratio

The power supply noise rejection of the CS5324 is frequency dependent. The rejection for frequencies between dc and 500 Hz (CLKIN=1.024 MHz) is nearly constant. Above 500 Hz, the off-chip digital filter will aid in rejecting interference until the frequency of the interference approaches frequencies near CLKIN/21.3 (above 48 kHz for CLKIN=1.024 MHz). Power supply interference above this frequency may cause noise to be

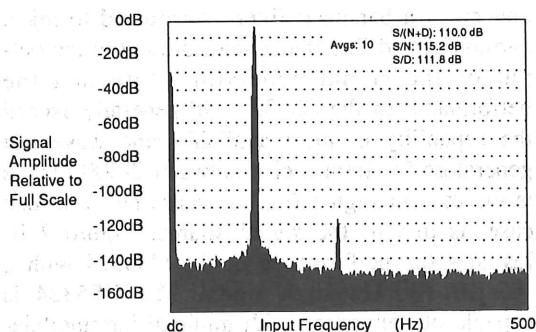


Figure 6. 1024 Point FFT Plot with Full Scale Input, 113 Hz.

modulated into the passband (dc to 500 Hz), degrading the performance of the A/D.

### Power Supply Considerations

The system connection diagram, Figure 1, illustrates the recommended power supply arrangements. The CS5324 has two positive analog supply pins and two negative analog supply pins. Multiple pins are used to minimize the possibility of noise coupling on the chip. All six power supply pins should be decoupled to their respective grounds, with a 0.1 uF capacitor located near the device. The digital supplies are decoupled from the analog supplies with 10 ohm resistors to minimize the effects of digital noise in the converter.

*The positive digital power supply of the CS5324 must never exceed either positive analog supply by more than a diode drop, or the CS5324 could experience permanent damage.* If separate supplies are used for the analog and digital sections of the chip, care must be taken that the analog supply comes up first at power-up. Additionally, the power supplies to the CS5324 should be active before the reference current generator supplies the IREF input current. For proper start-

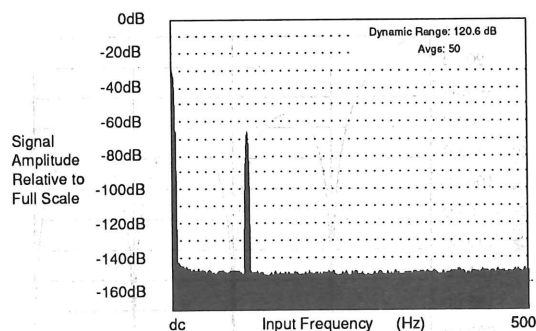


Figure 7. 1024 Point FFT Plot with -60 dB Input, 100 Hz.



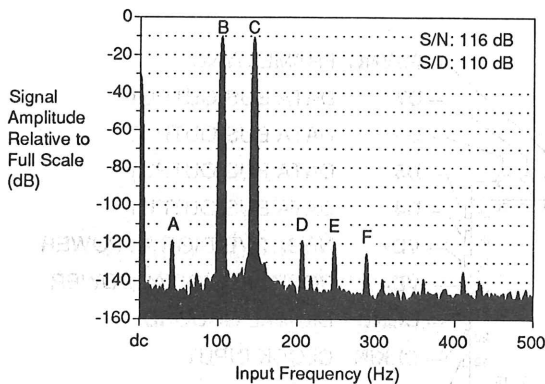


Figure 8. 1024 Point FFT Plot of Intermodulation Products.

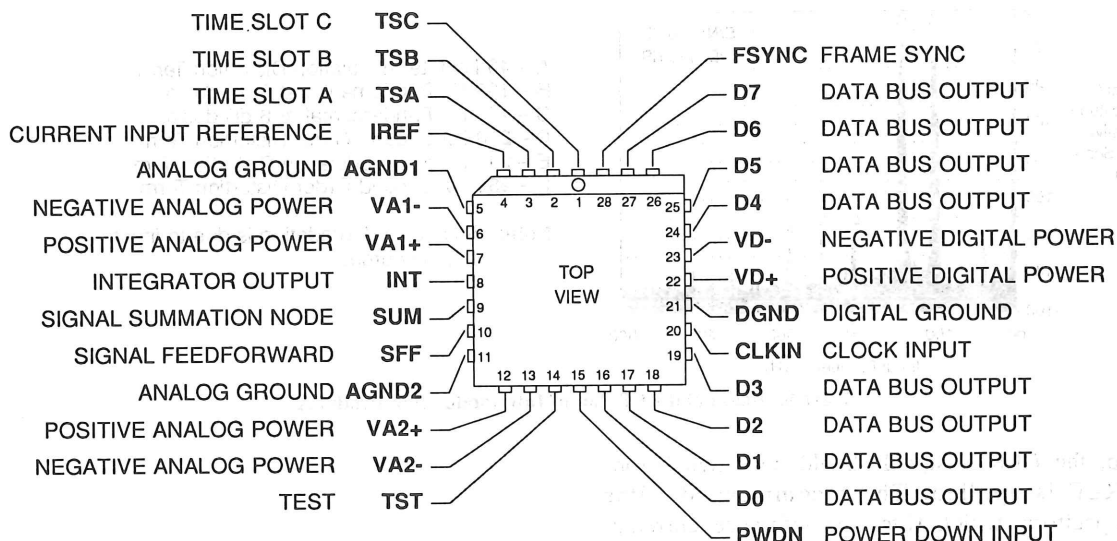
- A – 40 Hz Intermodulation Distortion Term
- B – 100 Hz Fundamental at 6 dB down
- C – 140 Hz Fundamental at 6 dB down
- D – 200 Hz Second Order Distortion Term
- E – 240 Hz Intermodulation Distortion Term
- F – 280 Hz Second Order Distortion Term

Note: S/N noise degradation is due to input signal source.

up, the CLKIN signal should be active before IREF is applied. The recommended filter capacitors, which filter the reference currents, will aid in accomplishing these requirements. Use of good ground plane layout is recommended to achieve maximum performance.

Many seismic or sonar systems are battery powered, and utilize dc-dc converters to generate the necessary supply voltages for the system. To minimize the effects of power supply interference, it is desirable to operate the dc-dc converter at a frequency which is rejected by the digital filtering in the A/D converter. To achieve maximum benefit of the digital filter in the A/D, the dc-dc operating frequency should be located below 48 kHz (see Power Supply Rejection). A synchronous dc-dc converter, whose operating frequency is derived from the 1.024 MHz clock used to drive the CS5324, will minimize the potential for "beat frequencies" appearing in the dc to 500 Hz passband.





## PIN DESCRIPTIONS

### Power Supplies

#### VA1+, VA2+ – Positive Analog Power, PINS 7, 12

Positive analog supply voltage. Nominally +5 volts.

#### VA1-, VA2- – Negative Analog Power, PINS 6, 13

Negative analog supply voltage. Nominally -5 volts.

#### AGND1, AGND2 – Analog Ground, PINS 5, 11

Analog ground reference.

#### VD+ – Positive Digital Power, PIN 22

Positive digital supply voltage. Nominally +5 volts.

#### VD- – Negative Digital Power, PIN 23

Negative digital supply voltage. Nominally -5 volts.

#### DGND – Digital Ground, PIN 21

Digital ground reference.

### **Analog Inputs**

#### **IREF – Current Input Reference Node, PIN 4**

This node accepts a 2 mA reference current to set the signal gain of the A/D converter.

#### **SFF – Signal Feedforward, PIN 10**

The input signal is fed forward around the integrator input stage by means of this input pin. This maximizes signal performance.

#### **SUM – Signal Summation node, PIN 9**

This is the input integrator virtual ground summing junction. The external integrator input resistor and integrating capacitor are connected to this node, along with a 500 uA bias current network.

#### **INT – Integrator Output, PIN 8**

Output pin of the input integrator stage. The external integrating capacitor is connected to this pin for proper operation.

### **Digital Inputs**

#### **CLKIN – Clock Input, PIN 20**

A CMOS-compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation of the modulator, digital filter and data output portions of the A/D converter.

#### **PWDN – Power Down Input, PIN 15**

When connected to +5 V (VD+) the CS5324 will enter a low-power state. For normal operation this pin should be tied to DGND.

#### **TSA – Time Slot A, PIN 3**

See TSC below.

#### **TSB – Time Slot B, PIN 2**

See TSC below.

#### **TSC – Time Slot C, PIN1**

The TSC input along with TSA and TSB select one of eight possible time periods in which data is output from the CS5324 in a time-multiplexed architecture. Table 2 indicates the decoding of the TSA, TSB, and TSC inputs.

#### **FSYNC – Frame Sync, PIN 28**

A transition from a low to high level on this input will re-initialize the CS5324. The digital filter will be initialized and the time-slot counter will be set to zero.

**D0 through D7 – Data Bus Outputs, PINS 16-19, 24-27**

3-state output pins. Data will be presented out of these pins in the form of two eight-bit bytes during a time slot selected by the TSA, TSB and TSC inputs. The high-order byte with eight data bits will be presented first followed by a second eight-bit byte, which consists of the four low-order data bits, three status bits, and one unused bit.

**Miscellaneous****TST – Test, PIN 14**

Reserved for production test facility. Should be tied to DGND for normal operation.

**PARAMETER DEFINITIONS****Dynamic Range**

The ratio of the full-scale (rms) signal to the broadband noise signal. Broadband noise is measured with the input grounded within the bandwidth of dc to 500 Hz. Units in dB.

**Signal-to-Distortion**

The ratio of the full-scale (rms) signal to the rms sum of all harmonics up to 500 Hz. Units in dB.

**Intermodulation Distortion**

The ratio of the rms sum of the two test frequencies (100 and 140 Hz) which are each 6 dB down from full-scale to the rms sum of all intermodulation components within the the bandwidth of dc to 500 Hz. Units in dB.

**Full Scale Error**

The ratio of the difference between the value of the voltage reference and analog input voltage to the full scale span (two times the voltage reference value). This ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted to yield a code value of 1280 out of the CS5324. Measurement of this parameter uses the circuitry illustrated in the System Connection Diagram. Units in %.

**Full Scale Drift**

The change in the Full Scale value with temperature. Units in %/°C.

**Offset**

The difference between the analog ground and the analog voltage necessary to yield an output code from the CS5324 of 00(H). Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in mV.

**Offset Drift**

The change in the Offset value with temperature. Units in  $\mu\text{V}/^\circ\text{C}$ .

## Appendix 1.

### Off-chip Filter Stages

Two stages of off-chip filtering are recommended for use with the CS5324. The first stage is a decimate-by-8 modified-sinc filter with 43 coefficients. Its magnitude response is illustrated in Figure A1.1. Table A1.1 lists its coefficients.

The second filter stage is a 301st-order low-pass filter. Its magnitude plot is illustrated in Figure A1.2 with an expanded view of the passband

ripple illustrated in Figure A1.3. Table A1.2 lists the coefficients for this filter.

An alternative second stage filter is also included. It has fewer coefficients, and therefore, is less complex than the previous second stage filter. The magnitude plot of the alternative filter is illustrated in Figure A1.4 with an expanded view of the passband ripple in Figure A1.5. Note that this low-pass function has slightly less out-of-band rejection and somewhat higher passband ripple. The filter coefficients for the alternative final stage are listed in Table A1.3.

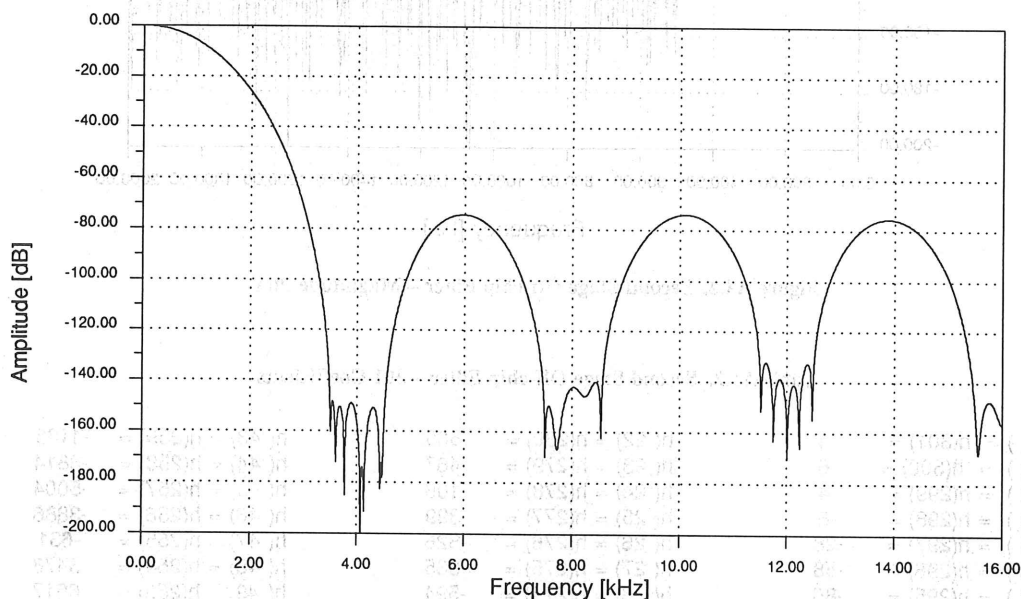
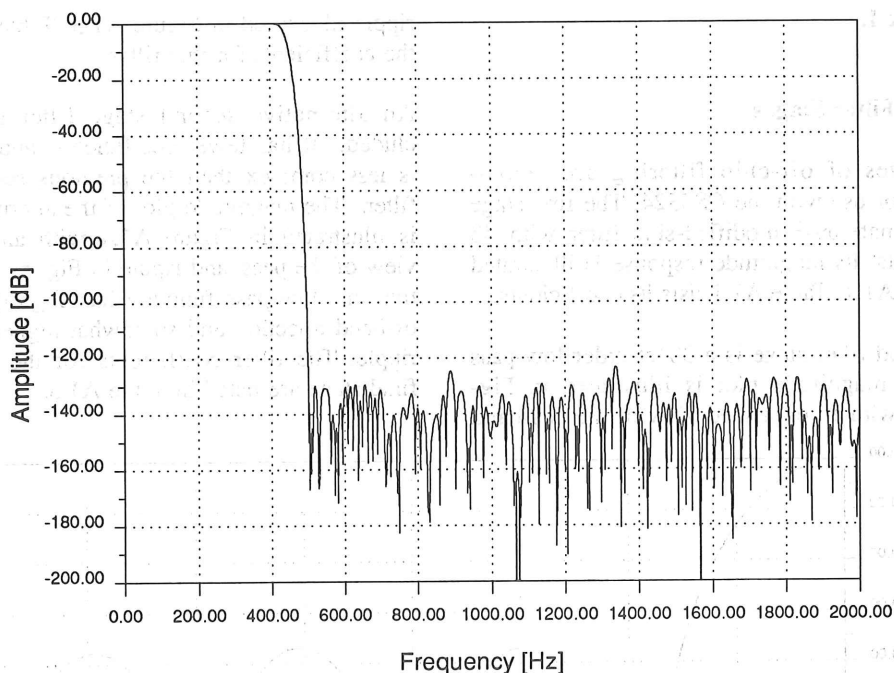


Figure A1.1. First Stage Off-chip Filter – Magnitude Plot

$h(1) = h(43) = 1623$	$h(12) = h(32) = 1143595$
$h(2) = h(42) = 5137$	$h(13) = h(31) = 1494661$
$h(3) = h(41) = 12950$	$h(14) = h(30) = 1889251$
$h(4) = h(40) = 28499$	$h(15) = h(29) = 2315005$
$h(5) = h(39) = 55210$	$h(16) = h(28) = 2752059$
$h(6) = h(38) = 99783$	$h(17) = h(27) = 3185947$
$h(7) = h(37) = 169332$	$h(18) = h(26) = 3584677$
$h(8) = h(36) = 272838$	$h(19) = h(25) = 3926472$
$h(9) = h(35) = 414146$	$h(20) = h(24) = 4191616$
$h(10) = h(34) = 604491$	$h(21) = h(23) = 4354400$
$h(11) = h(33) = 847470$	$h(22) = 4410541$

Table A1.1. First Stage Off-chip Filter – 43 Coefficients



**Figure A1.2. Second Stage Off-chip Filter – Magnitude Plot**

**Table A1.2. Second Stage Off-chip Filter – 301 Coefficients**

$h(1) = h(301) = 4$	$h(22) = h(280) = 565$	$h(43) = h(259) = -1168$
$h(2) = h(300) = 6$	$h(23) = h(279) = 467$	$h(44) = h(258) = -3814$
$h(3) = h(299) = 4$	$h(24) = h(278) = 106$	$h(45) = h(257) = -5004$
$h(4) = h(298) = -6$	$h(25) = h(277) = -399$	$h(46) = h(256) = -3886$
$h(5) = h(297) = -28$	$h(26) = h(276) = -826$	$h(47) = h(255) = -631$
$h(6) = h(296) = -58$	$h(27) = h(275) = -935$	$h(48) = h(254) = 3478$
$h(7) = h(295) = -85$	$h(28) = h(274) = -594$	$h(49) = h(253) = 6517$
$h(8) = h(294) = -93$	$h(29) = h(273) = 127$	$h(50) = h(252) = 6784$
$h(9) = h(293) = -68$	$h(30) = h(272) = 947$	$h(51) = h(251) = 3702$
$h(10) = h(292) = -7$	$h(31) = h(271) = 1468$	$h(52) = h(250) = -1711$
$h(11) = h(291) = 75$	$h(32) = h(270) = 1359$	$h(53) = h(249) = -7104$
$h(12) = h(290) = 146$	$h(33) = h(269) = 538$	$h(54) = h(248) = -9771$
$h(13) = h(289) = 166$	$h(34) = h(268) = -725$	$h(55) = h(247) = -7963$
$h(14) = h(288) = 108$	$h(35) = h(267) = -1882$	$h(56) = h(246) = -1918$
$h(15) = h(287) = -23$	$h(36) = h(266) = -2320$	$h(57) = h(245) = 5964$
$h(16) = h(286) = -185$	$h(37) = h(265) = -1673$	$h(58) = h(244) = 12013$
$h(17) = h(285) = -302$	$h(38) = h(264) = -56$	$h(59) = h(243) = 12943$
$h(18) = h(284) = -300$	$h(39) = h(263) = 1898$	$h(60) = h(242) = 7567$
$h(19) = h(283) = -144$	$h(40) = h(262) = 3264$	$h(61) = h(241) = -2315$
$h(20) = h(282) = 130$	$h(41) = h(261) = 3239$	$h(62) = h(240) = -12399$
$h(21) = h(281) = 414$	$h(42) = h(260) = 1580$	$h(63) = h(239) = -17689$

h( 64) = h(238) = -14905  
 h( 65) = h(237) = -4360  
 h( 66) = h(236) = 9720  
 h( 67) = h(235) = 20798  
 h( 68) = h(234) = 22983  
 h( 69) = h(233) = 14065  
 h( 70) = h(232) = -2922  
 h( 71) = h(231) = -20553  
 h( 72) = h(230) = -30166  
 h( 73) = h(229) = -26027  
 h( 74) = h(228) = -8537  
 h( 75) = h(227) = 15226  
 h( 76) = h(226) = 34244  
 h( 77) = h(225) = 38558  
 h( 78) = h(224) = 24349  
 h( 79) = h(223) = -3468  
 h( 80) = h(222) = -32689  
 h( 81) = h(221) = -49042  
 h( 82) = h(220) = -43038  
 h( 83) = h(219) = -15194  
 h( 84) = h(218) = 23126  
 h( 85) = h(217) = 54160  
 h( 86) = h(216) = 61841  
 h( 87) = h(215) = 39925  
 h( 88) = h(214) = -3894  
 h( 89) = h(213) = -50321  
 h( 90) = h(212) = -76781  
 h( 91) = h(211) = -68222  
 h( 92) = h(210) = -25304  
 h( 93) = h(209) = 34332

h( 94) = h(208) = 83049  
 h( 95) = h(207) = 95832  
 h( 96) = h(206) = 62860  
 h( 97) = h(205) = -4158  
 h( 98) = h(204) = -75642  
 h( 99) = h(203) = -116939  
 h(100) = h(202) = -104877  
 h(101) = h(201) = -40254  
 h(102) = h(200) = 50253  
 h(103) = h(199) = 124723  
 h(104) = h(198) = 145121  
 h(105) = h(197) = 96333  
 h(106) = h(196) = -4251  
 h(107) = h(195) = -112209  
 h(108) = h(194) = -175323  
 h(109) = h(193) = -158449  
 h(110) = h(192) = -62339  
 h(111) = h(191) = 73359  
 h(112) = h(190) = 185878  
 h(113) = h(189) = 217891  
 h(114) = h(188) = 146090  
 h(115) = h(187) = -4196  
 h(116) = h(186) = -166796  
 h(117) = h(185) = -263179  
 h(118) = h(184) = -239689  
 h(119) = h(183) = -96169  
 h(120) = h(182) = 108776  
 h(121) = h(181) = 280687  
 h(122) = h(180) = 331861  
 h(123) = h(179) = 224879

h(124) = h(178) = -4045  
 h(125) = h(177) = -255205  
 h(126) = h(176) = -407467  
 h(127) = h(175) = -375114  
 h(128) = h(174) = -153475  
 h(129) = h(173) = 169870  
 h(130) = h(172) = 447384  
 h(131) = h(171) = 536503  
 h(132) = h(170) = 369619  
 h(133) = h(169) = -3865  
 h(134) = h(168) = -426733  
 h(135) = h(167) = -696076  
 h(136) = h(166) = -655325  
 h(137) = h(165) = -276498  
 h(138) = h(164) = 307141  
 h(139) = h(163) = 839720  
 h(140) = h(162) = 1044525  
 h(141) = h(161) = 751372  
 h(142) = h(160) = -3724  
 h(143) = h(159) = -953887  
 h(144) = h(158) = -1671933  
 h(145) = h(157) = -1718209  
 h(146) = h(156) = -813868  
 h(147) = h(155) = 1027355  
 h(148) = h(154) = 3464481  
 h(149) = h(153) = 5912858  
 h(150) = h(152) = 7722306  
 h(151) = h(151) = 8388608

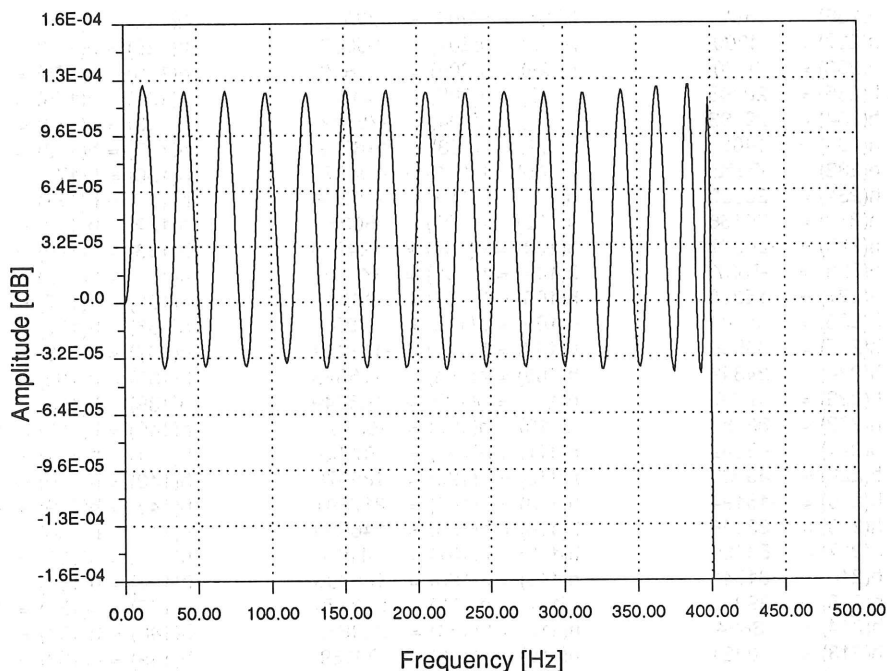


Figure A 1.3. Second Stage Off-chip Filter – Passband Ripple Plot

Table A 1.3. Alternate Second Stage Off-chip Filter – 201 Coefficients

$h(1) = h(201) = -68$	$h(21) = h(181) = -5542$	$h(41) = h(161) = 13122$
$h(2) = h(200) = -266$	$h(22) = h(180) = 4957$	$h(42) = h(160) = 49003$
$h(3) = h(199) = -681$	$h(23) = h(179) = 15066$	$h(43) = h(159) = 66874$
$h(4) = h(198) = -1350$	$h(24) = h(178) = 20225$	$h(44) = h(158) = 56133$
$h(5) = h(197) = -2192$	$h(25) = h(177) = 17383$	$h(45) = h(157) = 18103$
$h(6) = h(196) = -2938$	$h(26) = h(176) = 6584$	$h(46) = h(156) = -33025$
$h(7) = h(195) = -3124$	$h(27) = h(175) = -8560$	$h(47) = h(155) = -75161$
$h(8) = h(194) = -2181$	$h(28) = h(174) = -21921$	$h(48) = h(154) = -87623$
$h(9) = h(193) = 366$	$h(29) = h(173) = -27236$	$h(49) = h(153) = -60982$
$h(10) = h(192) = 4634$	$h(30) = h(172) = -20930$	$h(50) = h(152) = -2877$
$h(11) = h(191) = 10142$	$h(31) = h(171) = -4177$	$h(51) = h(151) = 63451$
$h(12) = h(190) = 15743$	$h(32) = h(170) = 16903$	$h(52) = h(150) = 108121$
$h(13) = h(189) = 19809$	$h(33) = h(169) = 33304$	$h(53) = h(149) = 107776$
$h(14) = h(188) = 20712$	$h(34) = h(168) = 36843$	$h(54) = h(148) = 57300$
$h(15) = h(187) = 17462$	$h(35) = h(167) = 24059$	$h(55) = h(147) = -25620$
$h(16) = h(186) = 10292$	$h(36) = h(166) = -1482$	$h(56) = h(146) = -106083$
$h(17) = h(185) = 889$	$h(37) = h(165) = -29822$	$h(57) = h(145) = -146288$
$h(18) = h(184) = -7915$	$h(38) = h(164) = -48300$	$h(58) = h(144) = -122895$
$h(19) = h(183) = -13029$	$h(39) = h(163) = -47054$	$h(59) = h(143) = -39611$
$h(20) = h(182) = -12292$	$h(40) = h(162) = -24000$	$h(60) = h(142) = 71441$



h( 61) = h(141) = 161525	h( 75) = h(127) = -349221	h( 89) = h(113) = 932553
h( 62) = h(140) = 186220	h( 76) = h(126) = -386474	h( 90) = h(112) = 1005109
h( 63) = h(139) = 126698	h( 77) = h(125) = -245727	h( 91) = h(111) = 595458
h( 64) = h(138) = 1412	h( 78) = h(124) = 28395	h( 92) = h(110) = -209660
h( 65) = h(137) = -138356	h( 79) = h(123) = 323264	h( 93) = h(109) = -1121850
h( 66) = h(136) = -228840	h( 80) = h(122) = 502448	h( 94) = h(108) = -1730461
h( 67) = h(135) = -222225	h( 81) = h(121) = 466350	h( 95) = h(107) = -1642084
h( 68) = h(134) = -110815	h( 82) = h(120) = 203318	h( 96) = h(106) = -632318
h( 69) = h(133) = 64893	h( 83) = h(119) = -193406	h( 97) = h(105) = 1247052
h( 70) = h(132) = 229769	h( 84) = h(118) = -554902	h( 98) = h(104) = 3649798
h( 71) = h(131) = 305309	h( 85) = h(117) = -704448	h( 99) = h(103) = 6019586
h( 72) = h(130) = 245984	h( 86) = h(116) = -538246	h(100) = h(102) = 7753188
h( 73) = h(129) = 64260	h( 87) = h(115) = -84243	h(101) = h(101) = 8388608
h( 74) = h(128) = -168625	h( 88) = h(114) = 490248	

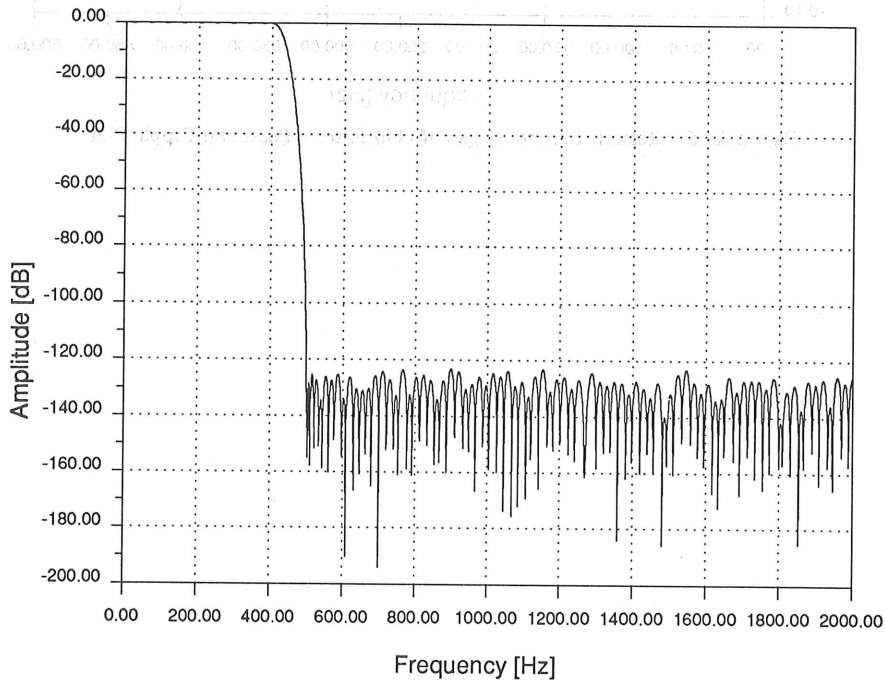
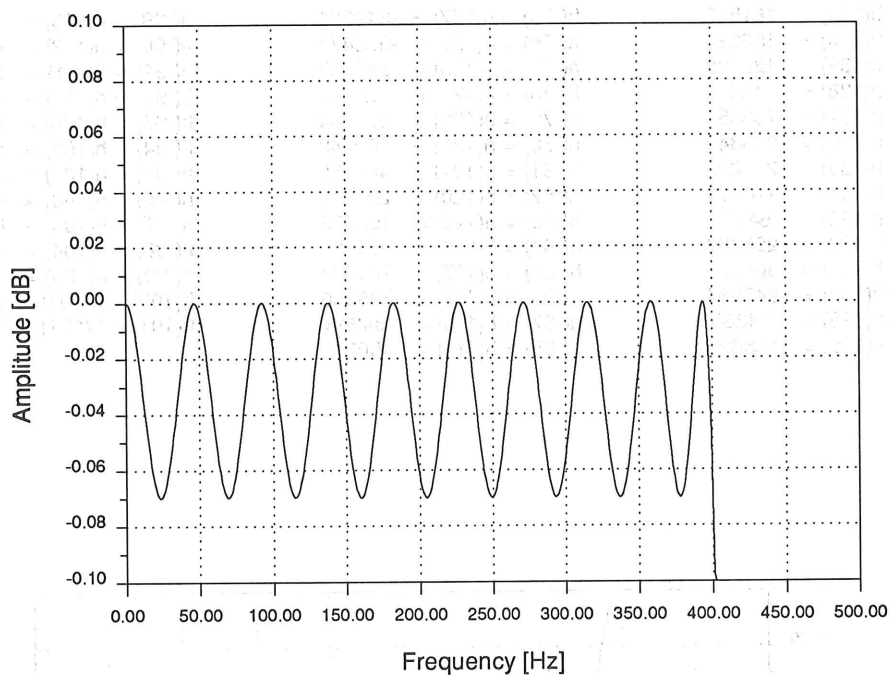


Figure A 1.4 Alternate Second Stage Off-chip Filter – Magnitude Plot



**Figure A1.5 Alternate Second Stage Off-chip Filter – Passband Ripple Plot**

## Evaluation Board for CS5324

### Features

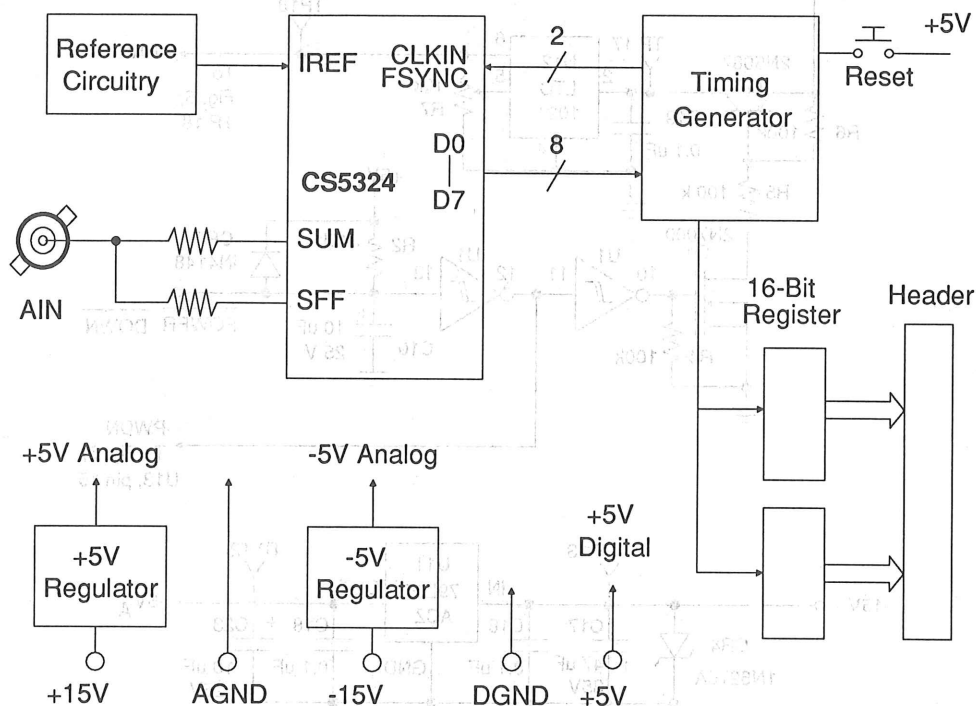
- PC/ $\mu$ P-compatible Header Connection
  - 16 Bit Parallel Data
  - Three-State Output
  - Data Ready Signal
- Analog/Digital Patch Areas
- Analog BNC Input Connector

### General Description

The CDB5324 is an evaluation board that allows the laboratory characterization of the CS5324 A/D converter. The CS5324 is a 120dB dynamic range, 500Hz bandwidth ADC intended for seismic applications. The board supports  $\pm 10$  volt analog input signals and generates the timing signals which format the output data from the CS5324 into a single 16-bit parallel word.

**Ordering Information:** CDB5324

3



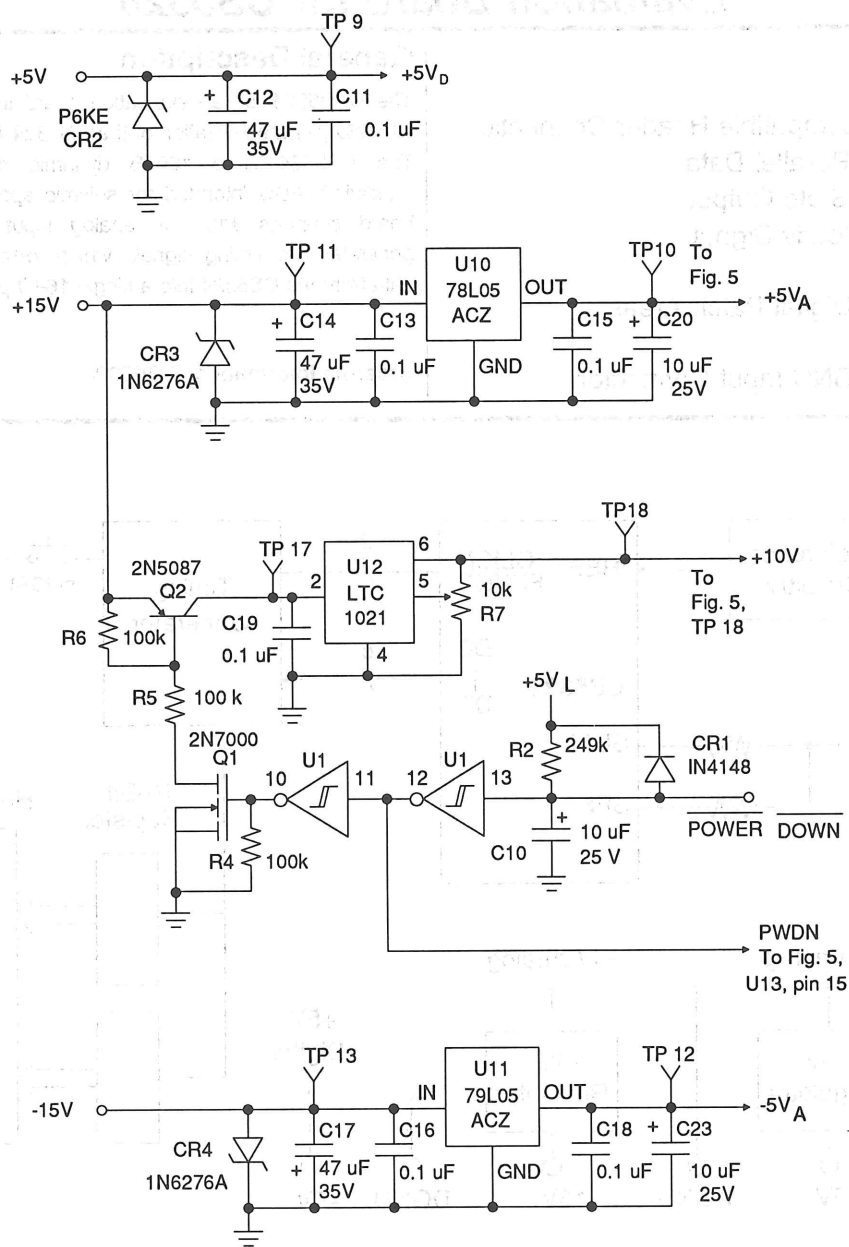


Figure 1. Voltage Regulators and +10V Reference

### Power Supplies and Voltage Reference

The CDB5324 evaluation board requires three separate input voltages for proper operation. Figure 1 illustrates the power supply connections. The required power supply input voltages consist of +5V, +15V, and -15V. The +5V input supplies power to the digital logic portion of the board. The +15V and -15V inputs are regulated down to

provide the +5V and -5V supplies necessary for the CS5324. Also included in Figure 1 is a start-up circuit which allows a power-down signal to turn off both the CS5324 and the supply current to the LTC1021 voltage reference. An RC delay is added as part of the start-up circuitry to insure the the +5V digital supply is present before the LTC1021 voltage reference is turned on. The FSYNC and CLKIN signals to the CS5324 must

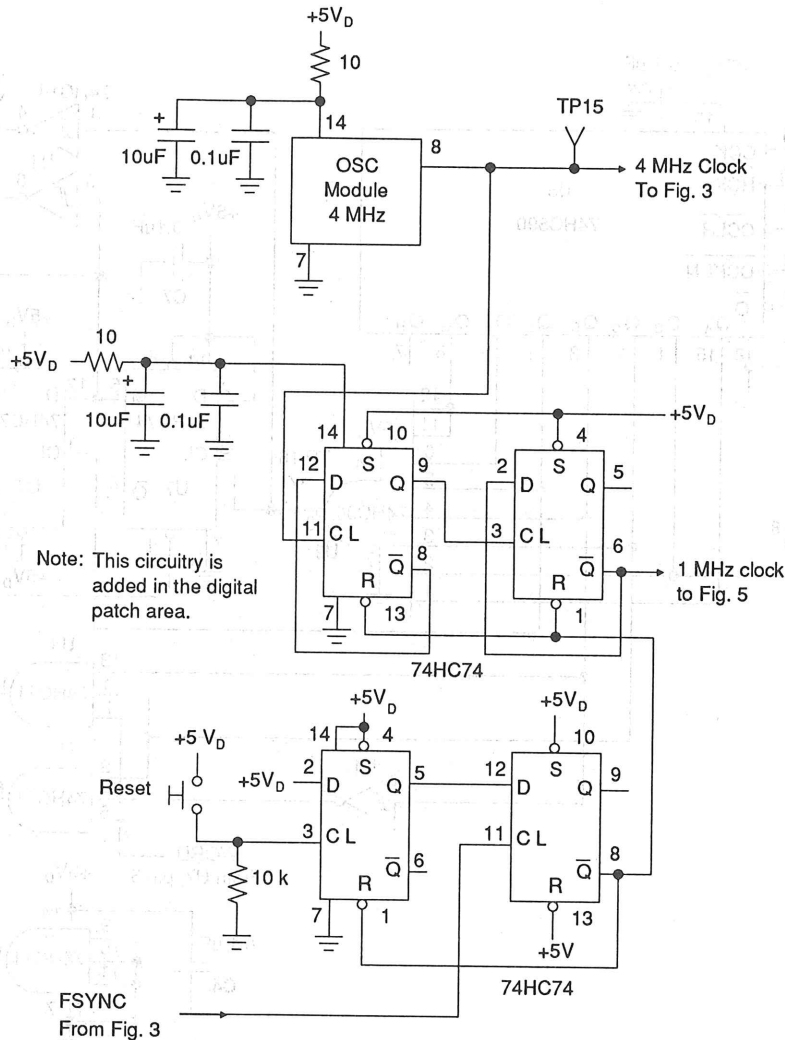
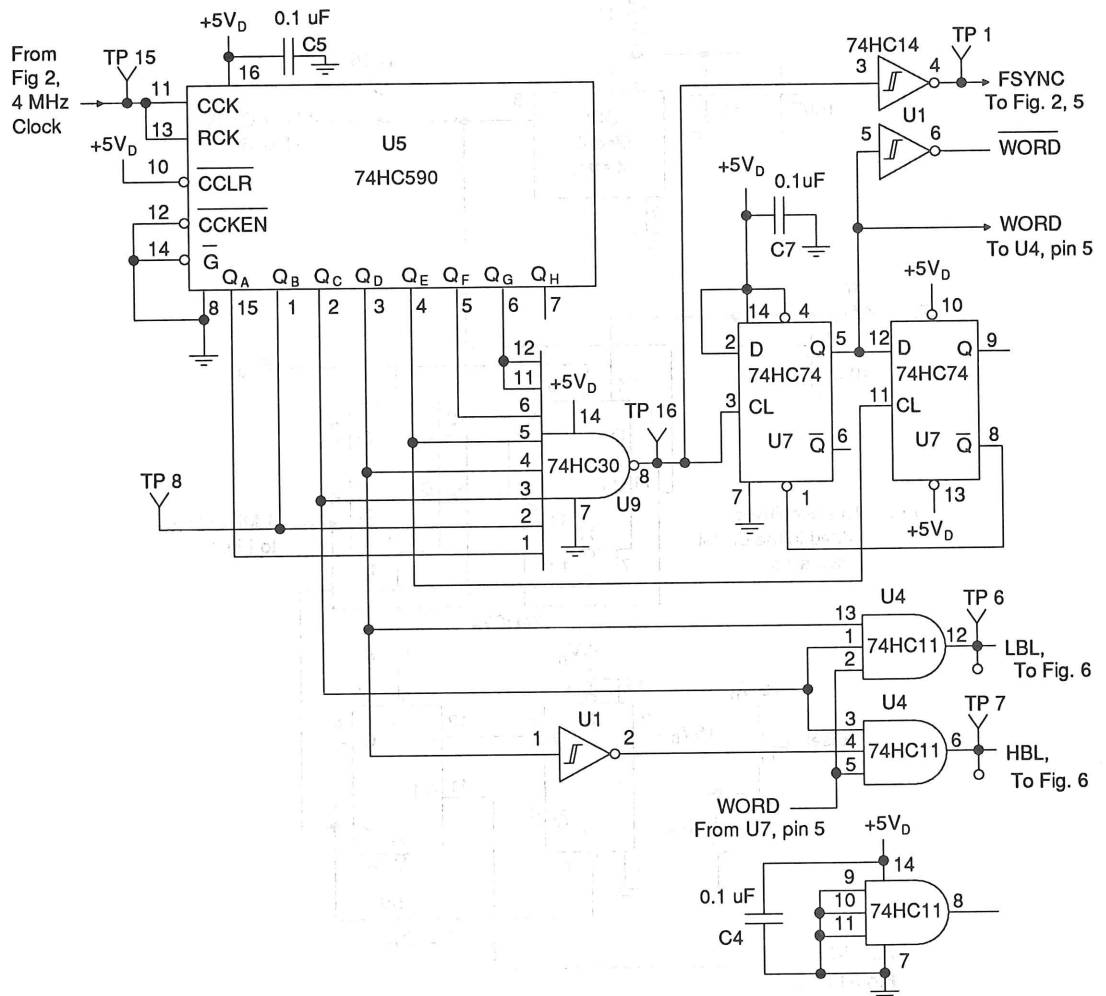


Figure 2. Clock Oscillator/Divider

be furnished by the digital logic whenever the voltage reference is turned on to insure proper start-up of the device. This start-up circuitry is provided on the evaluation board to insure proper start-up of the CS5324 while using separate laboratory supplies which may then be turned on in any sequence. This circuitry is not required if all of the supplies are activated at the same time.

### Clock Oscillator/Divider

Figure 2 illustrates the oscillator and clock divider circuitry used to generate the 1 MHz clock for the CS5324 A/D converter. This circuitry is in the digital patch area of the circuit card. The 1 MHz clock to the CS5324 must have low jitter. Jitter on the clock of any high resolution A/D converter



**Figure 3. Timing Generator**

will reduce the signal-to-noise capability of the device.

Note that both the oscillator and the dual D flip-flop used to divide the oscillator output are individually decoupled from the +5V logic supply. The second dual D flip-flop pair are used to synchronize the 1 MHz from the dual D divider to be in phase with the 1 MHz out of the 74HC590 counter. This synchronization is necessary to insure that the other timing signals derived from the 74HC590 outputs have the proper phase relationship to the 1 MHz clock in the CS5324.

## Reset

To insure synchronization of the 1 MHz clock to the CS5324 with the other clock signals in the system, the reset button in the digital patch area of the board must be activated after power is applied to the system.

## Timing Generator

Figure 3 illustrates the logic circuitry which generates the timing signals used to latch the data coming out of the CS5324 A/D converter. The outputs from the 74HC590 counter are used to generate FSYNC, HBL (High Byte Latch), LBL (Low Byte Latch), and WORD. Figure 4 illustrates the timing relationships of these signals.

3

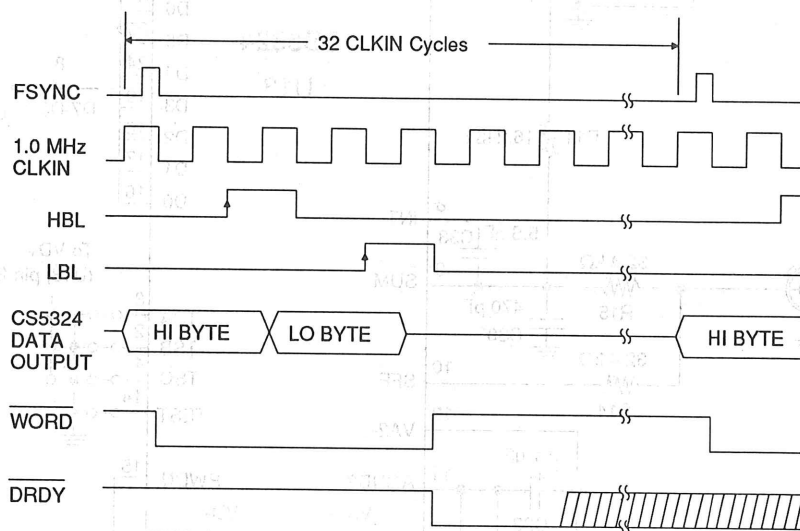


Figure 4. Timing Diagram





### Output Registers/Header Connector

Data from the CS5324 A/D converter is latched into the two 74HC574 octal flip-flops by the HBL and LBL latch signals generated by the timing generator. The outputs of the 74HC574's are then connected to the 40-pin header Connector. Figure 7 identifies the pins on the 40-pin header.

Note that each of the data output pins is adjacent to a ground pin on the header. In constructing a cable for interfacing to the evaluation board, twisted-pair ribbon cable (Beldon Vari-Twist 9V28040 or equivalent) should be used. Each twisted pair should include a ground line with the data signal as this minimizes radiated noise.

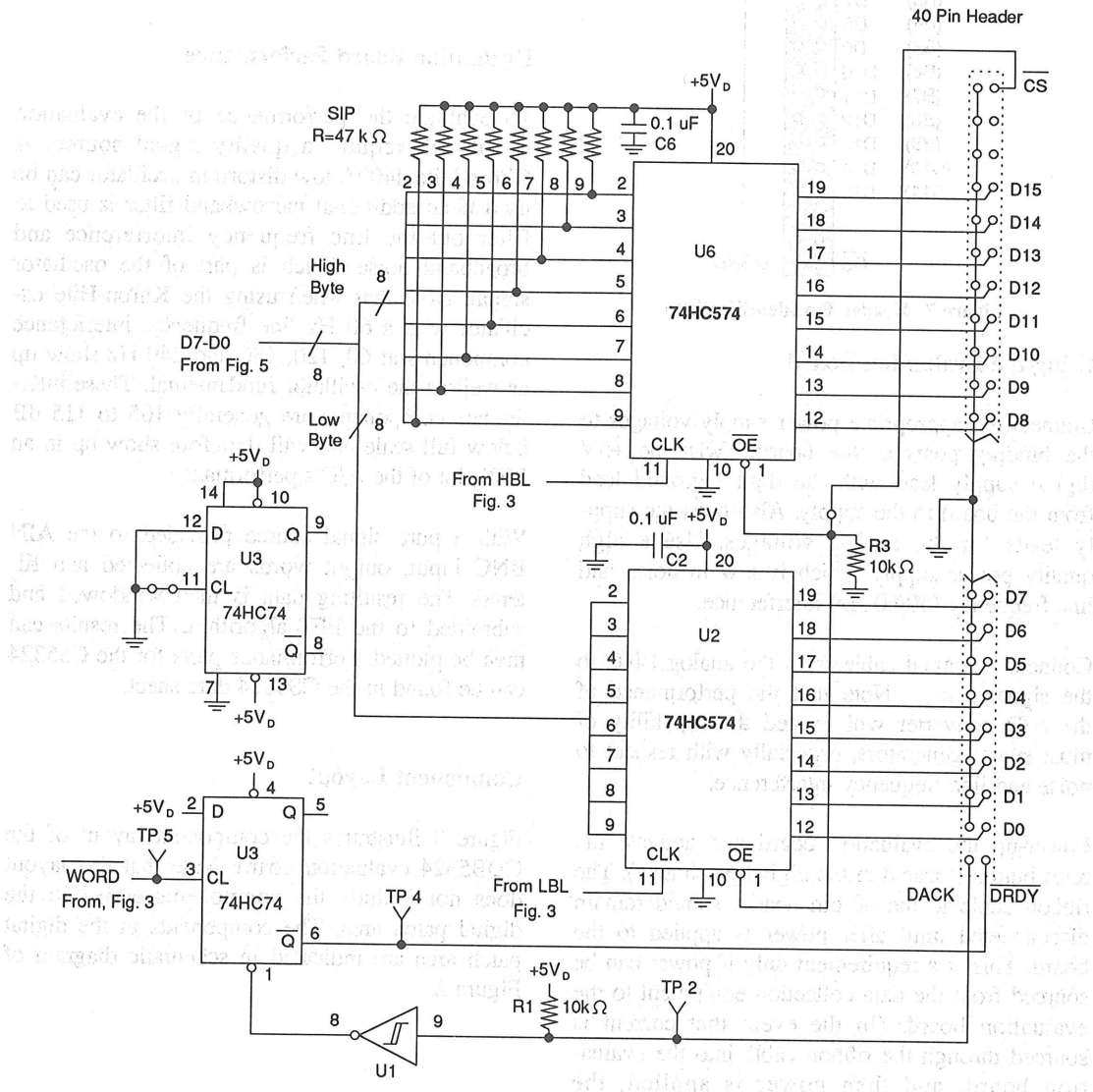
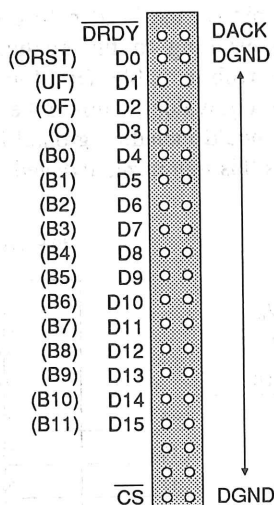


Figure 6. Output Registers/Header Connector



**Figure 7. Header Pin Identification**

### Using the Evaluation Board

Connect the appropriate power supply voltages to the binding posts of the board. Twist the +5V digital supply lead with the digital ground lead from the board to the supply. Also twist the supply leads for the analog voltages. Use a high quality power supply which is low in noise and line frequency (50/60 Hz) interference.

Connect a coaxial cable from the analog BNC to the signal source. Note that the performance of the A/D converter will exceed the capability of most signal generators, especially with respect to noise and line frequency interference.

Power-up the evaluation board and activate the reset button (located in the digital patch area). The ribbon cable to the 40-pin header should remain disconnected until after power is applied to the board. This is a requirement only if power can be sourced from the data collection equipment to the evaluation board. (In the event that current is sourced through the ribbon cable into the evaluation board, and then power is applied, the

evaluation board circuitry may not start-up properly).

Data from the evaluation board must be processed using digital filter functions, such as those found in the Appendix of the CS5324 data sheet to achieve the full 120 dB dynamic range of the A/D.

### Evaluation Board Performance

To evaluate the performance of the evaluation board will require a quality signal source. A Khron-Hite 4400A low distortion oscillator can be used if an additional narrowband filter is used to filter out the line frequency interference and broadband noise which is part of the oscillator signal. Note that when using the Khron-Hite oscillator with a 60 Hz line frequency, interference components at 60, 120, 180 and 240 Hz show up as well as the oscillator fundamental. These interference components are generally 105 to 115 dB below full scale and will therefore show up in an FFT plot of the A/D's performance.

With a pure signal source provided to the AIN BNC input, output words are collected and filtered. The resulting data is then windowed and submitted to the FFT algorithm. The results can then be plotted. Performance plots for the CS5324 can be found in the CS5324 data sheet.

### Component Layout

Figure 8 illustrates the component layout of the CDB5324 evaluation board. Note that this layout does not include the components added in the digital patch area. The components in the digital patch area are indicated in schematic diagram of Figure 2.

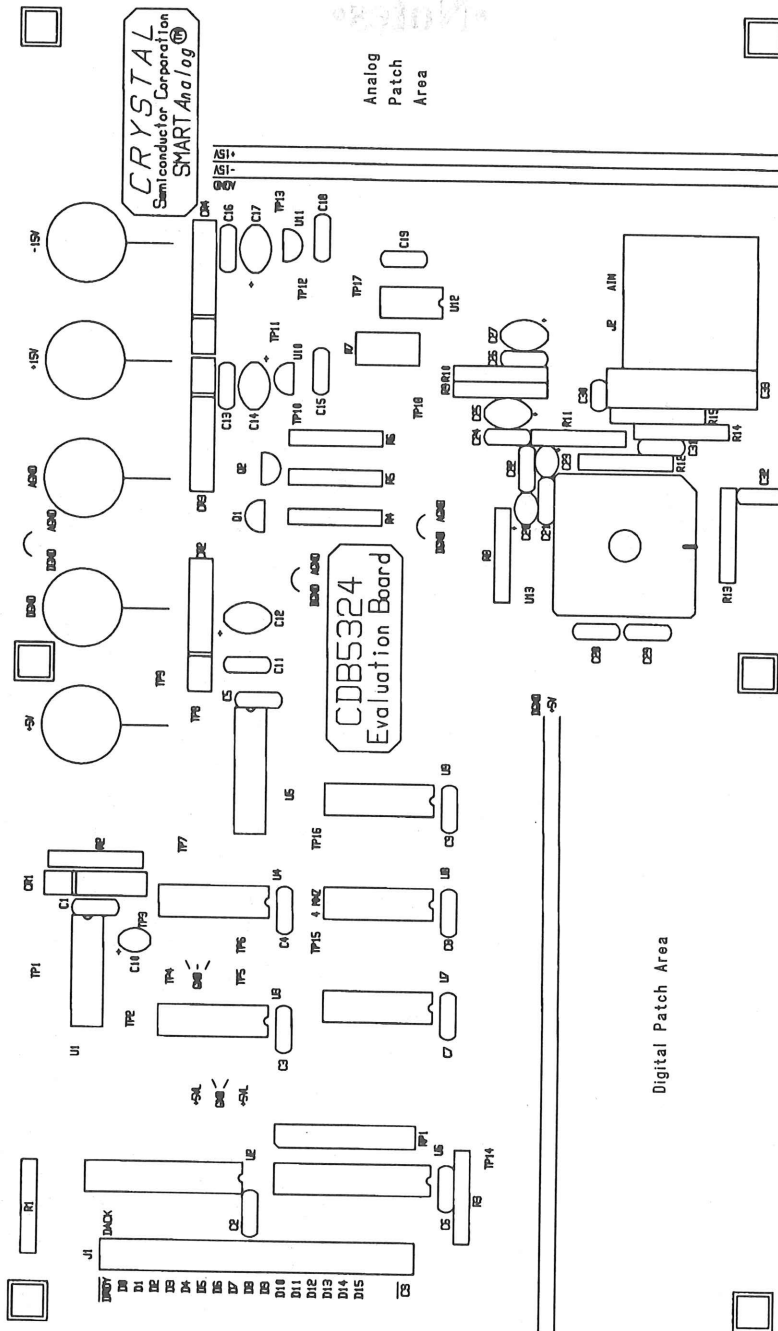


Figure 8. CDB5324 Component Layout

**•Notes•**

## 12-Bit, 1MHz Self-Calibrating A/D Converter

### Features

- Monolithic CMOS Sampling ADC  
On-Chip Track and Hold Amplifier  
Microprocessor Interface
- Throughput Rates up to 1MHz
- True 12-Bit Accuracy over Temperature  
Typical Nonlinearity: 3/4 LSB  
No Missing Codes to 12 Bits
- Total Harmonic Distortion: 0.02%
- Dynamic Range: 72dB
- Self-Calibration Maintains Accuracy  
over Time and Temperature
- Low Power Dissipation: 750mW

### General Description

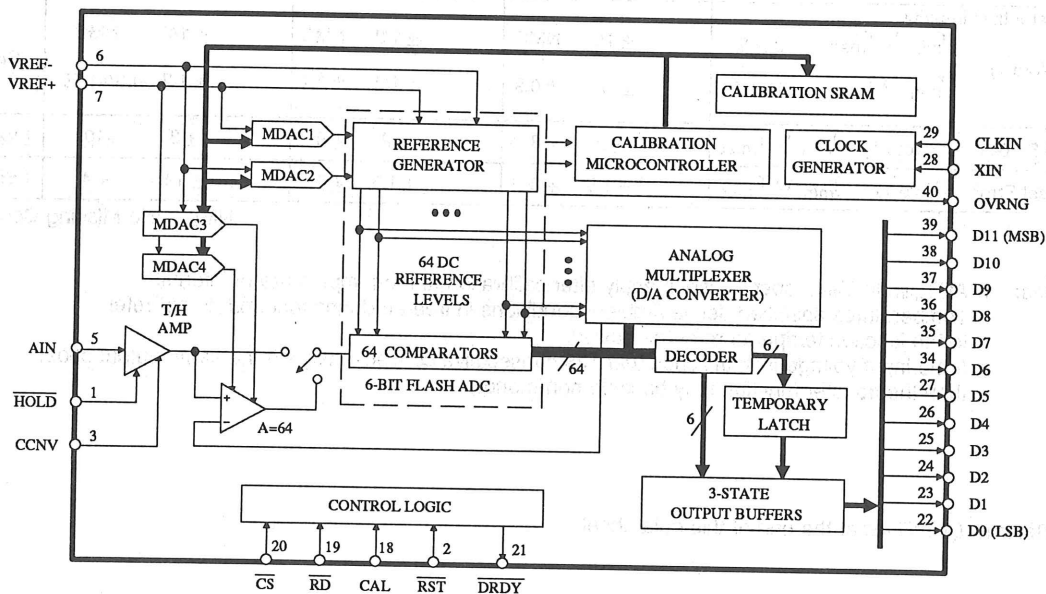
The CS5412 CMOS analog to digital converter provides a true 12-bit representation of an analog input signal at sampling rates up to 1MHz. To achieve high throughput, the CS5412 uses pipelined acquisition and settling times as well as overlapped conversion cycles.

Unique self-calibration circuitry insures 12-bit accuracy over time and temperature. Also, a background calibration process constantly adjusts the converter's linearity, thereby insuring superior harmonic distortion and signal-to-noise performance throughout operating life.

The CS5412's advanced CMOS construction provides low power consumption of 750mW and the inherent reliability of monolithic devices.

An evaluation board is available which allows fast confirmation of performance, as well as example ground and layout arrangements.

**ORDERING INFORMATION:** Page 3-228



# **ANALOG CHARACTERISTICS** (T<sub>A</sub> = 25°C (Note 1); All VA+ pins, VD+ = 5V; All VA- pins, VD- = -5V; VREF+ = +1.5V; VREF- = -1.5V; f<sub>CLK</sub> = 8MHz for -1; 100 kHz Full Scale Input Sinewave; Continuous Convert Mode unless otherwise specified).

Parameter*	CS5412-J,K min typ max	CS5412-A,B min typ max	CS5412-S,T min typ max	Units
Resolution T <sub>min</sub> to T <sub>max</sub>	12	12	12	Bits
Specified Temperature Range	0 to 70	-40 to +85	-55 to +125	°C
<b>Dynamic Performance</b>				
Peak Harmonic or Spurious Noise (Note 1) T <sub>min</sub> to T <sub>max</sub> 100kHz Input	75 82	75 82	75 82	dB
490kHz Input	68	68	68	
Total Harmonic Distortion	0.0125	0.0125	0.0125	%
Signal-to-(Noise plus Distortion)(Note 1) 0dB Input (Full Scale)	65 71 68 71 32	65 71 68 71 32	65 71 68 71 32	dB
T <sub>min</sub> to T <sub>max</sub> -J,A,S				
-K,B,T				
-40dB Input				
<b>dc Accuracy</b>				
Linearity Error T <sub>min</sub> to T <sub>max</sub> -J,A,S	± 3/4 ± 2.0	± 3/4 ± 2.0	± 1 ± 3.0	LSB
(Note 1,2) T <sub>min</sub> to T <sub>max</sub> -K,B,T	± 3/4 ± 1.0	± 3/4 ± 1.0	± 3/4 ± 2.0	
Differential Linearity T <sub>min</sub> to T <sub>max</sub> -J,A,S	± 1/2 NMC	± 1/2 NMC	± 1/2 NMC	LSB
(Note 1) T <sub>min</sub> to T <sub>max</sub> -K,B,T	± 1/2 ± 0.9	± 1/2 ± 0.9	± 1/2 -0.9/+1.25	
Full Scale Error (Note 1) T <sub>min</sub> to T <sub>max</sub>	± 2 ± 8	± 2 ± 8	± 3 ± 10	LSB
Offset Error (Note 1) T <sub>min</sub> to T <sub>max</sub>	± 1.5 ± 3	± 1.5 ± 3	± 1.5 ± 4	LSB

NMC = No Missing Codes

- Notes: 1. All T<sub>min</sub> to T<sub>max</sub> specifications apply after calibration at the temperature of interest.  
Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.
2. If the input voltage is static such that 128 consecutive conversions yield the same output code, then the transfer function may become non-monotonic.

\* Refer to *Definitions* at the end of this data sheet.

Specifications are subject to change without notice.



### ANALOG CHARACTERISTICS (Continued)

Parameter	CS5412-J,K			CS5412-A,B			CS5412-S,T			Units
	min	typ	max	min	typ	max	min	typ	max	
<b>Analog Input</b>										
Aperture Time		35			35			35		ns
Aperture Jitter		50			50			50		ps, rms
Input Bandwidth										
Small Signal, -3dB (Note 3)		4			4			4		MHz
Full Power, -3dB		3.5			3.5			3.5		MHz
Analog Input Impedance at dc		10			10			10		Mohms
Input Capacitance	VREF- pin	50			50			50		pF
	AIN, VREF+ pins	10			10			10		pF
<b>Conversion &amp; Throughput</b>										
Conversion Time (Notes 4, 5)	1.25		1.5	1.25		1.5	1.25		1.5	us
Throughput Rate	1			1			1			MHz
Acquisition Time (Note 6)		400			400			400		ns
<b>Power Supplies</b>										
Power Supply Current (Note 7)										
IA+		70	90		70	90		70	90	mA
IA-		-70	-90		-70	-90		-70	-90	mA
ID+		5	10		5	10		5	10	mA
ID-		-5	-10		-5	-10		-5	-10	mA
Power Consumption (Note 7)		750	1000		750	1000		750	1000	mW
Power Supply Rejection at dc										
Positive Supplies		50			50			50		dB
Negative Supplies		50			50			50		dB

- Notes:
3. Input 40 dB below full scale.
  4. Measured from falling transition on **HOLD** to falling transition on **DRDY**.
  5. Applies to conversions triggered externally. In Continuous Convert mode throughput proceeds at one-eighth the master clock frequency with a fixed 10 clock cycle conversion time.
  6. The internal track-and-hold returns to the track mode on the fourth master clock cycle after the start of a conversion cycle. It is guaranteed to acquire a full-scale step to 12-bit accuracy while operating at full throughput.
  7. All outputs unloaded. All inputs CMOS levels.

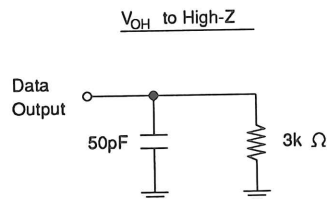
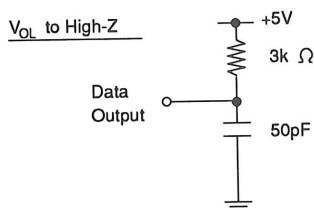
**SWITCHING CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ; All  $V_{A+}$  pins,  $V_{D+} = 5V \pm 5\%$ ; All  $V_{A-}$  pins,  $V_{D-} = -5V \pm 5\%$ ; Inputs: Logic 0 = 0V, Logic 1 =  $V_{D+}$ ;  $C_L = 50$  pF).

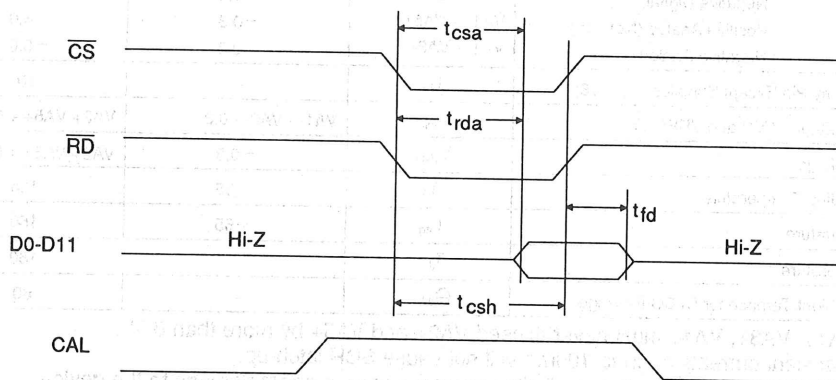
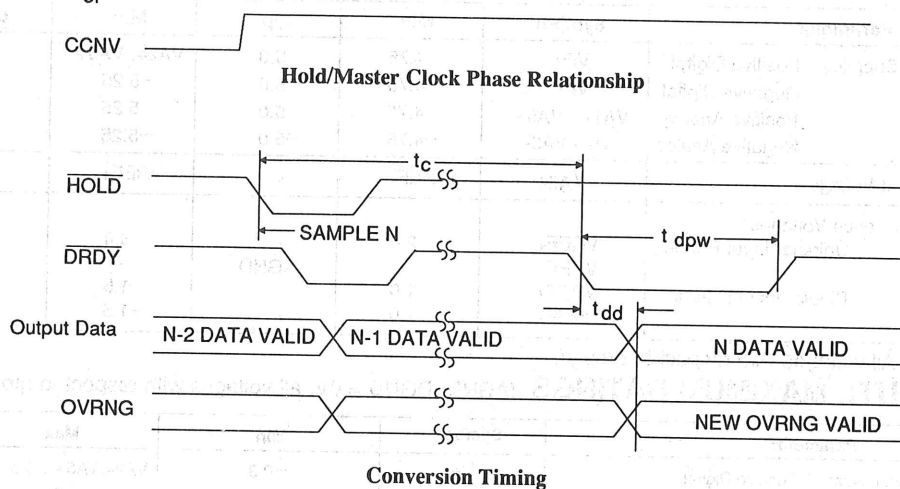
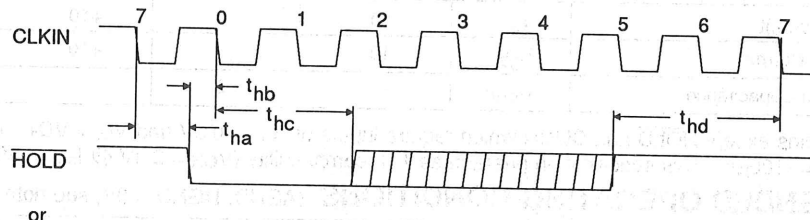
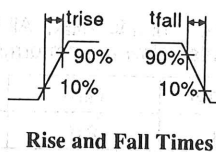
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:	$f_{CLK}$	3	-	8	MHz
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input (Note 8) Any Digital Output	$t_{rise}$	-	- 20	1.0 -	$\mu s$ ns
Fall Times: Any Digital Input (Note 8) Any Digital Output	$t_{fall}$	-	- 20	1.0 -	$\mu s$ ns
HOLD/CLKIN Phase Relationship State 7 to HOLD Low HOLD Low to State 0 State 0 to HOLD High HOLD High to State 7	$t_{ha}$ $t_{hb}$ $t_{hc}$ $t_{hd}$	62.5 0 75 30	- - - -	- - - -	ns ns ns ns
Conversion Time (Note 9)	$t_c$	10	-	12	MCC*
DRDY Pulse Width	$t_{dpw}$	-	3	-	MCC*
Data Delay Time	$t_{dd}$	-	20	50	ns
Access Times: $\overline{CS}$ Low to Data Valid (Note 9) $\overline{RD}$ Low to Data Valid	$t_{csa}$ $t_{rda}$	- -	55 55	110 110	ns ns
Output Float Delay: $\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z	$t_{fd}$	-	40	110	ns
Cal Pulse Width: (Note 11) CAL high and $\overline{CS}$ Low	$t_{csh}$	2	-	-	MCC*
$\overline{RST}$ Pulse Width	$t_{rpw}$	2	-	-	MCC*

- Notes: 8.  $\overline{HOLD}$  and CLKIN should be driven with signals which have rise and fall times of 25 ns or faster.  
9. Conversion time in the Continuous Convert mode is a fixed 10 clock cycles.  
10. Data goes valid when both  $\overline{CS}$  and  $\overline{RD}$  are low simultaneously. Each access time assumes the other control input is already low or falls concurrently.  
11. If CAL is brought low while  $\overline{CS}$  is low, a calibration cycle will be initiated.

\* MCC = Master Clock Cycles; 1 MCC =  $1/f_{CLK}$

**Float Delay Test Circuits**





**DIGITAL CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ; All VA+ pins,  $V_{D+} = 5V \pm 5\%$ ;  
All VA- pins,  $V_{D-} = -5V \pm 5\%$ ) All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 12)	$V_{IH}$	2.0	-	-	V
Low-Level Input Voltage (Note 12)	$V_{IL}$	-	-	0.8	V
High-Level Output Voltage (Note 13)	$V_{OH}$	$V_{D+} - 1.0V$	-	-	V
Low-Level Output Voltage $I_{out} = 1.6mA$	$V_{OL}$	-	-	0.4	V
Input Leakage Current	$I_{in}$	-10	-	+10	$\mu A$
3-State Leakage Current	$I_{OZ}$	-10	-	+10	$\mu A$
Digital Output Pin Capacitance	$C_{out}$	-	9	-	pF

Note: 12. All pins except  $\overline{HOLD}$  and CLKIN which require inputs of  $V_{IL} = 0.5V$  and  $V_{IH} = V_{D+} - 0.5V$ .  
13.  $I_{out} = -100\mu A$ . This specification guarantees TTL compatibility ( $V_{OH} = 2.4V$  @  $I_{out} = -40\mu A$ ).

**RECOMMENDED OPERATING CONDITIONS** ( $AGND$ ,  $DGND = 0V$ , see note 14).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	$V_{D+}$	4.75	5.0	$V_{A2+}, V_{A5+}$	V
Negative Digital	$V_{D-}$	-4.75	-5.0	-5.25	V
Positive Analog	$V_{A1+} - V_{A5+}$	4.75	5.0	5.25	V
Negative Analog	$V_{A1-} - V_{A3-}$	-4.75	-5.0	-5.25	V
Analog Input Voltage	$V_{AIN}$	$V_{REF-}$	-	$V_{REF+}$	V
Analog Reference Voltages					
Unipolar Input Range	$V_{REF+}$	2.0	-	3.0	V
	$V_{REF-}$	-	$AGND$	-	V
Bipolar Input Range	$V_{REF+}$	1.0	-	1.5	V
	$V_{REF-}$	-1.0	-	-1.5	V

Notes: 14. All voltages with respect to ground.

**ABSOLUTE MAXIMUM RATINGS** ( $AGND$ ,  $DGND = 0V$ , all voltages with respect to ground).

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive Digital	$V_{D+}$	-0.3	$V_{A2+}, V_{A5+} + 0.3$	V
Negative Digital	$V_{D-}$	0.3	-6.0	V
Positive Analog (Note 15)	$V_{A1+} - V_{A5+}$	-0.3	6.0	V
Negative Analog	$V_{A1-} - V_{A3-}$	0.3	-6.0	V
Input Current, Any Pin Except Supplies (Note 16)	$I_{in}$	-	+10	mA
Analog Input Voltage ( $A_{IN}$ and $V_{REF}$ pins)	$V_{INA}$	$V_{A1-} - V_{A3-} - 0.3$	$V_{A2+}, V_{A5+} + 0.3$	V
Digital Input Voltage	$V_{IND}$	-0.3	$V_{A2+}, V_{A5+} + 0.3$	V
Ambient Operating Temperature	$T_A$	-55	125	$^{\circ}C$
Storage Temperature	$T_{slg}$	-65	150	$^{\circ}C$
Junction Temperature	$T_J$	-	160	$^{\circ}C$
Junction to Ambient Tempco for CLCC Package	$\Theta_{JA}$	-	60	$^{\circ}C/W$

Notes: 15.  $V_{A1+}$ ,  $V_{A3+}$ ,  $V_{A4+}$  must never exceed  $V_{A2+}$  and  $V_{A5+}$  by more than 0.3V.

16. Transient currents of up to 100mA will not cause SCR latch-up.

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

## THEORY OF OPERATION

To achieve high speed and high accuracy, the CS5412 implements a standard 2-step flash A/D conversion using a self-calibrating architecture. Throughput is further maximized using pipelined acquisition and settling times as well as overlapped conversion cycles.

### 2-Step Flash A/D Conversion

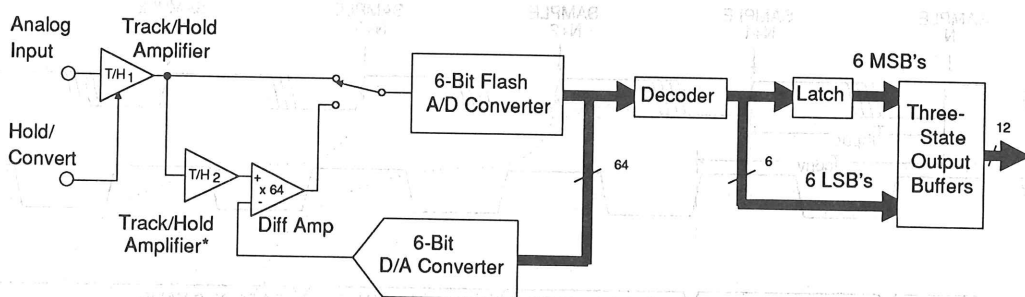
The fastest method of performing A/D conversion is the brute-force single-step flash approach, for which an N-bit conversion involves comparing the analog input to  $2^N - 1$  graduated voltage levels. The outputs from the  $2^N - 1$  comparators are then processed and encoded into the proper binary format. The major limitation to this technique is that the number (and accuracy requirements) of comparators doubles with each additional bit of resolution. Thus, single-step flash converters are impractical today at greater than 8 or 10 bits of resolution.

The 2-step technique that the CS5412 uses employs slightly more complex sub-circuit blocks to achieve high resolution and results in negligible speed degradation. As shown in Figure 1, the CS5412 consists of a track-and-hold amplifier (T/H<sub>1</sub>), a 6-bit flash ADC, a 6-bit DAC, and a differential amplifier. When the convert command is issued, T/H<sub>1</sub> holds the analog input signal and the flash ADC converts the six MSB's

(most-significant-bits) of the output word. The MSB's, once decoded, are latched. The flash converter's output is also loaded into the DAC. The DAC's output therefore represents the analog input less the quantization error of the first 6-bit flash conversion. This signal is then subtracted from the original analog input to yield the quantization error, which is then multiplied by 64 ( $2^6$ ) and again applied to the flash ADC to yield the six LSB's (least-significant-bits). In effect, the first 6-bit flash forms the transfer function into 64 segments which are then filled in with 64 codes each by the second 6-bit flash. This yields a total of 4096 codes ( $64 \times 64$ ) for 12-bit resolution.

### Calibration

The CS5412 uses several calibration techniques to insure 12-bit accuracy over time and temperature. A unique reference generating circuit provides the 64 graduated reference levels for the flash ADC and DAC. Critical to the CS5412's overall linearity, these references are continually adjusted to 12-bit accuracy during device operation. This background adjustment process is completely transparent to the user and results in less than  $\pm 1/2$  LSB nonlinearity. Also, all comparators in the flash ADC are auto-zeroed to avoid differential linearity errors at the 64 segment boundaries due to noise and/or offsets in the comparators.



\* Used in CS5412 to pipeline acquisition time.

Figure 1. Block Diagram of 2-Step Flash A/D Converter

The CS5412 also uses digital correction schemes. An on-chip microcontroller manipulates dedicated MDAC's to set the gain and offset of the 6-bit flash ADC; this insures less than  $\pm 1/2$  LSB overall full-scale and offset errors in the CS5412. Gain and offset are similarly calibrated in the differential amplifier to avoid linearity errors at the 64 segment boundaries.

Upon power-up, the CS5412 is reset in hardware or software to initially calibrate the device. Calibration can be similarly initiated at any later time throughout operating life to insure 12-bit accuracy independent of environmental conditions.

### Pipelined Timing

To achieve throughput rates up to 1MHz, the CS5412 pipelines settling times in both the sampling and conversion processes. The CS5412 can actually begin a conversion cycle while still operating on the previous sample. As shown in Figure 2, the *Hold and Convert* command for Sample N+1 can be issued before data from Sample N is valid at the output. By definition, the throughput time of the CS5412 is shorter than the conversion time due to the overlapped conversion cycles. Compared to a non-pipelined 1MHz ADC, the CS5412 provides the same 1MHz throughput, only the output data is delayed slightly in time (1.25 $\mu$ s delay through the ADC rather than 1 $\mu$ s).

The CS5412 also uses a second track-and-hold amplifier (termed  $T/H_2$  in Figure 3) to pipeline the converter's acquisition time. As shown in Figure 3,  $T/H_2$  holds the output from  $T/H_1$  valid for the second flash conversion, *Flash 2*. This allows  $T/H_1$  to release and acquire the analog input signal during the second flash conversion, allowing another *Hold & Convert* command to be issued even before the completion of *Flash 2*.

### DIGITAL CIRCUIT CONNECTIONS

In addition to master clock and sampling connections which set the converter's timing, the CS5412 offers an *Overrange* output, 3-state output buffers, and flexible control interface. The CS5412 can therefore connect directly to a microprocessor's data and control busses or can be operated in a stand-alone mode.

#### Master Clock

The CS5412 operates from a master clock reference which must be supplied in the form of either a crystal or external clock. A crystal can be tied across the CLKIN and XIN pins, or alternatively, the CS5412 can be synchronized to the external system by driving CLKIN with a CMOS-compatible clock (XIN left floating). If the master clock is shut off while the CS5412 is powered up, an internal oscillator will start-up to keep all in-

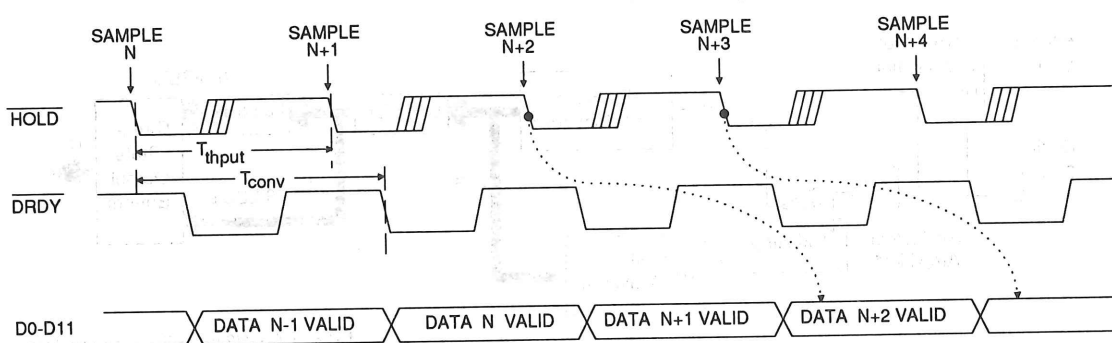


Figure 2. Pipelined Conversion Cycles

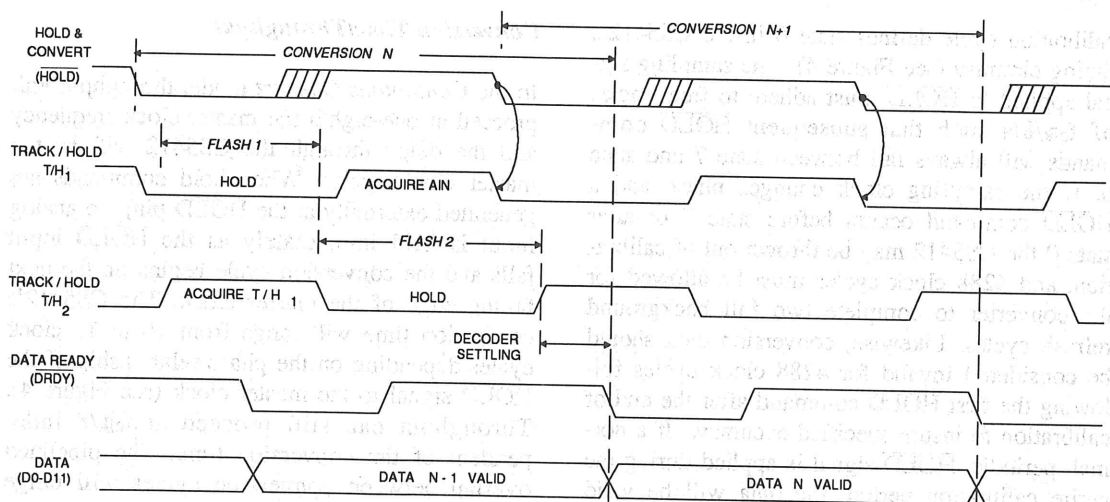


Figure 3. Pipelined Acquisition and Settling Times.

3

ternal dynamic logic refreshed. This internal oscillator should not be used for conversions. Clock cycles can be selectively skipped at any time, but the clock's average frequency should never drop below the device's minimum specification (see Switching Characteristics).

### Sampling/Initiating Conversions

There are two methods of controlling the CS5412's sampling/conversion timing. First, the CS5412 has a **HOLD** input which, on a falling edge, places the input track-and-hold amplifier in the hold state and initiates a conversion cycle. The CS5412 also features a *Continuous Convert* mode (**CCNV** and **HOLD** high) in which hold commands are internally generated every eight master clock cycles. The sampling/throughput rate is therefore controlled by adjusting the master clock frequency and there is no need to generate a sampling clock.

When **CCNV** is brought high with the proper relationship to **CLKIN** (shown in the timing diagrams), the next falling clock edge defines state 0.

Lower sampling rates can be created in the *Continuous Convert* mode by running the CS5412 at full throughput and decimating the output, selectively reading only a fraction of the available samples. Variable sampling rates can be implemented in this manner using a programmable divider on the **DRDY** output. When operating in the *Continuous Convert* mode, attention should be paid to jitter on the master clock, since jitter will directly affect sampling purity.

If the phase of sampling must be precisely controlled, the **HOLD** input must be used since the hold signal is internally-generated in the *Continuous Convert* mode. A falling edge on **HOLD** places the internal track-and-hold amplifier in the hold state and signals a conversion cycle to begin on the next falling edge of the master clock. The **HOLD** input was designed for minimum aperture jitter and therefore requires CMOS-compatible logic levels (not TTL-compatible).

Due to the CS5412's refreshing the 64 reference levels in the background, **HOLD** commands must be synchronized to the master clock and can only occur at intervals of 8 master clock cycles. The first **HOLD** command after the start of a reset or



calibration cycle defines state 0 in the CS5412's timing circuitry (see Figure 4). The sampling signal applied to  $\overline{\text{HOLD}}$  must adhere to frequencies of  $f_{\text{CLK}}/8N$  such that subsequent  $\overline{\text{HOLD}}$  commands will always fall between state 7 and state 0. If the sampling clock changes phase and a  $\overline{\text{HOLD}}$  command occurs before state 7 or after state 0 the CS5412 may be thrown out of calibration, and 4288 clock cycles must be allowed for the converter to complete two full background refresh cycles. Likewise, conversion data should be considered invalid for 4288 clock cycles following the first  $\overline{\text{HOLD}}$  command after the end of calibration to insure specified accuracy. If a normal, periodic,  $\overline{\text{HOLD}}$  signal is applied during the entire calibration period, the data will be valid immediately after calibration, i.e. when  $\text{OVRNG}$  goes low.

Most often the sampling signal applied to  $\overline{\text{HOLD}}$  can be derived from the master clock. In these cases, the master clock is divided by 8, 16, 24, 32, etc. If sampling must be locked to some external clock source, a phase-locked loop can be used to generate a master clock signal for  $\text{CLKIN}$  from the sampling signal. In this instance jitter on the  $\overline{\text{HOLD}}$  input will directly affect sampling purity; however, the CS5412 will tolerate significant jitter on the master clock without loss of accuracy (assuming the  $\overline{\text{HOLD}}/\text{CLKIN}$  phase specifications are met).

### Conversion Time/Throughput

In the *Continuous Convert* mode, throughput will proceed at one-eighth the master clock frequency and the delay through the CS5412 will be ten master clock cycles. When hold commands are generated externally at the  $\overline{\text{HOLD}}$  pin, the analog input is held immediately as the  $\overline{\text{HOLD}}$  input falls and the conversion cycle begins on the next falling edge of the master clock. The CS5412's conversion time will range from 10 to 11 clock cycles depending on the phase relationship of the  $\overline{\text{HOLD}}$  signal to the master clock (see Figure 4). Throughput can still proceed at  $f_{\text{CLK}}/8$  independent of the conversion time. The pipelined overlap between conversion cycles will range from 2 to 3 clock cycles.

### Reset

Upon power-up, the CS5412 must be reset to guarantee a consistent starting condition and initially calibrate the device. A falling edge on the  $\overline{\text{RST}}$  pin clears internal logic and a rising edge initiates a calibration cycle which takes 6,052,445 master clock cycles to complete. The  $\overline{\text{RST}}$  input must remain low for at least 2 master clock cycles to be considered valid. A simple power-up reset circuit can be constructed by tying a capacitor from  $\overline{\text{RST}}$  to  $\text{DGND}$  and a resistor from  $\overline{\text{RST}}$  to  $\text{VD+}$ .

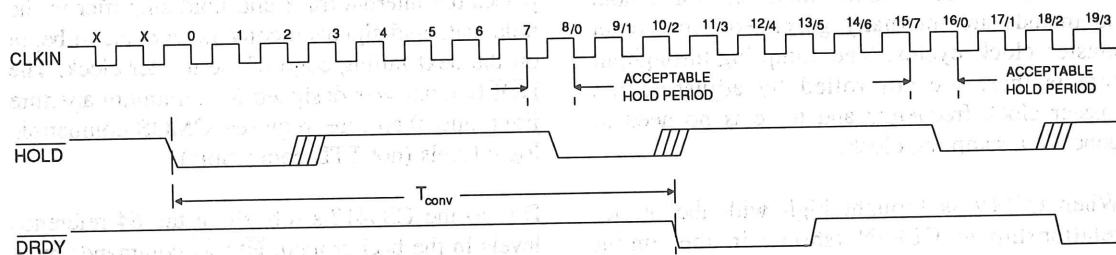


Figure 4. Hold / Conversion Timing.

Due to the CS5412's modest power dissipation and low temperature drift, no warm-up time is needed before reset to accommodate any self-heating effects. However, the voltage references (VREF+ and VREF-) should have stabilized to within their specified accuracies. The CS5412 can be reset later at any time during operation to initiate calibration. Reset overrides all other functions. If reset, the CS5412 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

### Overrange

The CS5412 will flag an overrange input at the OVRNG pin whenever the sampled analog input exceeds either the positive or negative reference voltage. If the sampled input exceeds VREF+, OVRNG will go high as DRDY falls, and all ones will be loaded into the output buffers. Similarly, if the analog input is below VREF-, OVRNG will go high as all zeroes are loaded into the output buffers. OVRNG should be latched on the rising edge of DRDY. The internal reference voltages are not affected by excursions of AIN outside the external reference voltages up to the supply voltages.

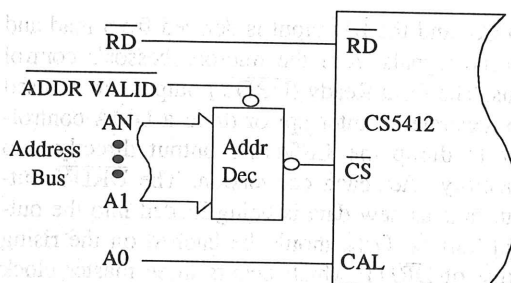


Figure 5. Microprocessor Controlled Operation.

Thirteen clock cycles after  $\overline{\text{RST}}$  or CAL transitions, OVRNG goes high. The OVRNG output remains high throughout a reset/calibration sequence and will return low after its completion. It can therefore be used to generate an interrupt indicating the CS5412 has completed calibration and is ready for operation.

### Microprocessor Controlled Operation

The CS5412 features 3-state output buffers and a control interface which allow the device to connect directly to a microprocessor's data and control busses. Strobing both  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  low enables the CS5412's 3-state output buffers with the converter's 12-bit output word. As shown in Figure 5, a decoded address is normally applied

$\overline{\text{CS}}$	$\overline{\text{RD}}$	CCNV	$\overline{\text{HOLD}}$	CAL	$\overline{\text{RST}}$	Function
0	0	X	X	0	1	Read Output Data
*	1	X	X	*	1	High Impedance Data Bus
1	X	X	X	X	1	High Impedance Data Bus
*	X	1	X	*	1	Continuous Convert Mode
*	X	0	$\downarrow$	*	1	Hold and Start Convert
X	X	X	X	X	$\downarrow$	Start Reset
0	X	X	X	$\downarrow$	X	Start Reset

\* Not critical to the operation specified. However,  $\overline{\text{CS}}$  should not be low with CAL transitioning low or a software reset will result.

Table 1. CS5412 Truth Table.

to  $\overline{CS}$ , and the  $\overline{RD}$  input is derived from read and strobe signals from the microprocessor's control bus. The Data Ready ( $\overline{DRDY}$ ) output can be used to generate an interrupt or drive a DMA controller to dump the CS5412's output directly into memory after each conversion. The  $\overline{DRDY}$  output falls as new data is being loaded into the output buffers. Data should be latched on the rising edge of  $\overline{DRDY}$  which occurs three master clock cycles after it falls.

The CS5412 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. The CS5412 should be synchronized to the digital system via CLKIN to avoid potential errors due to enabling the 3-state output buffers while the part is converting. Using TTL loads also increases the potential for crosstalk between the digital and analog portions of the system. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the CS5412's digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

### *Initiating Calibration*

In addition to the hardware reset, the CS5412 features a software calibration capability. Whenever CAL transitions low with  $\overline{CS}$  low, or  $\overline{CS}$  transitions high with CAL high, a calibration cycle will be initiated which is equivalent to the reset function. As shown in Figure 5, line A0 from the address bus can be connected to the CAL input when operating under microprocessor control. A read cycle from the CS5412's base address with A0 low will therefore retrieve output data while a read or write cycle with A0 high will initiate calibration. The CAL input is level sensitive, and like  $\overline{RST}$ , CAL overrides all other functions. Software-initiated calibrations can thus be used in lieu of a hardware reset at power-up.

### *Stand-Alone Operation*

The CS5412 can be operated in a stand-alone mode independent of intelligent control. In this mode,  $\overline{CS}$  and  $\overline{RD}$  are hard-wired low, permanently enabling the 3-state output buffers. A free-running condition is established when CAL is tied low, and  $\overline{HOLD}$  is continually strobed low or CCNV is held high. The CS5412's  $\overline{DRDY}$  output can be used to externally latch the output data if desired. The  $\overline{DRDY}$  output will strobe low for three master clock cycles after each conversion. Data will typically be unstable for 40ns after  $\overline{DRDY}$  falls, so it should be latched on the rising edge of  $\overline{DRDY}$ . This results in a total delay of 13 master clock cycles through the CS5412.

### *ANALOG CIRCUIT CONNECTIONS*

Like most 2-step flash A/D converters with internal track-and-hold amplifiers, the CS5412 offers a trivial load at its analog input compared to successive-approximation and single-step flash A/D converters. The reference connections similarly present high impedance loads. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

### *Analog Input and Reference Connections*

The CS5412's analog input range is defined by the voltages applied to the VREF- and VREF+ pins. The analog input (AIN) is referenced only to these reference voltages and is completely independent of the analog ground pins. The first code transition ideally occurs 1 LSB above VREF- and the last transition occurs 1 LSB below VREF+. The CS5412 can operate with a full-scale reference as low as 2.0V p-p, but signal-to-noise performance is maximized by using the full specified range of 3V p-p. Unipolar input ranges are achieved by tying VREF- to the system's analog ground and applying the reference voltage to VREF+. Bipolar input ranges are

achieved by applying positive and negative voltages of equal magnitude to VREF+ and VREF- respectively. In this configuration, coding is in offset-binary format.

The CS5412's analog input (AIN) pin looks directly into the noninverting terminal of the track-and-hold amplifier resulting in over 10M $\Omega$  input impedance and less than 10pF input capacitance.

The reference voltages at the +VREF and -VREF inputs are dynamically sampled. This pulsed charge load requires each of the reference inputs to be decoupled with a 0.1 $\mu$ F ceramic capacitor in parallel with a 3.3 $\mu$ F tantalum capacitor. The tantalum capacitors should be chosen to maintain 3.3 $\mu$ F minimum capacitance over the operating temperature range. To maintain DC accuracy the reference(s) should have an output impedance of less than 5 $\Omega$  at DC.

The CS3901 voltage reference provides +3V or  $\pm 1.5$ V for the CS5412 (see CS3901 data sheet).

### Grounding and Power Supply Decoupling

The CS5412 uses the analog ground connections, AGND1 and AGND2, only as stable, low impedance sources. No dc power currents flow through these connections, and they are completely independent of AIN and DGND. Still, AGND1 and AGND2 should be tied to the system's analog ground. The CS5412's analog input is referenced only to VREF+ and VREF-. Therefore, the analog input and reference voltages should be referred to the same ground potential (not necessarily AGND) which should be used as the entire system's analog ground. The optimal grounding configuration for the CS5412 utilizes one ground plane under the CS5412. Peripheral analog and digital circuitry should be partitioned on the circuit board and separate ground planes may or may not be used.

The digital and analog supplies are isolated within the CS5412 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. The analog supplies also have multiple connections which minimize lead inductances and power separate portions of the converter's analog circuitry. The decoupling scheme shown in the *System Connection Diagram* in Figure 9 provides optimal decoupling between the CS5412's digital circuitry and the various analog sections of the chip. Ceramic capacitors are acceptable for all decoupling, and they should be placed as close to the supply pins as possible. If significant low-frequency noise is present on the supplies, 10 $\mu$ F tantalum capacitors are recommended in parallel with 0.1 $\mu$ F ceramic capacitors on the  $\pm 5$ V rails.

*The positive digital power supply (VD+) should never exceed the positive analog supplies (VA2+ or VA5+) or the CS5412 could experience permanent damage.* If the two supplies are derived from separate sources, care should be taken that the analog supply comes up first at power-up. The *System Connection Diagram* in Figure 8 shows a decoupling scheme which allows the CS5412 to be powered from a single set of  $\pm 5$ V rails. The positive digital supply is derived from the analog supplies through a 10 $\Omega$  resistor to avoid the analog supply dropping below the digital supply. If this scheme is used, care must be taken to insure that any digital load currents (which flow through the 10 $\Omega$  resistors) do not cause the magnitude of the digital supplies to drop below their minimum specification of 4.75V.

As with any high-speed, high-precision A/D converter, the CS5412 requires careful attention to grounding and layout arrangements. The CDB5412 evaluation board is available for the CS5412, which eliminates the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5412 and can be quickly reconfigured to simulate any combination of sampling, calibration, and master clock conditions.

### Performance

Two types of performance test results are presented here. With FFT based tests, a pure sine wave is input to the CS5412, and an FFT analysis is performed on the output data. Figure 6 shows the resulting plot with a 100 kHz input sine. Notice the absence of any harmonic distortion and the overall Signal to (Noise + Distortion) value of 70.3 dB.

Figure 7 shows the FFT plot when two sine waves are simultaneously applied to the input. Notice the lack of sum and difference products, indicating very good linearity.

A second test looks for variation in the code width of the CS5412, as the input moves from -Full Scale to +Full Scale. This is called the Differential Non Linearity (DNL) and is expressed as a deviation from the ideal (in LSB), with 0 being perfect. Figure 8 shows the CS5412's excellent DNL performance with most codes being within  $\pm 0.1$  LSB of perfect.

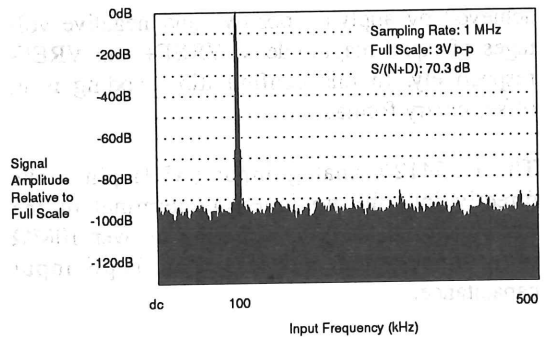


Figure 6. Typical CS5412 FFT Performance

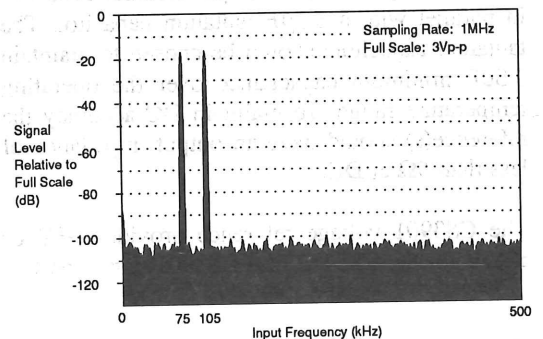


Figure 7. Intermodulation Distortion Performance

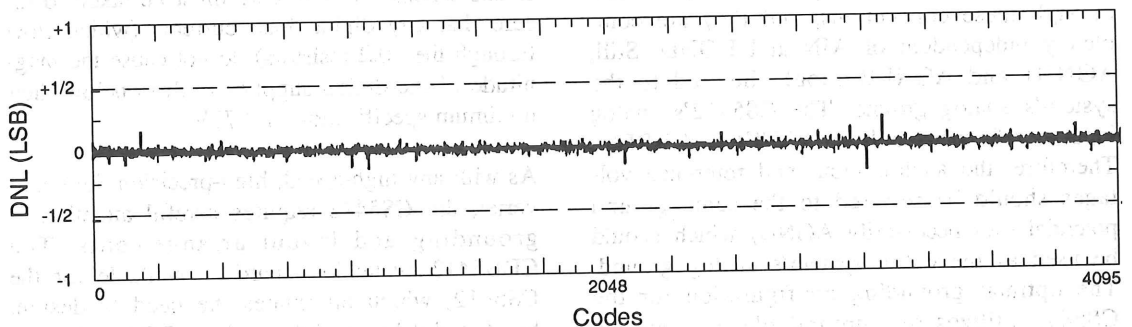
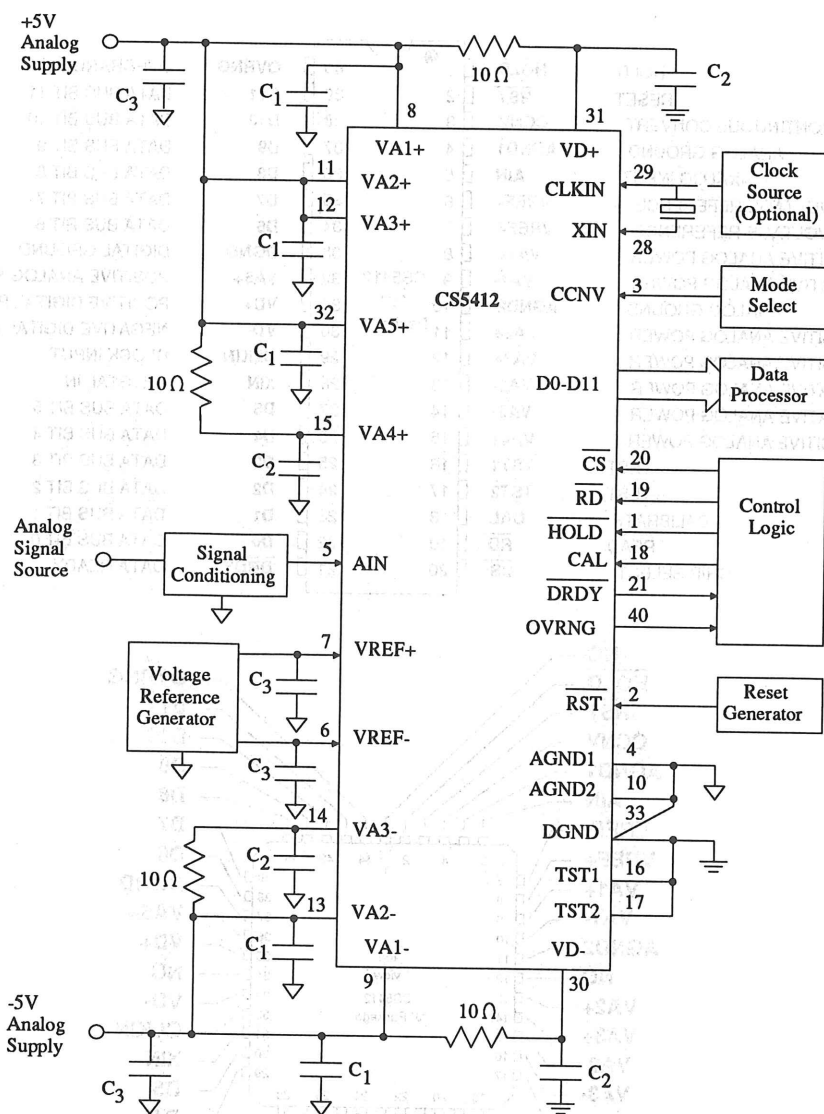


Figure 8. Typical CS5412 Differential Non-Linearity Plot



C1 - 0.01 $\mu$ F ceramic

C2 - 0.01 $\mu$ F in parallel with 0.1 $\mu$ F ceramic

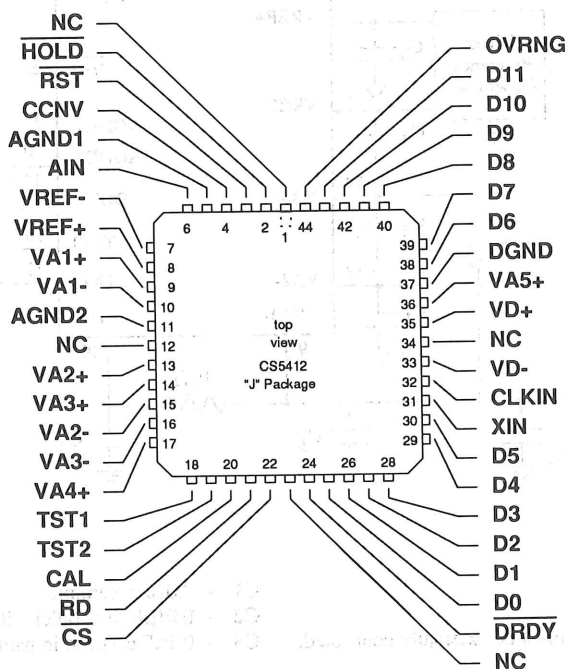
C3 - 0.1 $\mu$ F ceramic in parallel with 3.3  $\mu$ F tantalum

\*VA2+ and VA5+ must be externally connected.

**Figure 9. System Connection Diagram.**

### PIN DESCRIPTIONS

HOLD	<u>HOLD</u>	1	40	OVRNG	OVERRANGE
RESET	<u>RST</u>	2	39	D11	DATA BUS BIT 11
CONTINUOUS CONVERT	CCNV	3	38	D10	DATA BUS BIT 10
ANALOG GROUND	AGND1	4	37	D9	DATA BUS BIT 9
ANALOG INPUT	AIN	5	36	D8	DATA BUS BIT 8
NEGATIVE VOLTAGE REFERENCE	VREF-	6	35	D7	DATA BUS BIT 7
POSITIVE VOLTAGE REFERENCE	VREF+	7	34	D6	DATA BUS BIT 6
POSITIVE ANALOG POWER	VA1+	8	33	DGND	DIGITAL GROUND
NEGATIVE ANALOG POWER	VA1-	9	CS5412	VA5+	POSITIVE ANALOG POWER
ANALOG GROUND	AGND2	10	"C"	VD+	POSITIVE DIGITAL POWER
POSITIVE ANALOG POWER	VA2+	11	Package	VD-	NEGATIVE DIGITAL POWER
POSITIVE ANALOG POWER	VA3+	12	29	CLKIN	CLOCK INPUT
NEGATIVE ANALOG POWER	VA2-	13	28	XIN	CRYSTAL IN
NEGATIVE ANALOG POWER	VA3-	14	27	D5	DATA BUS BIT 5
POSITIVE ANALOG POWER	VA4+	15	26	D4	DATA BUS BIT 4
TEST	TST1	16	25	D3	DATA BUS BIT 3
TEST	TST2	17	24	D2	DATA BUS BIT 2
CALIBRATE	CAL	18	23	D1	DATA BUS BIT 1
READ	<u>RD</u>	19	22	D0	DATA BUS BIT 0
CHIP SELECT	<u>CS</u>	20	21	DRDY	DATA READY





### **Power Supply Connections**

**VD+ - Positive Digital Power, PIN 31.**

Positive digital supply voltage. Nominally +5 volts.

**VD- - Negative Digital Power, PIN 30.**

Negative digital supply voltage. Nominally -5 volts.

**DGND - Digital Ground, PIN 33.**

Digital ground reference.

**VA+ - Positive Analog Power, PINS 8, 11, 12, 15, 32.**

Positive analog supply voltage. Nominally +5 volts.

**VA- - Negative Analog Power, PINS 9, 13, 14.**

Negative analog supply voltage. Nominally -5 volts.

**AGND - Analog Ground, PIN 4, 10.**

Analog ground reference.

### **Oscillator**

**CLKIN; XIN - Clock In, PIN 29; Crystal In, PIN 28.**

Used to generate the internal master clock. A crystal can be tied across the two pins or an external CMOS-compatible clock can be driven into CLKIN if XIN is left floating.

### **Digital Inputs**

 **$\overline{\text{HOLD}}$  - Hold Input, PIN 1.**

A negative transition on  $\overline{\text{HOLD}}$  puts the track-and-hold amplifier into the hold state and initiates the conversion sequence. Conversions must be synchronized with the master clock at  $\text{fCLK}/8N$  where  $N = 1, 2, 3$ . The  $\overline{\text{HOLD}}$  input is CMOS-compatible.

**CCNV - Continuous Convert, PIN 3.**

When held high throughput will proceed at  $1/8^{\text{th}}$  the master clock frequency. The  $\overline{\text{HOLD}}$  pin can be high or low but must not transition.

 **$\overline{\text{CS}}$  - Chip Select, PIN 20.**

Activates the  $\overline{\text{RD}}$  and  $\overline{\text{CAL}}$  inputs. When  $\overline{\text{CS}}$  is high, these inputs have no effect and the data bus (D0 through D11) is held in a high impedance state.

 **$\overline{\text{RD}}$  - Read, PIN 19.**

When held low with  $\overline{\text{CS}}$  also low, enables D0-D11.

Note: Pin numbers are for the DIP package.

**$\overline{\text{RST}}$  - Reset, PIN 2.**

When  $\overline{\text{RST}}$  transitions from low to high a full calibration is started 13 master clock cycles later indicated by OVRNG going high. OVRNG will return low when calibration is finished. Calibration takes 6,052,445 master clock cycles.

**CAL - Calibrate, PIN 18.**

Same as  $\overline{\text{RST}}$  except it is logically inverted and enabled by  $\overline{\text{CS}}$  going low.

**Analog Inputs****VREF+ - Positive Voltage Reference, PIN 7.**

Represents positive full scale voltage. Typically +1.5V with respect to AGND (bipolar system) or +3V with respect to AGND and VREF- (unipolar system).

**VREF- - Negative Voltage Reference, PIN 6.**

Represents negative full scale voltage. Typically -1.5V with respect to AGND (bipolar system) or tied to AGND (unipolar system).

**AIN - Analog Input, PIN 5.**

Analog input to the track-and-hold amplifier.

**Digital Outputs****OVRNG - Overrange, PIN 40.**

Goes high if the sampled analog input voltage exceeds VREF+ or VREF-. OVRNG also goes high during calibration cycles and can therefore be used to indicate end of calibration.

 **$\overline{\text{DRDY}}$  - Data Ready, PIN 21.**

Falls when new data is becoming available at the outputs. Returns high three master clock cycles later. Data should be retrieved on the rising edge of  $\overline{\text{DRDY}}$ .

**Digital Input/Outputs****D0 through D11 - Data Bus, PINS 22 thru 27, 34 thru 39.**

Three-state data bus where D11 is the MSB and D0 is the LSB. The output coding is binary for unipolar and offset binary for bipolar.

**Miscellaneous Pins****TST1 - Test, PIN 16.**

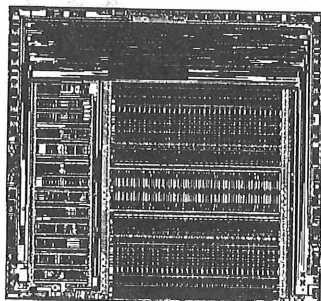
Reserved for factory use. Must be tied to DGND for proper device operation.

**TST2 - Test, PIN 17.**

Reserved for factory use. Must be tied to DGND for proper device operation.

Note: Pin numbers are for the DIP package.

## DIE INFORMATION



CS5412-YU

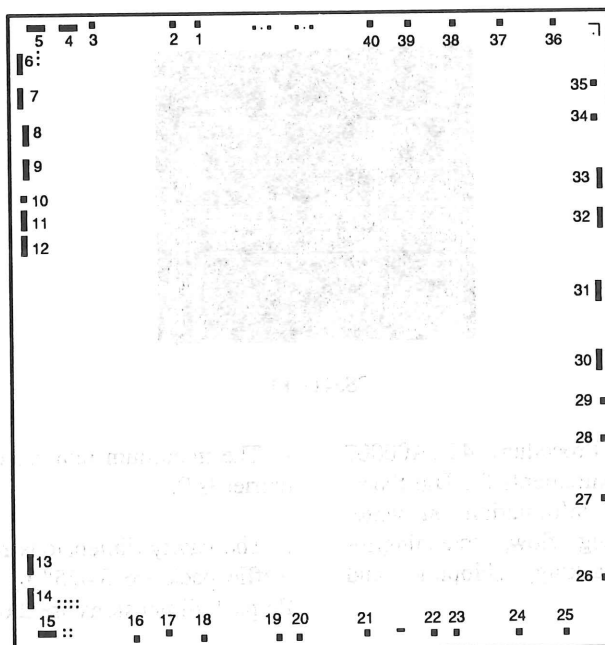
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Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

### Assembly Information

1. Die size shall be 0.374" by 0.348" ( $\pm 0.002$ ").
2. The die is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.
3. Die thickness shall be 0.0175"  $\pm 0.0035$ ". If tighter tolerances are required, contact the factory.
4. The maximum number of die per waffle pack carrier is 9.
5. The cavity dimensions for each die within the waffle pack are 0.425" by 0.425". Exterior waffle pack dimensions are 2.0" by 2.0"
6. The die requires no particular bonding sequence.
7. Each pin on the CS5412 has both ESD and latch-up protection circuitry. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.
8. Technical constraints limit the viability of accurate performance measurements of precision analog IC's at wafer probe. Although high yield to the limits listed in the specification tables is anticipated, no guarantee is given for unpackaged die product.

## CS5412-YU Bonding Diagram



1 - <u>HOLD</u>	21 - <u>DRDY</u>
2 - <u>RST</u>	22 - <u>D0</u>
3 - <u>CCNV</u>	23 - <u>D1</u>
4 - <u>AGND1</u>	24 - <u>D2</u>
5 - <u>AIN</u>	25 - <u>D3</u>
6 - <u>VREF-</u>	26 - <u>D4</u>
7 - <u>VREF+</u>	27 - <u>D5</u>
8 - <u>VA1+</u>	28 - <u>XIN</u>
9 - <u>VA1-</u>	29 - <u>CLKIN</u>
10 - <u>ANGD2</u>	30 - <u>VD-</u>
11 - <u>VA2+</u>	31 - <u>VD+</u>
12 - <u>VA3+</u>	32 - <u>VA5+</u>
13 - <u>VA2-</u>	33 - <u>DGND</u>
14 - <u>VA3-</u>	34 - <u>D6</u>
15 - <u>VA4+</u>	35 - <u>D7</u>
16 - <u>TST1</u>	36 - <u>D8</u>
17 - <u>TST2</u>	37 - <u>D9</u>
18 - <u>CAL</u>	38 - <u>D10</u>
19 - <u>RD</u>	39 - <u>D11</u>
20 - <u>CS</u>	40 - <u>OVRNG</u>

## DEFINITIONS

**Peak Harmonic or Spurious Noise** (More accurately, Signal to Peak Harmonic or Spurious Noise) - The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

**Total Harmonic Distortion** - Ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

**Signal-to-(Noise plus Distortion)** - Ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc). Expressed in decibels.

**Linearity Error** - The deviation of the worst code width center, out of all 4096 codes, from a straight line. The straight line is determined by using a least squares fit algorithm from the measured points. Units in LSB's.

**Differential Nonlinearity** - The deviation of a code's width from the ideal width. Units in LSB's.

**Full Scale Error** - The deviation of the last code transition from the ideal ( $V_{REF} + 1 \text{ LSB}$ ). Units in LSB's.

**Offset Error** - The deviation of the first code transition from the ideal ( $V_{REF} - 1 \text{ LSB}$ ). Units in LSB's.

**Aperture Time** - The time required after the hold command is issued for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

**Aperture Jitter** - The range of variation in the aperture time. Effectively a "sampling window" which ultimately dictates the maximum input slew rate acceptable for a given accuracy. Units in picoseconds.

## Ordering Guide

Model	Throughput	Signal to (Noise plus Distortion)	Linearity Error	Temp Range	Package
CS5412-JC1	1 MHz	65 dB	± 2.0 LSB	0 to 70 °C	40-Pin Ceramic SB DIP
CS5412-JJ1	1 MHz	65 dB	± 2.0 LSB	0 to 70 °C	44-Pin J Lead CLCC
CS5412-KC1	1 MHz	68 dB	± 1.0 LSB	0 to 70 °C	40-Pin Ceramic SB DIP
CS5412-KJ1	1 MHz	68 dB	± 1.0 LSB	0 to 70 °C	44-Pin J Lead CLCC
CS5412-AC1	1 MHz	65 dB	± 2.0 LSB	-40 to +85 °C	40-Pin Ceramic SB DIP
CS5412-BC1	1 MHz	68 dB	± 1.0 LSB	-40 to +85 °C	40-Pin Ceramic SB DIP
CS5412-SC1	1 MHz	65 dB	± 3.0 LSB	-55 to +125 °C	40-Pin Ceramic SB DIP
CS5412-TC1	1 MHz	68 dB	± 2.0 LSB	-55 to +125 °C	40-Pin Ceramic SB DIP
CS5412-SJ1	1 MHz	65 dB	± 3.0 LSB	-55 to +125 °C	44-Pin J Lead CLCC
CS5412-TJ1	1 MHz	68 dB	± 2.0 LSB	-55 to +125 °C	44-Pin J Lead CLCC

CS5412-YU 1 MHz Unpackaged Die

### MIL-STD-883C Rev.B Versions

SMD Number: 5962-90957

Refer to SMD for accuracy and package suffixes.

## CS5412 Evaluation Board

### Features

- Throughout Rates to 1MHz
- Jumper Selectable  
Unipolar/Bipolar Input Range  
Continuous Conversion
- Buffered 12-Bit Data
- Optional Phase-Locked-Loop to  
Synchronize to Sampling Signal
- Adjustable Voltage Reference
- PC/uP-Compatible Header Connection

### General Description

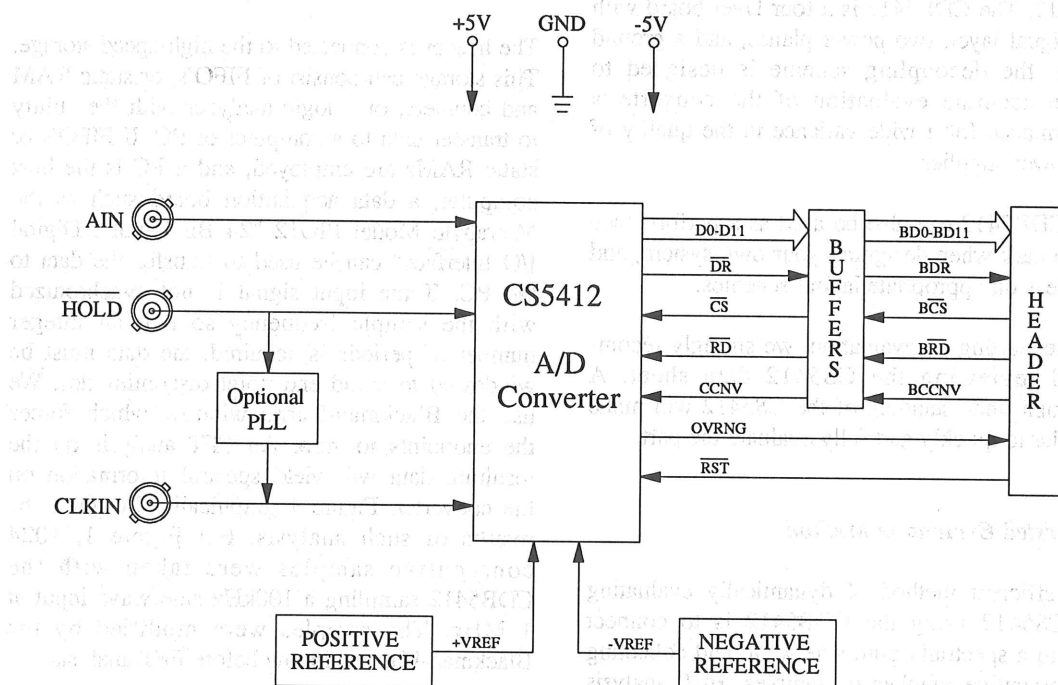
The CDB5412 is a completed, tested evaluation board for the CS5412 12-bit high-speed analog to digital converter. It includes a CS5412 and all of the components necessary to quickly and thoroughly verify the converter's performance under a wide variety of operating conditions.

On-board circuitry includes voltage references and clock circuitry, plus data buffers, so that the user need only supply power and an input signal to exercise the CS5412.

An on-board phase-locked-loop may be used to simulate systems that have a periodic sample clock not synchronized to a system clock, or where a clock 8 times the sampling clock is not available.

**ORDERING INFORMATION:** CDB5412

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## GENERAL DESCRIPTION

The CDB5412 Evaluation Board is a stand-alone environment for easy lab evaluation of the CS5412 High-Speed Analog-to-Digital Converter. Positive and negative references are included on the board and can be configured for  $\pm 1.5$  volt bipolar or 0-to-3 volt unipolar operation. The digital output of the CS5412 is buffered and series terminated allowing the board to drive twisted-pair ribbon cable. The CDB5412 also includes an optional phase-locked-loop (PLL) that will generate the requisite master clock given a periodic sample clock. When supplied with the necessary +5 volt and -5 volt power supplies and an analog signal source, the CDB5412 will provide converted data at the 40 pin header.

The CDB5412 is designed to allow easy and thorough evaluation of the performance of the CS5412. The CDB5412 is a four layer board with one signal layer, two power planes, and a ground plane; the decoupling scheme is designed to insure accurate evaluation of the converter's performance for a wide variance in the quality of the power supplies.

The CDB5412 can also be used as a performance benchmark when designing your own system, and for ideas on appropriate layout schemes.

Before starting an evaluation, we strongly recommend reviewing the CS5412 data sheet. A thorough understanding of the CS5412 will make it easier to quickly and fully evaluate the part.

### *Suggested Evaluation Method*

One efficient method of dynamically evaluating the CS5412 using the CDB5412 is to connect AIN to a spectrally pure sine wave and collecting a consecutive number of samples. FFT analysis can then be done on the samples to produce signal-to-noise and signal-to-distortion ratios.

Equipment needed consist of the following:

- CDB5412 Evaluation Board
- Good split power supply capable of supplying +5V and -5V.
- A spectrally pure sine wave generator such as the Krohn-Hite Model 4400A "Ultra-Low Distortion Oscillator"
- High-speed data storage
- Computer/PC capable of acquiring data from high-speed data storage
- A software routine to perform a Fast Fourier Transform (FFT)

The sine-wave generator supplies the analog signal, AIN, to the CDB5412. Converted data will appear at the header since the board is, by default, in the continuous convert mode.

The header is connected to the high-speed storage. This storage can consist of FIFO's, or static RAM and counters, or a logic analyzer with the ability to transfer data to a computer or PC. If FIFO's or static RAMs are employed, and a PC is the host computer, a data acquisition board such as the Metrabyte Model PIO12 "24 Bit Parallel Digital I/O Interface" can be used to transfer the data to the PC. If the input signal is not synchronized with the sample frequency so that an integer number of periods is acquired, the data must be windowed to avoid end point discontinuities. We use the Blackman-Harris window which forces the endpoints to zero. An FFT analysis on the resulting data will yield spectral information on the converter. Figure 1 graphically illustrates the results of such analysis. For Figure 1, 1024 consecutive samples were taken with the CDB5412 sampling a 100kHz sine wave input at 1 MHz. The samples were modified by the Blackman-Harris window before FFT analysis.

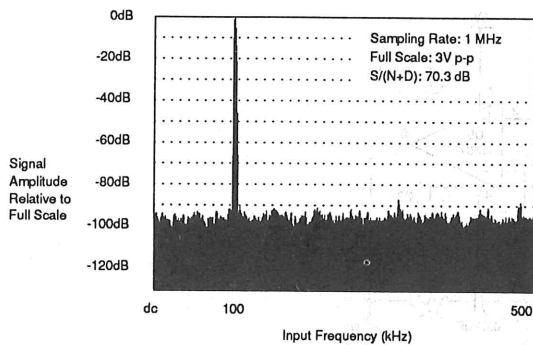


Figure 6. Typical CS5412 FFT Performance

References:

F.J. HARRIS, "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transfer", Proc. IEEE, Vol. 66, No. 1, Jan. 1978, pp. 51-83.

G.D. BERGLAND & M.T. DOLAN, "Fast Fourier Transform Algorithms", Programs for Digital Signal Processing, IEEE Press: 0-87942-127-4, Section 1.2.

## BOARD DESCRIPTION

### MODES

#### Continuous Convert

The default mode for the CDB5412 is continuous convert (CCNV) active with the PLL inactive. Therefore, the CS5412 is always converting and the **HOLD** signal is not used. The part can be taken out of continuous convert mode in one of two ways, either by placing a strap jumper on J6 or by driving BCCNV at the stake header low. Once out of continuous convert mode, the **HOLD** signal must be driven. **HOLD** is described in greater detail in the "Inputs" section.

#### Unipolar/Bipolar

The CDB5412 board is factory calibrated for bipolar mode ( $A_{IN} = \pm 1.5 \text{ V}_{\text{peak}}$ ). In bipolar mode, strap jumpers are placed on J3 and J5 (both marked with a "B") which are located in the Negative Reference, Figure 2, and the Positive Reference, Figure 3.

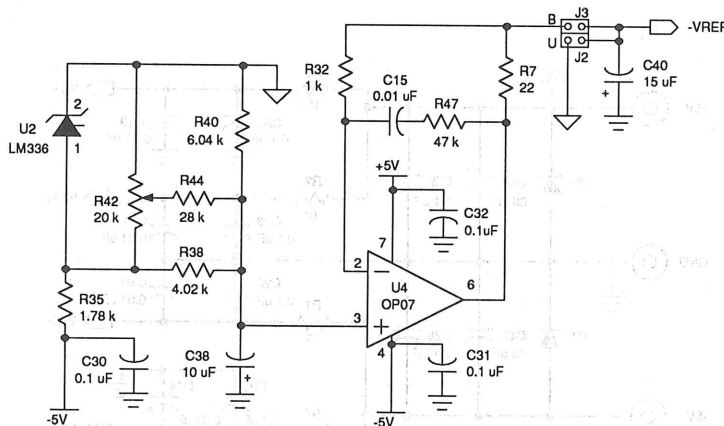


Figure 2. Negative Reference

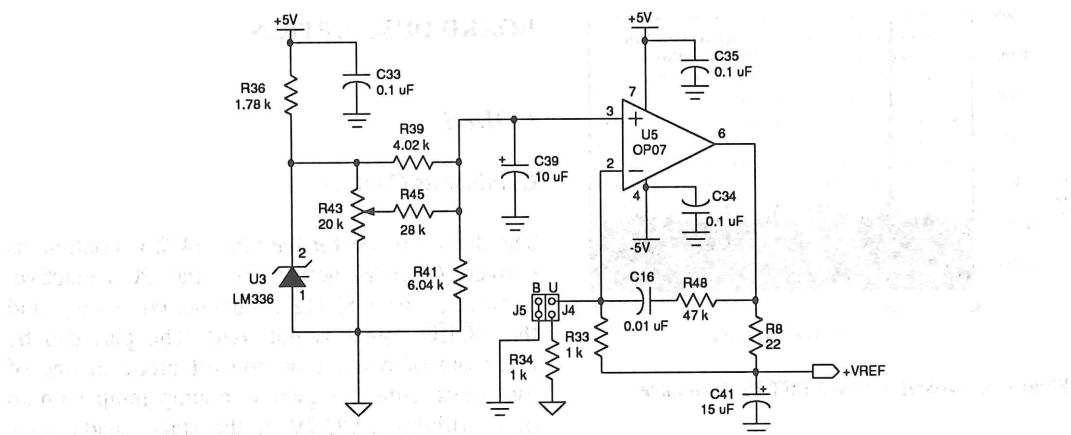


Figure 3. Positive Reference

To operate the board in unipolar mode (AIN = AGND to +3 Vpeak), move the strap jumpers to J2 and J4 (both marked with a "U"). The positive reference pot, R43, must be calibrated to +3.000 volts at +VREF (pin 7) of the CS5412 converter.

When receiving a new board, Crystal recommends that the reference voltages, +VREF and -VREF, be verified before operation. The pots located in their respective reference section may be

tweaked to calibrate the voltage level which should be measured at the CS5412 converter.

#### Calibration

Since the Reset switch provides a means to calibrate the part, the CAL pin is hard-wired to ground through jumper J1. The reset signal is also available at the stake header and can be driven by any source that can drive a 1 kΩ resistor connected to +5 volts (see Figure 5).

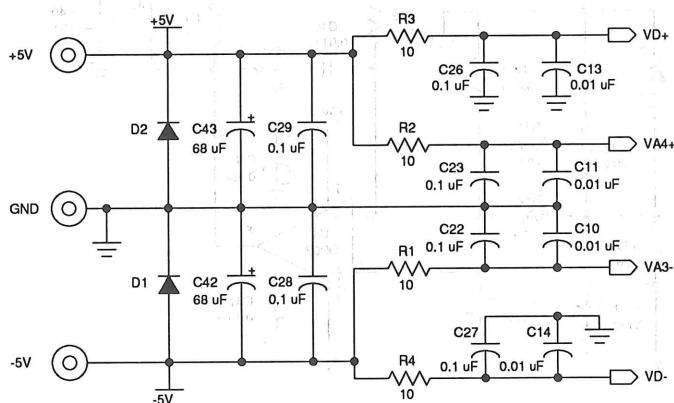


Figure 4. Power Supply



replaced with an appropriate resistor to low-pass filter the input noise.

In addition to the input filtering capability, R11 is available for impedance matching. If the source driving AIN has low impedance, an appropriate termination resistor should be soldered in R11. (see Figure 5.)

### Clock -CLKIN

The CDB5412 has an 8.0000 MHz crystal installed at the factory which generates a sample frequency of 1 MHz. If another sample frequency is desired, either replace the crystal or remove the crystal from its socket and use the CLKIN BNC to generate other master clock frequencies. R14 provides series termination of 51  $\Omega$ . R13 may be used for parallel termination but must be left open for the crystal to oscillate (factory setting). CLKIN can also be generated by the on-board PLL. The PLL, when active, will generate a CLKIN frequency eight times the frequency of

the  $\overline{\text{HOLD}}$  signal. For more information on the PLL, see the "Phase-Locked- Loop" section.

### Hold - $\overline{\text{HOLD}}$

As described in the Continuous Convert section, the CDB5412 is factory set not to use the  $\overline{\text{HOLD}}$  input. Driving the  $\overline{\text{HOLD}}$  input while the CS5412 is in the continuous convert mode will give erratic results. To use the  $\overline{\text{HOLD}}$  signal, the CCNV signal must be driven low by placing a strap jumper on J6 or by driving the BCCNV signal at the stake header low. As described in the CS5412 data sheet, the  $\overline{\text{HOLD}}$  signal must be modulo eight and synchronized to the master clock, CLKIN.

Since  $\overline{\text{HOLD}}$  must not be left floating, the factory configuration is a shorting wire in R10 (series termination) and a 47k  $\Omega$  resistor (R9) to ground. This configuration ties  $\overline{\text{HOLD}}$  to ground (through R9) and provides fairly high impedance when driving  $\overline{\text{HOLD}}$  externally.

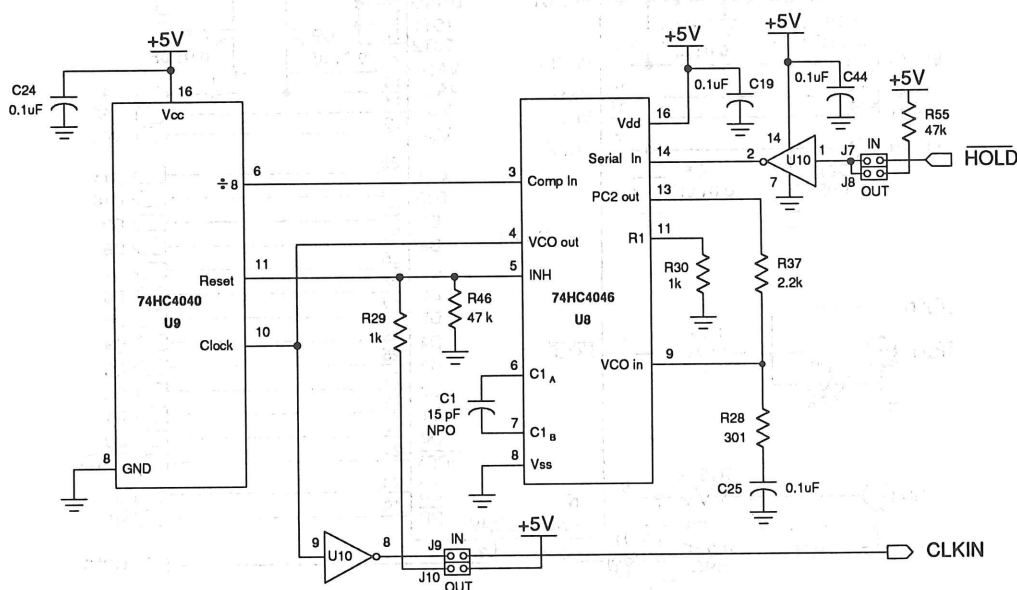


Figure 6. Phase-Locked-Loop

If the signal source used to drive  $\overline{\text{HOLD}}$  is low impedance, R9 should be replaced with the appropriate resistor. R10 can provide series termination.

## Phase-Locked-Loop - (PLL)

The CDB5412 contains an optional Phase- Locked-Loop (PLL) which can be used by systems containing a periodic sampling clock,  $\overline{\text{HOLD}}$ , but no master clock, CLKIN. The PLL generates a clock eight times the frequency of  $\overline{\text{HOLD}}$  and the PLL drives the CLKIN pin.

The schematic for the PLL is shown in Figure 6. Shorting jumpers on J8 and J10 (both marked "OUT") disable the PLL (factory setting). To enable the PLL move the jumpers from J8 and J10 to J7 and J9 (both marked "IN"). Since the CLKIN pin is driven by the PLL, the on-board crystal should be removed and the CLKIN BNC must not be driven or loaded by an external source.

The PLL will not work with a sampling signal,  $\overline{\text{HOLD}}$ , that is not periodic. The PLL is designed to work with a  $\overline{\text{HOLD}}$  signal range of 300 kHz to 1 MHz. To redesign the PLL for other frequencies see the National Semiconductor 74HC4046 PLL Data Sheet.

## OUTPUTS

The 12 data bits output from the CS5412 are buffered as shown in Figures 7 and 8, which minimize loading of the converters outputs. Series resistors are then used to minimize ringing when connected to twisted-pair ribbon cable. The +5 volt supply for the buffers is derived from the analog supply using the same low-pass RC network used on the digital supplies of the CS5412.

Three of the signals at the stake header are inputs to the board (Figure 8).  $\overline{\text{B\overline{C}S}}$  and  $\overline{\text{B\overline{R}D}}$  are pulled

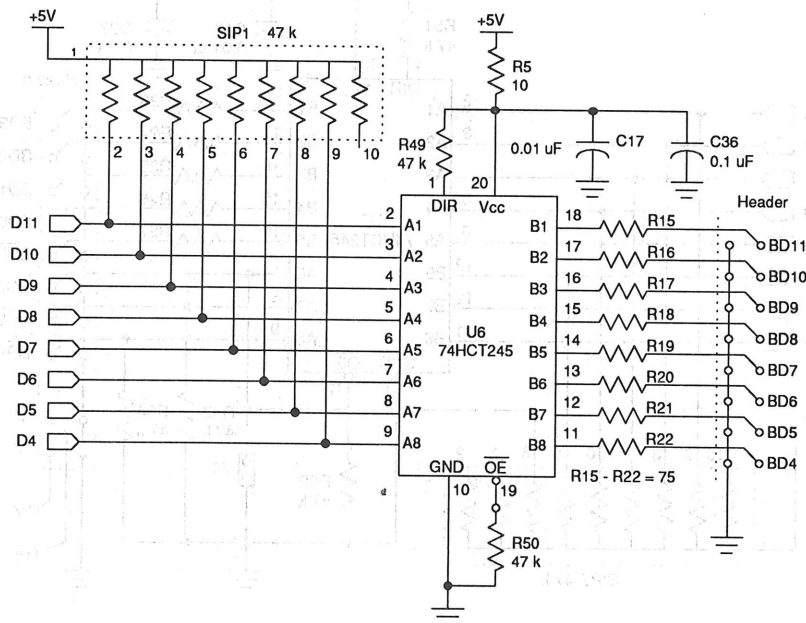


Figure 7. Upper Buffer

down to ground through a resistor allowing the CS5412 to continually output data as soon as it becomes available. The third input is a buffered continuous convert signal, BCCNV. By default this signal is pulled up to +5 volts through a resistor, which configures the CS5412 to convert at one eighth the master clock frequency. (The HOLD BNC must not be driven in this mode.)

The 20 stake header pins opposite the signal names are all tied to ground. Signals with a "B" prefix indicate buffered signals. The "X" and "Y" pins are unused and allow customization of the CDB5412 evaluation board.

Figure 9 illustrates the CDB5412 board layout to help in locating components.

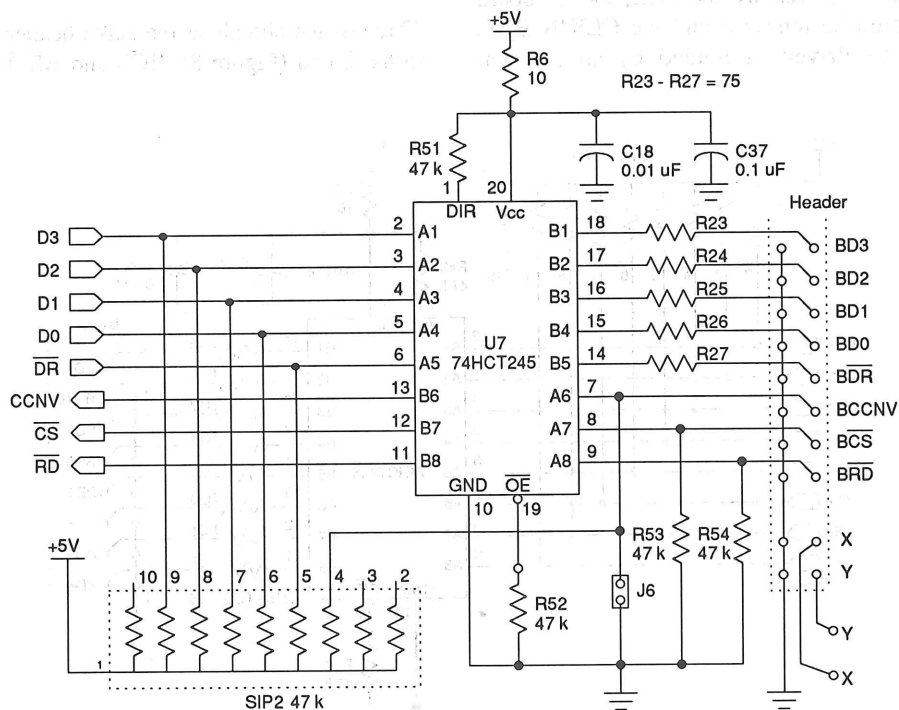


Figure 8. Lower Buffer



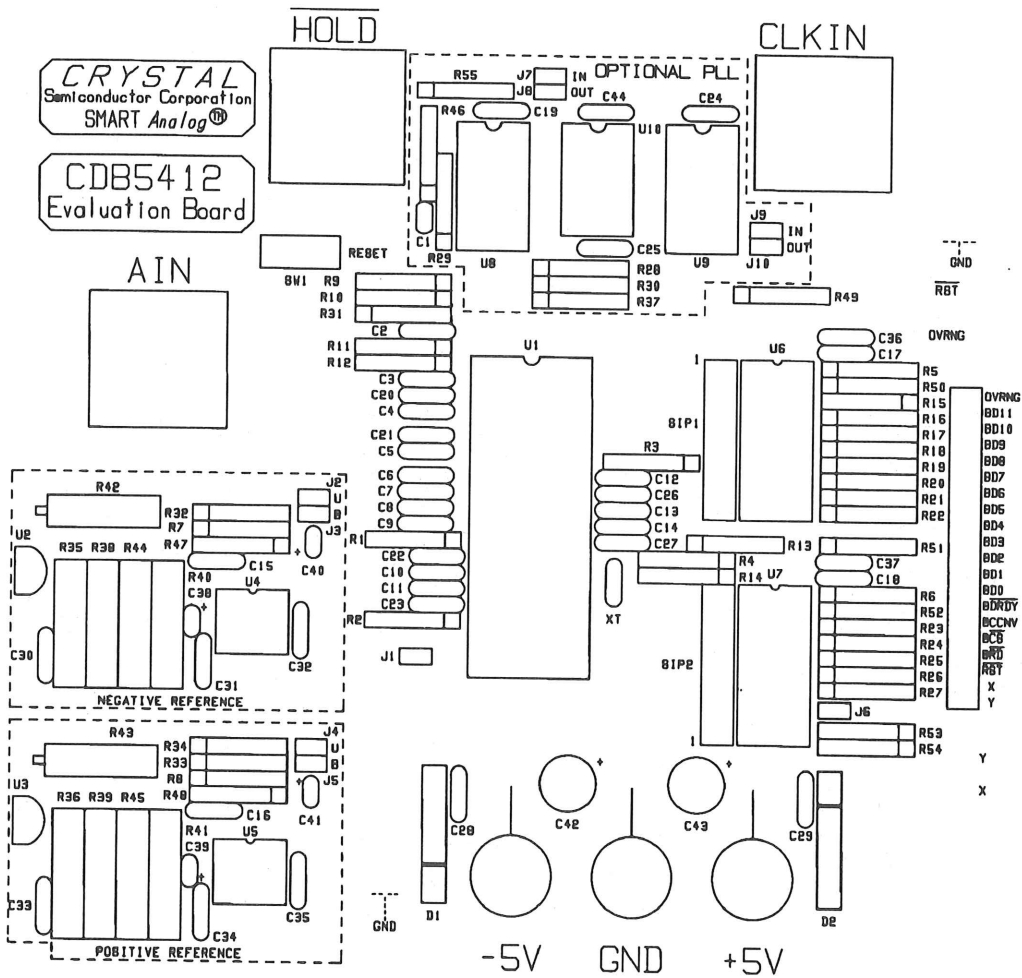


Figure 9. CDB5412 Board Layout

**•Notes•**

## Low-Cost, 16 & 20-Bit Measurement A/D Converter

### Features

- Monolithic CMOS ADC with Filtering  
6-Pole, Low-Pass Gaussian Filter
- Up to 4kHz Output Word Rates
- On Chip Self-Calibration Circuitry
  - Linearity Error:  $\pm 0.0003\%$
  - Differential Nonlinearity:  
CS5501: 16-Bit No Missing Codes (DNL  $\pm 1/8\text{LSB}$ )  
CS5503: 20-Bit No Missing Codes
- System Calibration Capability
- Flexible Serial Communications Port
  - $\mu\text{C}$ -Compatible Formats
  - 3-State Data and Clock Outputs
  - UART Format (CS5501 only)
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 25mW
  - $10\mu\text{W}$  Sleep Mode for Portable Applications
- Evaluation Boards Available

### General Description

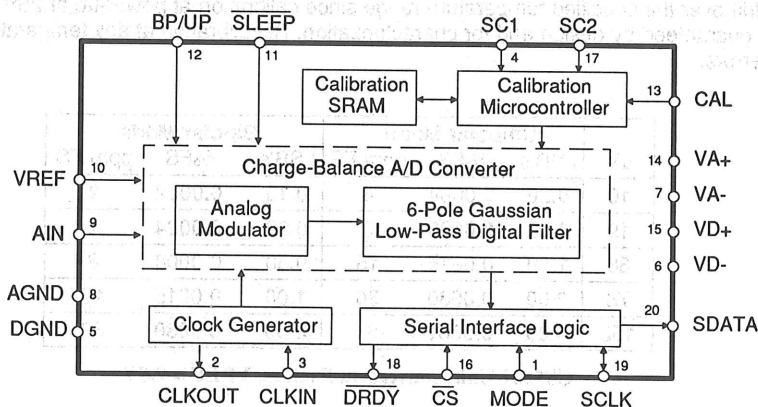
The CS5501 and CS5503 are low-cost CMOS A/D converters ideal for measuring low-frequency signals representing physical, chemical, and biological processes. They utilize charge-balance techniques to achieve 16-bit (CS5501) and 20-bit (CS5503) performance with up to 4kHz word rates at very low cost.

The converters continuously sample at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at up to a 4kHz rate. The converters' low-pass, 6-pole Gaussian response filter is designed to allow corner frequency settings from .1Hz to 10Hz in the CS5501 and .5Hz to 10Hz in the CS5503. Thus, each converter rejects 50Hz and 60Hz line frequencies as well as any noise at spurious frequencies.

The CS5501 and CS5503 include on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of typically less than  $1/2\text{LSB}$  for the CS5501 and less than  $4\text{LSB}$  for the CS5503. The devices can also be applied in system calibration schemes to null offset and gain errors in the input channel.

Each device's serial port offers two general purpose modes of operation for direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers. In addition, the CS5501's serial port offers a third, UART-compatible mode of asynchronous communication.

**ORDERING INFORMATION:** Page 3-273



**CS5501 ANALOG CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}, V_{D+} = 5V$ ;  $V_{A-}, V_{D-} = -5V$ ;  $V_{REF} = 2.5V$ ;  $CLKIN = 4.096MHz$ ; Bipolar Mode;  $MODE = +5V$ ;  $R_{source} = 750\Omega$  with a  $1nF$  to AGND at AIN (see Note 1); Digital Inputs: Logic 0 = GND; Logic 1 =  $V_{D+}$ ; unless otherwise specified.)

Parameter*		CS5501-A,B,C			CS5501-S,T			Units
		Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range		-40 to +85			-55 to +125			°C
Accuracy								
Linearity Error	-A,S -B,T -C	-	0.0015 0.0007 0.0003	0.003 0.0015 0.0012	-	- 0.0007	0.003 0.0015	±%FS ±%FS ±%FS
Differential Nonlinearity	T <sub>MIN</sub> to T <sub>MAX</sub>	-	±1/8	±1/2	-	±1/8	±1/2	LSB16
Full Scale Error	(Note 2)	-	±0.13	±0.5	-	±0.13	±0.5	LSB16
Full Scale Drift	(Note 3)	-	±1.2	-	-	±2.3	-	LSB16
Unipolar Offset	(Note 2)	-	±0.25	±1	-	±0.25	±1	LSB16
Unipolar Offset Drift	(Note 3)	-	±4.2	-	-	+3.0 -25.0	-	LSB16
Bipolar Offset	(Note 2)	-	±0.25	±1	-	±0.25	±1	LSB16
Bipolar Offset Drift	(Note 3)	-	±2.1	-	-	+1.5 -12.5	-	LSB16
Bipolar Negative Full Scale Error	(Note 2)	-	±0.5	±2	-	±0.5	±2	LSB16
Bipolar Negative Full Scale Drift	(Note 3)	-	±0.6	-	-	±1.2	-	LSB16
Noise (Referred to Output)		-	1/10	-	-	1/10	-	LSBrms (16)

- Notes:
1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the CS5501's source impedance requirements. For more information refer the text section *Analog Input Impedance Considerations*.
  2. Applies after calibration at the temperature of interest.
  3. Total drift over the specified temperature range since calibration at power-up at 25°C (see Figure 11). This is guaranteed by design and /or characterization. Recalibration at any temperature will remove these errors.

$\mu V$	Unipolar Mode			Bipolar Mode		
	LSB's	%FS	ppm FS	LSB's	%FS	ppm FS
10	0.26	0.0004	4	0.13	0.0002	2
19	0.50	0.0008	8	0.26	0.0004	4
38	1.00	0.0015	15	0.50	0.0008	8
76	2.00	0.0030	30	1.00	0.0015	15
152	4.00	0.0061	61	2.00	0.0030	30

CS5501 Unit Conversion Factors,  $V_{REF} = 2.5V$

\* Refer to the Specification Definitions immediately following the Pin Description Section.

### CS5503 ANALOG CHARACTERISTICS (T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>; V<sub>A+</sub>, V<sub>D+</sub> = 5V; V<sub>A-</sub>, V<sub>D-</sub> = -5V; V<sub>REF</sub> = 2.5V; CLKIN = 4.096MHz; Bipolar Mode; MODE = +5V; R<sub>source</sub> = 750Ω with a 1nF to AGND at AIN (see Note 1); unless otherwise specified.)

Parameter*		CS5503-A,B,C			CS5503-S,T			Units
		Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range		-40 to +85			-55 to +125			°C
Accuracy								
Linearity Error	-AS -B,T -C	-	0.0015	0.003	-	-	0.003	±%FS
		-	0.0007	0.0015	-	0.0007	TBD	±%FS
		-	0.0003	0.0012				±%FS
Differential Nonlinearity (No Missing Codes)	T <sub>MIN</sub> to T <sub>MAX</sub>	-	20		-	20	-	Bits
Full Scale Error (Note 2)		-	±4	±16	-	±4	±16	LSB <sub>20</sub>
Full Scale Drift (Note 3)		-	±19	-	-	±37	-	LSB <sub>20</sub>
Unipolar Offset (Note 2)		-	±4	±16	-	±4	±16	LSB <sub>20</sub>
Unipolar Offset Drift (Note 3)		-	±67	-	-	+48 -400	-	LSB <sub>20</sub>
Bipolar Offset (Note 2)		-	±4	±16	-	±4	±16	LSB <sub>20</sub>
Bipolar Offset Drift (Note 3)		-	±34	-	-	+24 -200	-	LSB <sub>20</sub>
Bipolar Negative Full Scale Error (Note 2)		-	±8	±32	-	±8	±32	LSB <sub>20</sub>
Bipolar Negative Full Scale Drift (Note 3)		-	±10	-	-	±20	-	LSB <sub>20</sub>
Noise (Referred to Output)		-	1.6	-	-	1.6	-	LSBrms (20)

3

μV	Unipolar Mode			Bipolar Mode		
	LSB's	%FS	ppm FS	LSB's	%FS	ppm FS
0.596	0.25	0.0000238	0.24	0.13	0.0000119	0.12
1.192	0.50	0.0000477	0.47	0.26	0.0000238	0.24
2.384	1.00	0.0000954	0.95	0.50	0.0000477	0.47
4.768	2.00	0.0001907	1.91	1.00	0.0000954	0.95
9.537	4.000	0.0003814	3.81	2.00	0.0001907	1.91

CS5503 Unit Conversion Factors, V<sub>REF</sub> = 2.5V

\* Refer to the Specification Definitions immediately following the Pin Description Section.

**ANALOG CHARACTERISTICS** (Continued)

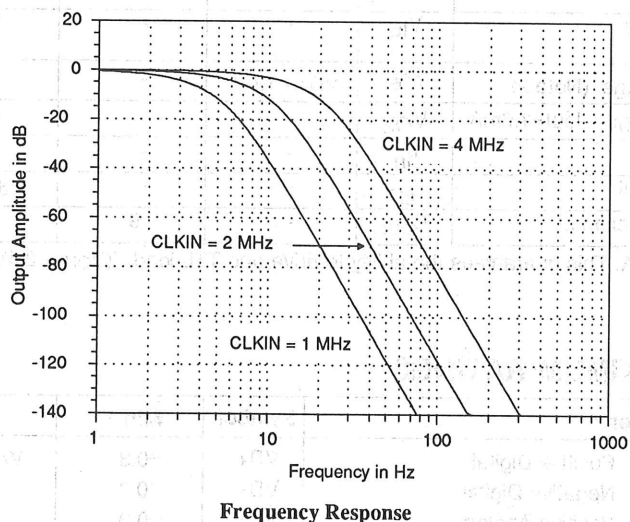
Parameter		CS5501/3-A,B,C			CS5501/3-S,T			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supplies								
DC Power Supply Currents								
	IA+	-	2	3.2	-	2	3.2	mA
	IA-	-	2	3.2	-	2	3.2	mA
	ID+	-	1	1.5	-	1	1.5	mA
	ID- (Note 4)	-	0.03	0.1	-	0.03	0.1	mA
Power Dissipation								
	SLEEP High	-	25	40	-	25	40	mW
	SLEEP Low (Note 4)	-	10	20	-	10	40	μW
Power Supply Rejection								
	Positive Supplies	-	70	-	-	70	-	dB
	Negative Supplies (Note 5)	-	75	-	-	75	-	dB
Analog Input								
Analog Input Range								
	Unipolar	0 to +2.5			0 to +2.5			V
	Bipolar	±2.5			±2.5			V
Input Capacitance		-	20	-	-	20	-	pF
System Calibration Specifications								
Positive Full Scale Calibration Range		VREF+0.1			VREF+0.1			V
Positive Full Scale Input Overrange		VREF+0.1			VREF+0.1			V
Negative Full Scale Input Overrange		-(VREF+0.1)			-(VREF+0.1)			V
Maximum Offset Unipolar Mode		-(VREF+0.1)			-(VREF+0.1)			V
Calibration Range (Notes 6, 7)		-40%VREF to +40%VREF			-40%VREF to +40%VREF			V
Bipolar Mode								
Input Span (Note 8)		80%VREF	2VREF +0.2		80%VREF	2VREF +0.2		V

4. All outputs unloaded.
5. 0.1Hz to 10Hz. PSRR at 60 Hz will exceed 120 dB due to the benefit of the digital filter.
6. In unipolar mode the offset can have a negative value (-VREF) such that the unipolar mode can mimic bipolar mode operation.
7. The specifications for Input Overrange and for Input Span apply additional constraints on the offset calibration range.
8. For Unipolar mode, Input Span is the difference between full scale and zero scale. For Bipolar mode, Input Span is the difference between positive and negative full scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of  $\pm(VREF + 0.1)$ .

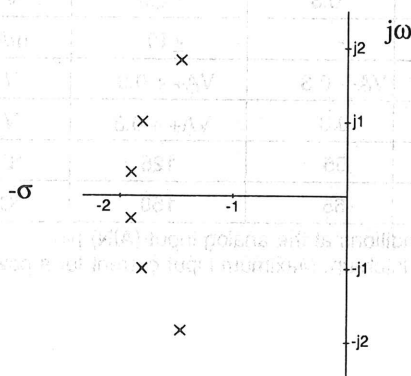
Specifications are subject to change without notice.

### DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Sampling Frequency	$f_s$	CLKIN/ 256	Hz
Output Update Rate	$f_{out}$	CLKIN /1024	Hz
Filter Corner Frequency	$f_{-3dB}$	CLKIN /409,600	Hz
Settling Time to $\pm 0.0007\%$ FS (FS Step)	$t_s$	506,880/CLKIN	s



3



$$S_{1,2} = -1.4667 \pm j1.8199$$

$$S_{3,4} = -1.7559 \pm j1.0008$$

$$S_{5,6} = -1.8746 \pm j0.32276$$

S-Domain Pole/Zero Plot (Continuous-Time Representation)

$$H(x) = [1 + 0.694x^2 + 0.241x^4 + 0.0557x^6 + 0.009664x^8 + 0.00134x^{10} + 0.000155x^{12}]^{-1/2}$$

where  $x = f/f_{-3dB}$ ,  $f_{-3dB} = \text{CLKIN}/409,600$ , and  $f$  is the frequency of interest.

Continuous-Time Representation of 6-Pole Gaussian Filter



**DIGITAL CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ;  $V_{A+}, V_{D+} = 5V \pm 10\%$ ;  $V_{A-}, V_{D-} = -5V \pm 10\%$ )

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention Power Supply Voltage ( $V_{D+}$ and $V_{A+}$ )	$V_{MR}$	2.0	-	-	V
High-Level Input Voltage All Except CLKIN	$V_{IH}$	2.0	-	-	V
High-Level Input Voltage CLKIN	$V_{IH}$	3.5	-	-	V
Low-Level Input Voltage All Except CLKIN	$V_{IL}$	-	-	0.8	V
Low-Level Input Voltage CLKIN	$V_{IL}$	-	-	1.5	V
High-Level Output Voltage (Note 9)	$V_{OH}$	$V_{D+} - 1.0V$	-	-	V
Low-Level Output Voltage $I_{out}=1.6mA$	$V_{OL}$	-	-	0.4	V
Input Leakage Current	$I_{in}$	-	-	10	$\mu A$
3-State Leakage Current	$I_{OZ}$	-	-	$\pm 10$	$\mu A$
Digital Output Pin Capacitance	$C_{out}$	-	9	-	pF

Notes: 9.  $I_{out} = -100 \mu A$ . This guarantees the ability to drive one TTL load. ( $V_{OH} = 2.4V$  @  $I_{out} = -40 \mu A$ ).

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive Digital	$V_{D+}$	-0.3	$V_{A+} + 0.3$	V
Negative Digital	$V_{D-}$	0.3	-6.0	V
Positive Analog	$V_{A+}$	-0.3	6.0	V
Negative Analog	$V_{A-}$	0.3	-6.0	V
Input Current, Any Pin Except Supplies (Notes 10, 11)	$I_{in}$	-	$\pm 10$	mA
Analog Input Voltage ( $A_{IN}$ and $V_{REF}$ pins)	$V_{INA}$	$V_{A-} - 0.3$	$V_{A+} + 0.3$	V
Digital Input Voltage	$V_{IND}$	-0.3	$V_{A+} + 0.3$	V
Ambient Operating Temperature	$T_A$	-55	125	$^{\circ}C$
Storage Temperature	$T_{stg}$	-65	150	$^{\circ}C$

Notes: 10. Applies to all pins including continuous overvoltage conditions at the analog input ( $A_{IN}$ ) pin.

11. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is  $\pm 50$  mA.

### RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 12.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	4.5	5.0	VA+	V
Negative Digital	VD-	-4.5	-5.0	-5.5	V
Positive Analog	VA+	4.5	5.0	5.5	V
Negative Analog	VA-	-4.5	-5.0	-5.5	V
Analog Reference Voltage	VREF	1.0	2.5	3.0	V
Analog Input Voltage: Unipolar (Note 13)	V <sub>AIN</sub>	AGND	-	VREF	V
Bipolar	V <sub>AIN</sub>	-VREF	-	VREF	V

Notes: 12. All voltages with respect to ground.

13. The CS5501 and CS5503 can accept input voltages up to the analog supplies (VA+ and VA-). They will accurately convert and filter signals with noise excursions up to 100mV beyond |VREF|.

After filtering, the devices will output all 1's for any input above VREF and all 0's for any input below

3

### SWITCHING CHARACTERISTICS (T<sub>A</sub> = T<sub>min</sub> to T<sub>max</sub>; CLKIN=4.096 MHz; VA+, VD+ = 5V±10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C<sub>L</sub> = 50 pF; unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency: Internal Gate Oscillator: (See Table 1)	CLKIN	200	4096	5000	kHz
Externally Supplied: (Note 14)	CLKIN	-	-	5000	kHz
Maximum	CLKIN	200	40	-	kHz
Minimum (Note 15)	CLKIN	200	40	-	kHz
CLKIN Duty Cycle	-	20	-	80	%
Rise Times: Any Digital Input	t <sub>rise</sub>	-	-	1.0	μs
Any Digital Output (Note 16)	t <sub>rise</sub>	-	20	-	ns
Fall Times: Any Digital Input	t <sub>fall</sub>	-	-	1.0	μs
Any Digital Output (Note 16)	t <sub>fall</sub>	-	20	-	ns
Set Up Times: SC1, SC2 to CAL Low (Note 17)	t <sub>scs</sub>	100	-	-	ns
SLEEP High to CLKIN High (Note 18)	t <sub>sls</sub>	1	-	-	μs
Hold Time: SC1, SC2 hold after CAL falls	t <sub>sch</sub>	100	-	-	ns

Notes: 14. CLKIN must be supplied whenever the CS5501 or CS5503 is not in SLEEP mode. If no clock is present when not in SLEEP mode, the device can draw higher current than specified and possibly become uncalibrated.

15. The CS5501/CS5503 is production tested at 4.096 MHz. It is guaranteed by characterization to operate at 200 kHz.

16. Specified using 10% and 90% points on waveform of interest.

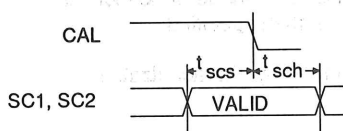
17. Silicon prior to mid 1992 latched SC0, SC2 on the rising edge of CAL. All silicon after mid 1992 will latch SC1, SC2 on the falling edge of CAL.

18. In order to synchronize several CS5501's or CS5503's together using the SLEEP pin, this specification must be met.

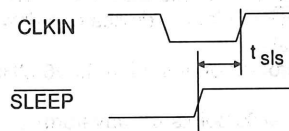
**SWITCHING CHARACTERISTICS** (continued) ( $T_A = T_{min}$  to  $T_{max}$ ;  
 $V_{A+}$ ,  $V_{D+} = 5V \pm 10\%$ ;  $V_{A-}$ ,  $V_{D-} = -5V \pm 10\%$ ; Input Levels: Logic 0 = 0V, Logic 1 =  $V_{D+}$ ;  $C_L = 50$  pF)

Parameter	Symbol	Min	Typ	Max	Units
<b>SSC Mode (Mode = <math>V_{D+}</math>)</b>					
Access Time $\overline{CS}$ Low to SDATA Out	$t_{csd1}$	3/CLKIN	-	-	ns
SDATA Delay Time SCLK Falling to New SDATA bit	$t_{dd1}$	-	25	100	ns
SCLK Delay Time SDATA MSB bit to SCLK Rising (at 4.096 MHz)	$t_{cd1}$	250	380	-	ns
Serial Clock (Out) Pulse Width High (at 4.096MHz) Pulse Width Low	$t_{ph1}$	-	240	300	ns
	$t_{pl1}$	-	730	790	ns
Output Float Delay SCLK Rising to Hi-Z	$t_{fd2}$	-	1/CLKIN + 100	1/CLKIN + 200	ns
Output Float Delay (Note 19) $\overline{CS}$ High to Output Hi-Z	$t_{fd1}$	-	-	4/CLKIN + 200	ns
<b>SEC Mode (Mode = DGND)</b>					
Serial Clock (In)	$f_{sclk}$	dc	-	4.2	MHz
Serial Clock (In) Pulse Width High Pulse Width Low	$t_{ph2}$	50	-	-	ns
	$t_{pl2}$	180	-	-	ns
Access Time $\overline{CS}$ Low to Data Valid (Note 20)	$t_{csd2}$	-	80	160	ns
Maximum Data Delay Time (Note 21) SCLK Falling to New SDATA bit	$t_{dd2}$	-	75	150	ns
Output Float Delay $\overline{CS}$ High to Output Hi-Z	$t_{fd3}$	-	-	250	ns
Output Float Delay SCLK Falling to Output Hi-Z	$t_{fd4}$	-	100	200	ns

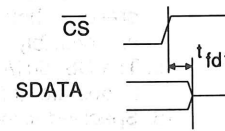
- Notes: 19. If  $\overline{CS}$  is returned high before all data bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.
20. If  $\overline{CS}$  is activated asynchronously to  $\overline{DRDY}$ ,  $\overline{CS}$  will not be recognized if it occurs when  $\overline{DRDY}$  is high for 4 clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asynchronous  $\overline{CS}$ , SCLK(i) should not be taken high sooner than 4 CLKIN cycles plus 160ns after  $\overline{CS}$  goes low.
21. SDATA transitions on the falling edge of SCLK(i).



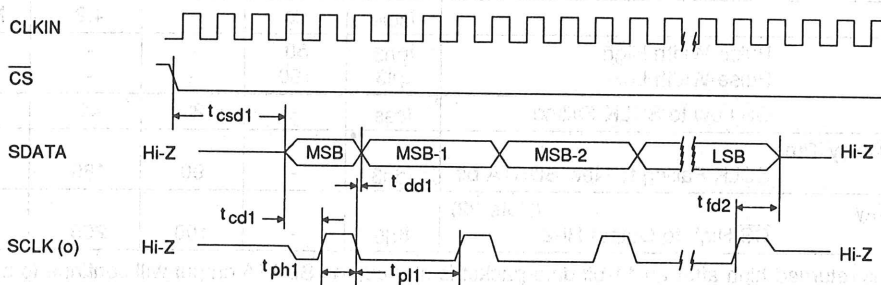
Calibration Control Timing



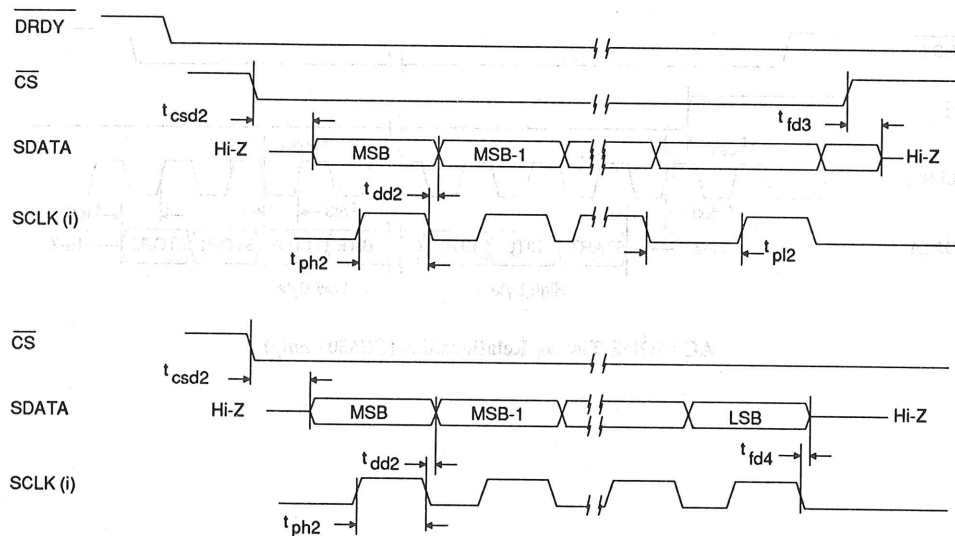
Sleep Mode Timing for Synchronization



Output Float Delay SSC Mode (Note 19)



**SSC MODE Timing Relationships**



**SEC MODE Timing Relationships**

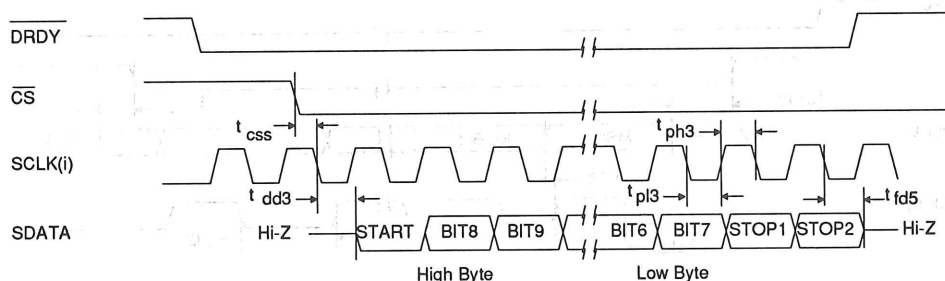
# SWITCHING CHARACTERISTICS (continued)

( $T_A = T_{min}$  to  $T_{max}$ ;

$V_{A+}, V_{D+} = 5V \pm 10\%$ ;  $V_{A-}, V_{D-} = -5V \pm 10\%$ ; Input Levels: Logic 0 = 0V, Logic 1 =  $V_{D+}$ ;  $C_L = 50$  pF)

Parameter	Symbol	Min	Typ	Max	Units
<b>AC Mode (Mode = VD-) CS5501 only</b>					
Serial Clock (In)	f <sub>sclk</sub>	dc	-	4.2	MHz
Serial Clock (In)	Pulse Width High	t <sub>ph3</sub>	50	-	ns
	Pulse Width Low	t <sub>pl3</sub>	180	-	ns
Set-up Time	$\overline{CS}$ Low to SCLK Falling	t <sub>css</sub>	-	20	ns
Maximum Data Delay Time	SCLK Falling to New SDATA bit	t <sub>dd3</sub>	90	180	ns
Output Float Delay	(Note 22) $\overline{CS}$ High to Output Hi-Z	t <sub>fd5</sub>	-	100	ns

22. If  $\overline{CS}$  is returned high after an 11-bit data packet is started, the SDATA output will continue to output data until the end of the second stop bit. At that time the SDATA output will go to high impedance.



**AC MODE Timing Relationships (CS5501 only)**

## GENERAL DESCRIPTION

The CS5501/CS5503 are monolithic CMOS A/D converters designed specifically for high resolution measurement of low-frequency signals. Each device consists of a charge-balance converter (16-Bit for the CS5501, 20-Bit for the CS5503), calibration microcontroller with on-chip SRAM, and serial communications port.

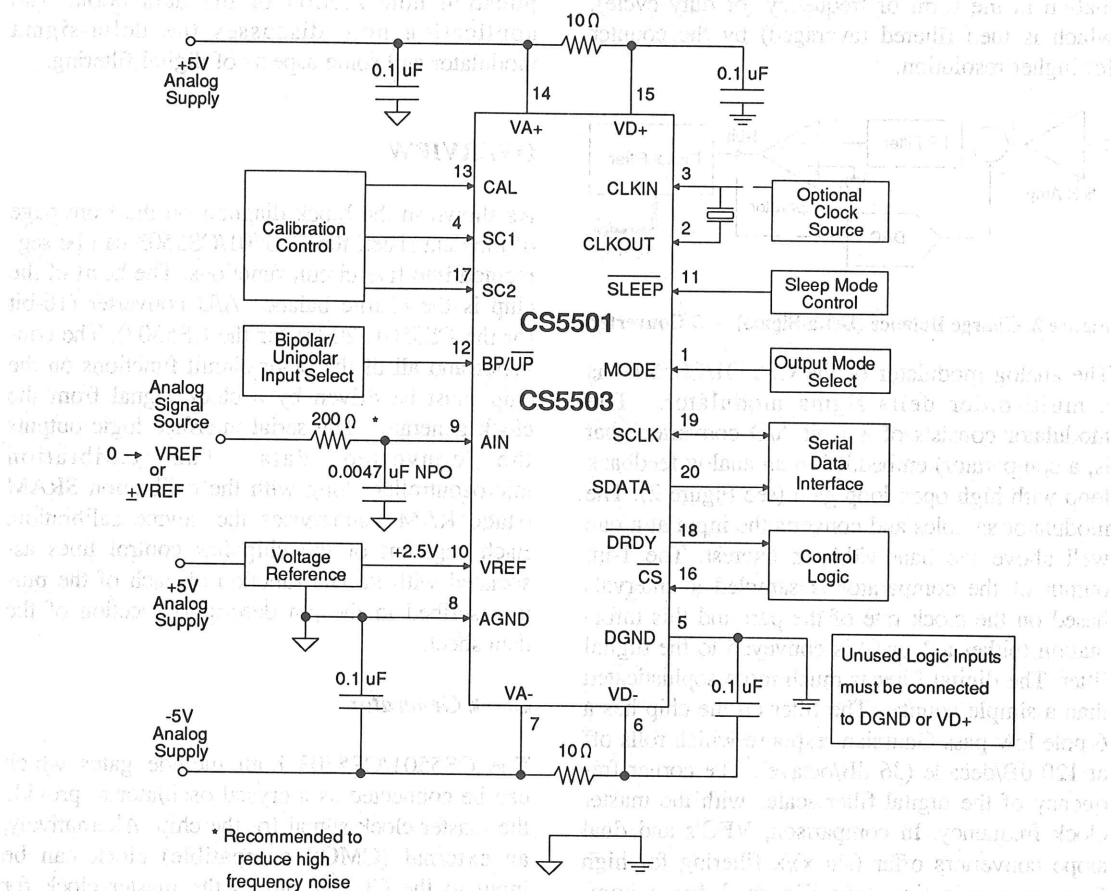
The CS5501/CS5503 A/D converters perform conversions continuously and update their output ports after every conversion (unless the serial port is active). Conversions are performed and the serial port is updated independent of external con-

trol. Both devices are capable of measuring either unipolar or bipolar input signals, and calibration cycles may be initiated at any time to ensure measurement accuracy.

The CS5501/CS5503 perform conversions at a rate determined by the master clock signal. The master clock can be set by an external clock or with a crystal connected to the pins of the on-chip gate oscillator. The master clock frequency determines:

1. The sample rate of the analog input signal.
2. The corner frequency of the on-chip digital filter.
3. The output update rate of the serial output port.

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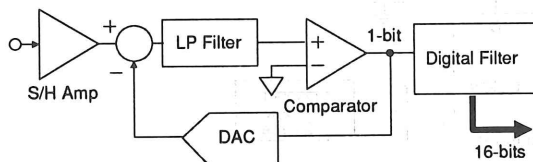


**Figure 1. Typical Connection Diagram**

The CS5501/CS5503 design includes several self-calibration modes and several serial port interface modes to offer users maximum system design flexibility.

### **The Delta-Sigma Conversion Method**

The CS5501/CS5503 A/D converters use charge-balance techniques to achieve low cost, high resolution measurements. A charge-balance A/D converter consists of two basic blocks: an analog modulator and a digital filter. An elementary example of a charge-balance A/D converter is a conventional voltage-to-frequency converter and counter. The VFC's 1-bit output conveys information in the form of frequency (or duty cycle), which is then filtered (averaged) by the counter for higher resolution.



**Figure 2. Charge Balance (Delta-Sigma) A/D Converter**

The analog modulator of the CS5501/CS5503 is a multi-order delta-sigma modulator. The modulator consists of a 1-bit A/D converter (that is, a comparator) embedded in an analog feedback loop with high open loop gain (see Figure 2). The modulator samples and converts the input at a rate well above the bandwidth of interest. The 1-bit output of the comparator is sampled at intervals based on the clock rate of the part and this information (either a 1 or 0) is conveyed to the digital filter. The digital filter is much more sophisticated than a simple counter. The filter on the chip has a 6-pole low pass Gaussian response which rolls off at 120 dB/decade (36 dB/octave). The corner frequency of the digital filter scales with the master clock frequency. In comparison, VFC's and dual slope converters offer  $(\sin x)/x$  filtering for high frequency rejection (see Figure 3 for a comparison of the characteristics of these two filter

types). When operating from a 1 MHz master clock the digital filter in the CS5501/CS5503 offers better than 120 dB rejection of 50 and 60 Hz line frequencies and does not require any type of line synchronization to achieve this rejection. It should be noted that the CS5501/CS5503 will update its output port almost at 1000 times per second when operating from the 1 MHz clock. This is a much higher update rate (typically by a factor of at least 50 times) than either VFCs or dual-slope converters can offer.

For a more detailed discussion on the delta-sigma modulator see the Application note "Delta-Sigma A/D Conversion Technique Overview" in the application note section of the data book. The application note discusses the delta-sigma modulator and some aspects of digital filtering.

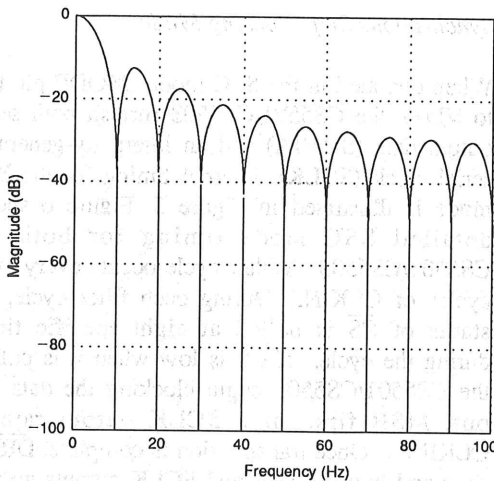
### **OVERVIEW**

As shown in the block diagram on the front page of the data sheet, the CS5501/CS5503 can be segmented into five circuit functions. The heart of the chip is the charge balance A/D converter (16-bit for the CS5501, 20-bit for the CS5503). The converter and all of the other circuit functions on the chip must be driven by a clock signal from the clock generator. The serial interface logic outputs the converted data. The calibration microcontroller along with the calibration SRAM (static RAM), supervises the device calibration. Each segment of the chip has control lines associated with it. The function of each of the pins is described in the pin description section of the data sheet.

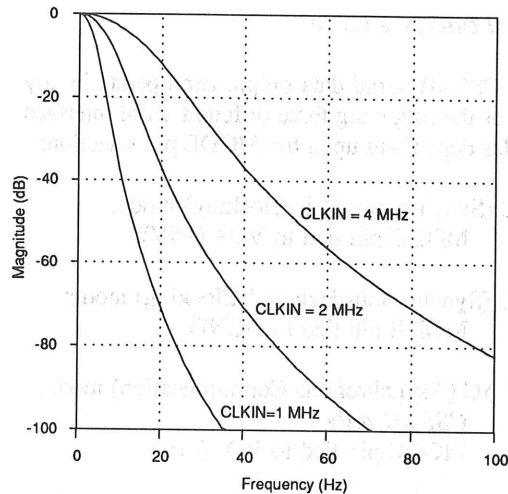
### **Clock Generator**

The CS5501/CS5503 both include gates which can be connected as a crystal oscillator to provide the master clock signal for the chip. Alternatively, an external (CMOS compatible) clock can be input to the CLKIN pin as the master clock for the device. Figure 4 illustrates a simple model of





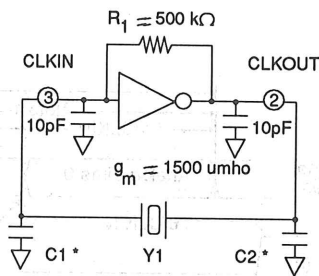
a. Averaging (Integrating) Filter Response (tavg = 100 ms)



b. 6-Pole Gaussian Filter Response

Figure 3. Filter Responses

the on-chip gate oscillator. The gate has a typical transconductance of 1500  $\mu\text{mho}$ . The gate model includes 10 pF capacitors at the input and output pins. These capacitances include the typical stray capacitance of the pins of the device. The on-chip gate oscillator is designed to properly operate without additional loading capacitors when using a 4.096 MHz (or 4 MHz) crystal. If other crystal frequencies or if ceramic resonators are used, loading capacitors may be necessary for reliable operation of the oscillator. Table 1 illustrates some typical capacitor values to be used with selected resonating elements.



\* See Table 1

Figure 4. On-chip Gate Oscillator Model

CLKOUT (pin 2) can be used to drive one external CMOS gate for system clock requirements. In this case, the external gate capacitance must be taken into account when choosing the value of C2.

**Caution:** A clock signal should always be present whenever the SLEEP is inactive (SLEEP = VD+). If no clock is provided to the part when not in SLEEP, the part may draw excess current and possibly even lose its calibration data. This is because the device is built using dynamic logic.

Resonators	C1	C2
Ceramic		
200 kHz	330pF	470pF
455 kHz	100pF	100pF
1.0 MHz	50pF	50pF
2.0 MHz	20pF	20pF
Crystals		
2.000 MHz	30pF	30pF
3.579 MHz	20pF	20pF
4.096 MHz	None	None

Table 1. Resonator Loading Capacitors

### Serial Interface Logic

The CS5501 serial data output can operate in any one of the following three different serial interface modes depending upon the MODE pin selection:

SSC (Synchronous Self-Clocking) mode;  
MODE pin tied to VD+ (+5V).

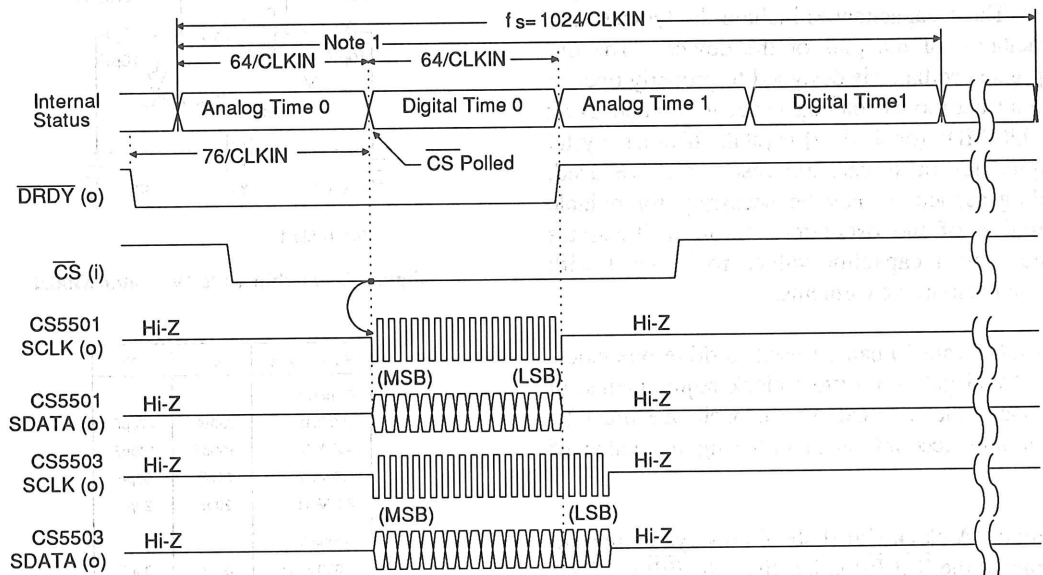
SEC (Synchronous External Clocking) mode;  
MODE pin tied to DGND.

and AC (Asynchronous Communication) mode;  
**CS5501 only**  
MODE pin tied to VD- (-5V)

The CS5503 can only operate in the first two modes, SEC and SSC.

### Synchronous Self-Clocking Mode

When operated in the SSC mode (MODE pin tied to VD+), the CS5501/CS5503 furnish both serial output data (SDATA) and an internally-generated serial clock (SCLK). Internal timing for the SSC mode is illustrated in Figure 5. Figure 6 shows detailed SSC mode timing for both the CS5501/CS5503. A filter cycle occurs every 1024 cycles of CLKIN. During each filter cycle, the status of  $\overline{CS}$  is polled at eight specific times during the cycle. If  $\overline{CS}$  is low when it is polled, the CS5501/CS5503 begin clocking the data bits out, MSB first, at a SCLK output rate of CLKIN/4. Once transmission is complete,  $\overline{DRDY}$  rises and both SDATA and SCLK outputs go into a high impedance state. A filter cycle begins each time  $\overline{DRDY}$  falls. If the  $\overline{CS}$  line is not active,  $\overline{DRDY}$  will return high 1020 clock cycles after it falls. Four clock cycles later  $\overline{DRDY}$  will fall to signal that the serial port has been updated with new data and that a new filter cycle has begun.



Note: There are 16 analog and digital settling periods per filter cycle (4 are shown). Data can be output in the SSC mode in only 1 of the 8 digital time periods in each filter cycle.

**Figure 5. Internal Timing**

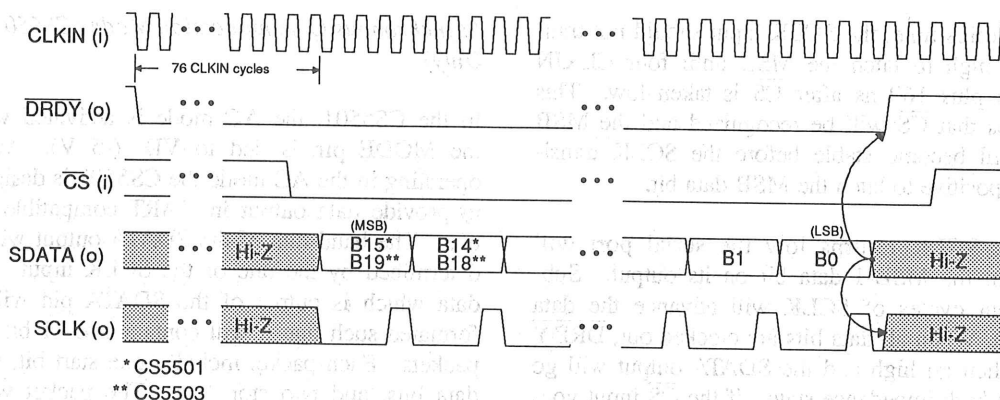


Figure 6. Synchronous Self-Clocking (SSC) Mode Timing

The first  $\overline{CS}$  polling during a filter cycle occurs 76 clock cycles after  $\overline{DRDY}$  falls (the rising edge of CLKIN on which  $\overline{DRDY}$  falls is considered clock cycle number one). Subsequent pollings of  $\overline{CS}$  occur at intervals of 128 clock cycles thereafter (76, 204, 332, etc.). The  $\overline{CS}$  signal is polled at the beginning of each of eight data output windows which occur in a filter cycle. To transmit data during any one of the eight output windows,  $\overline{CS}$  must be low at least three CLKIN cycles before it is polled. If  $\overline{CS}$  does not meet this set-up time, data will not be transmitted during the window time. Furthermore,  $\overline{CS}$  is not latched internally and therefore must be held low during the entire data transmission to obtain all of the data bits.

The eighth output window time overlaps the time in which the serial output port is to be updated. If the  $\overline{CS}$  is recognized as being low when it is polled for the eighth window time, data will be output as normal, but the serial port will not be updated with new data until the next serial port update time. Under these conditions, the serial port will experience an update rate of only 2 kHz (CLKIN = 4.096 MHz) instead of the normal 4 kHz serial port update rate.

Upon completion of transmission of all the data bits, the SCLK and SDATA outputs will go to a high impedance state even with  $\overline{CS}$  held low. In

the event that  $\overline{CS}$  is taken high before all data bits are output, the SDATA and SCLK outputs will complete the current data bit output and go to a high impedance state when SCLK goes low.

#### Synchronous External Clocking Mode

When operated in the SEC mode (MODE pin tied to DGND), the CS5501/CS5503 outputs the data in its serial port at a rate determined by an external clock which is input into the SCLK pin. In this mode the output port will be updated every 1024 CLKIN cycles.  $\overline{DRDY}$  will go low when new data is loaded into the output port. If  $\overline{CS}$  is not active,  $\overline{DRDY}$  will return positive 1020 CLKIN cycles later and remain so for four CLKIN cycles. If  $\overline{CS}$  is taken low it will be recognized immediately unless it occurs while  $\overline{DRDY}$  is high for the four clock cycles. As soon as  $\overline{CS}$  is recognized, the SDATA output will come out of its high-impedance state and present the MSB data bit. The MSB data bit will remain present until a falling edge of SCLK occurs to advance the output to the MSB-1 bit. If the  $\overline{CS}$  and external SCLK are operated asynchronously to CLKIN, errors can result in the output data unless certain precautions are taken. If  $\overline{CS}$  is activated asynchronously, it may occur during the four clock cycles when  $\overline{DRDY}$  is high and therefore not be recognized immediately. To be certain that data misread errors will not result if  $\overline{CS}$  oc-

curs at this time, the SCLK input should not transition high to latch the MSB until four CLKIN cycles plus 160 ns after  $\overline{CS}$  is taken low. This insures that  $\overline{CS}$  will be recognized and the MSB bit will become stable before the SCLK transitions positive to latch the MSB data bit.

When SCLK returns low the serial port will present the MSB-1 data bit on its output. Subsequent cycles of SCLK will advance the data output. When all data bits are clocked out,  $\overline{DRDY}$  will then go high and the SDATA output will go into a high impedance state. If the  $\overline{CS}$  input goes low and all of the data bits are not clocked out of the port, filter cycles will continue to occur but the output serial port will not be updated with new data ( $\overline{DRDY}$  will remain low). If  $\overline{CS}$  is taken high at any time, the SDATA output pin will go to a high impedance state. If any of the data bits in the serial port have not been clocked out, they will remain available until  $\overline{DRDY}$  returns high for four clock cycles. After this  $\overline{DRDY}$  will fall and the port will be updated with a new 16-bit word in the CS5501 or 20-bit word in the CS5503. It is acceptable to clock out less than all possible data bits if  $\overline{CS}$  is returned high to allow the port to be updated. Figure 7 illustrates the serial port timing in the SEC mode.

#### Asynchronous Communication Mode (CS5501 Only)

In the CS5501, the AC mode is activated when the MODE pin is tied to VD- (-5 V). When operating in the AC mode the CS5501 is designed to provide data output in UART compatible format. The baud rate of the SDATA output will be determined by the rate of the SCLK input. The data which is output of the SDATA pin will be formatted such that it will contain two 11 bit data packets. Each packet includes one start bit, eight data bits, and two stop bits. The packet which carries the most-significant-byte data will be output first, with its lsb being the first data bit output after the start bit.

In this mode,  $\overline{DRDY}$  will occur every 1024 clock cycles. If the serial port is not outputting a data byte,  $\overline{DRDY}$  will return high after 1020 clock cycles and remain high for 4 clock cycles.  $\overline{DRDY}$  will then go low to indicate that an update to the serial output port with a new 16 bit word has occurred. To initiate a transmission from the port the  $\overline{CS}$  line must be taken low. Then SCLK, which is an input in this mode, must transition from a high to a low to latch the state of  $\overline{CS}$  internal to the CS5501. Once  $\overline{CS}$  is recognized and latched as a low, the port will begin to output data. Figure 8 details the timing for this output.  $\overline{CS}$  can be returned high before the end of the 11-bit transmission and the transmission will continue until the second stop bit of the first 11-bit packet is

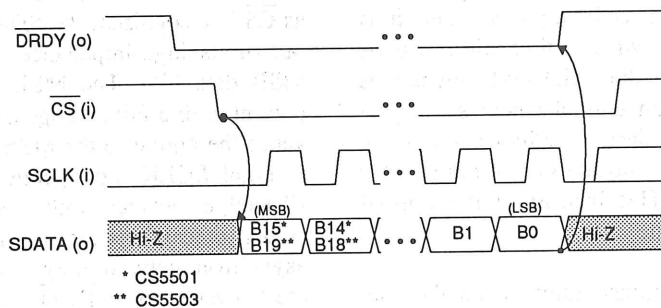


Figure 7. Synchronous External-Clocking (SEC) Mode Timing

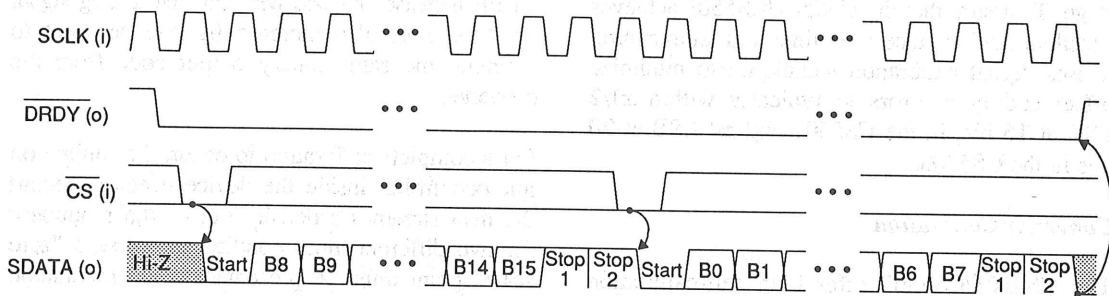


Figure 8. CS5501 Asynchronous (UART) Mode Timing

output. The SDATA output will go into a high impedance state after the second stop bit is output. To obtain the second 11-bit packet  $\overline{CS}$  must again be brought low before  $\overline{DRDY}$  goes high or the second 11-bit data packet will be overwritten with a serial port update. For the second 11-bit packet,  $\overline{CS}$  need only to go low for 50 ns; it need not be latched by a falling edge of SCLK. Alternately, the  $\overline{CS}$  line can be taken low and held low until both 11-bit data packets are output. This is the preferred method of control as it will prevent losing the second 11-bit data packet if the port is updated. Some serial data rates can be quite slow compared to the rate at which the CS5501 can update its output port. A slow data rate will leave only a short period of time to start the second 11-bit packet if  $\overline{CS}$  is returned high momentarily. If  $\overline{CS}$  is held low continuously ( $\overline{CS}$  hard-wired to DGND), the serial port will be updated only after all 22 bits have been clocked out of the port.

Upon the completion of a transmission of the two 11-bit data packets the SDATA output will go into a high impedance state. If at any time during transmission the  $\overline{CS}$  is taken back high, the current 11-bit data packet will continue to be output. At the end of the second stop bit of the data packet, the SDATA output will go into a high impedance state.

### Linearity Performance

The CS5501/CS5503 delta-sigma converters are like conventional charge-balance converters in that they have no source of nonmonotonicity. The devices therefore have no missing codes in their transfer functions. See Figure 9 for a plot of the excellent differential linearity achieved by the CS5501. The CS5501/CS5503 also have excellent integral linearity, which is accomplished with a well-designed charge-balance architecture. Each device also achieves low input drift through the use of chopper-stabilized techniques in its input

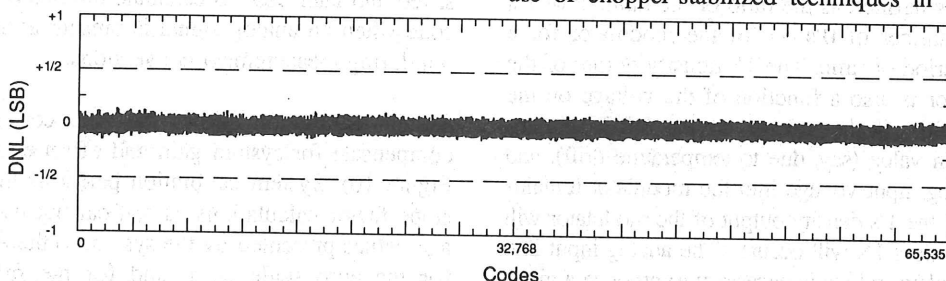


Figure 9. CS5501 Differential Nonlinearity Plot

stage. To assure that the CS5501/CS5503 achieves excellent performance over time and temperature, it uses digital calibration techniques to minimize offset and gain errors to typically within  $\pm 1/2$  LSB at 16 bits in the CS5501 and  $\pm 4$  LSB at 20 bits in the CS5503.

### **Converter Calibration**

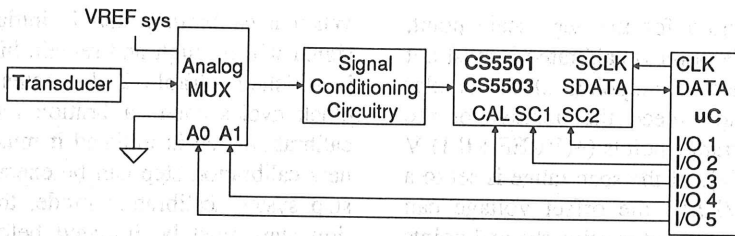
The CS5501/CS5503 offer both self-calibration and system level calibration capability. To understand the calibration features, a basic comprehension of the internal workings of the converter are helpful. As mentioned previously in this data sheet, the converter consists of two sections. First is the analog modulator which is a delta-sigma type charge-balance converter. This is followed by a digital filter. The filter circuitry is actually an arithmetic logic unit (ALU) whose architecture and instructions execute the filter function. The modulator (explained in more detail in the applications note "Delta-Sigma Conversion Technique Overview") uses the VREF voltage connected to pin 10 to determine the magnitude of the voltages used in its feedback DAC. The modulator accepts an analog signal at its input and produces a data stream of 1's and 0's as its output. This data stream value can change (from 1 to 0 or vice versa) every 256 CLKIN cycles. As the input voltage increases the ratio of 1's to 0's out of the modulator increases proportionally. The 1's density of the data stream out of the modulator therefore provides a digital representation of the analog input signal where the 1's density is defined as the ratio of the number of 1's to the number of 0's out of the modulator for a given period of time. The 1's density output of the modulator is also a function of the voltage on the VREF pin. If the voltage on the VREF pin increases in value (say, due to temperature drift), and the analog input voltage into the modulator remains constant, the 1's density output of the modulator will decrease (less 1's will occur). The analog input into the modulator which is necessary to produce a given binary output code from the converter is ratiometric to the voltage on the VREF pin. This means that if

VREF increases by one per cent, the analog signal on AIN must also increase by one per cent to maintain the same binary output code from the converter.

For a complete calibration to occur, the calibration microcontroller inside the device needs to record the data stream 1's density out of the modulator for two different input conditions. First, a "zero scale" point must be presented to the modulator. Then a "full scale" point must be presented to the modulator. In unipolar self-cal mode the zero scale point is AGND and the full scale point is the voltage on the VREF pin. The calibration microcontroller then remembers the 1's density out of the modulator for each of these points and calculates a slope factor (LSB/uV). This slope factor represents the gain slope for the input to output transfer function of the converter. In unipolar mode the calibration microcontroller determines the slope factor by dividing the span between the zero point and the full scale point by the total resolution of the converter ( $2^{16}$  for the CS5501, resulting in 65,536 segments or  $2^{20}$  for the CS5503, resulting in 1,048,578 segments). In bipolar mode the calibration microcontroller divides the span between the zero point and the full scale point into 524,288 segments for the CS5503 and 32,768 segments for the CS5501. It then extends the measurement range 524,288 segments for the CS5503, 32,768 segments for the CS5501, below the zero scale point to achieve bipolar measurement capability. In either unipolar or bipolar modes the calculated slope factor is saved and later used to calculate the binary output code when an analog signal is present at the AIN pin during measurement conversions.

System calibration allows the A/D converter to compensate for system gain and offset errors (see Figure 10). System calibration performs the same slope factor calculations as self-cal but uses voltage values presented by the system to the AIN pin for the zero scale point and for the full scale point. Table 2 depicts the calibration modes available. Two system calibration modes are





**Figure 10. System Calibration**

CAL	SC1	SC2	Cal Type	ZS Cal	FS Cal	Sequence	Calibration Time
↓	0	0	Self-Cal	AGND	VREF	One Step	3,145,655/fclk
↓	1	1	System Offset & System Gain	AIN	-	1st Step	1,052,599/fclk
↓	0	1		-	AIN	2nd Step	1,068,813/fclk
↓	1	0	System Offset	AIN	VREF	One Step	2,117,389/fclk

\* DRDY remains high throughout the calibration sequence. In Self-Cal mode (SC1 and SC2 low) DRDY falls once the CS5501 or CS5503 has settled to the analog input. In all other modes DRDY falls immediately after the calibration term has been determined.

**Table 2. Calibration Control**

listed. The first mode offers system level calibration for system offset and for system gain. This is a two-step calibration. The zero scale point (system offset) must be presented to the converter first. The voltage that represents zero scale point must be input to the converter before the calibration step is initiated and must remain stable until the step is complete. The DRDY output from the converter will signal when the step is complete by going low. After the zero scale point is calibrated, the voltage representing the full scale point is input to the converter and the second calibration step is initiated. Again the voltage must remain stable throughout the calibration step.

This two-step calibration mode offers another calibration feature. After a two-step calibration sequence (system offset and system gain) has been properly performed, additional offset calibrations can be performed by themselves to reposition the gain slope (the slope factor is not changed) to adjust its zero reference point to the new system zero reference value.

A second system calibration mode is available which uses an input voltage for the zero scale

calibration point, but uses the VREF voltage as the full scale calibration point.

Whenever a system calibration mode is used, there are limits to the amount of offset and to the amount of span which can be accommodated. The range of input span which can be accommodated in either unipolar or bipolar mode is restricted to not less than 80% of the voltage on VREF and not more than 200% of (VREF + 0.1) V. The amount of offset which can be calibrated depends upon whether unipolar or bipolar mode is being used. In unipolar mode the system calibration modes can handle offsets as positive as 20% of VREF (this is restricted by the minimum span requirement of 80% VREF) or as negative as -(VREF + 0.1) V. This capability enables the unipolar mode of the CS5501/CS5503 to be calibrated to mimic bipolar mode operation.

In the bipolar mode the system offset calibration range is restricted to a maximum of  $\pm 40\%$  of VREF. It should be noted that the span restrictions limit the amount of offset which can be calibrated. The span range of the converter in bipolar mode extends an equidistance (+ and -)



from the voltage used for the zero scale point. When the zero scale point is calibrated it must not cause either of the two endpoints of the bipolar transfer function to exceed the positive or the negative input overrange points  $(+(VREF + 0.1) V$  or  $-(VREF + 0.1) V$ ). If the span range is set to a minimum (80% VREF) the offset voltage can move  $\pm 40\%$  VREF without causing the end points of the transfer function to exceed the overrange points. Alternatively, if the span range is set to 200% of VREF, the input offset cannot move more than  $+0.1$  or  $-0.1 V$  before an endpoint of the transfer function exceeds the input overrange limit.

### Initiating Calibration

Table 2 illustrates the calibration modes available in the CS5501/CS5503. Not shown in the table is the function of the BP/UP pin which determines whether the converter is calibrated to measure bipolar or unipolar signals. A calibration step is initiated by bringing the CAL pin (13) high for at least 4 CLKIN cycles to reset the part and then bringing CAL low. The states of SC1 (pin 4) and SC2 (pin 17) along with the BP/UP (pin 12) will determine the type of calibration to be performed. The SC1 and SC2 inputs are latched when CAL goes low. The BP/UP input is not latched and therefore must remain in a fixed state throughout the calibration and measurement cycles. Any time the state of the BP/UP pin is changed, a new calibration cycle must be performed to enable the CS5501/CS5503 to properly function in the new mode.

$$DOUT = \text{Slope} (AIN - \text{Unipolar Offset}) + 0.5 \text{ LSB}$$

a. Unipolar Calibration

When a calibration step is initiated, the  $\overline{DRDY}$  signal will go high and remain high until the step is finished. Table 2 illustrates the number of clock cycles each calibration requires. Once a calibration step is initiated it must finish before a new calibration step can be executed. In the two step system calibration mode, the offset calibration step must be initiated before initiating the gain calibration step.

When a self-cal is completed  $\overline{DRDY}$  falls and the output port is updated with a data word that represents the analog input signal at the AIN pin. When a system calibration step is completed,  $\overline{DRDY}$  will fall and the output port will be updated with the appropriate data value (zero scale point, or full scale point). In the system calibration mode, the digital filter must settle before the output code will represent the value of the analog input signal.

Tables 3 and 4 indicate the output code size and output coding of the CS5501/CS5503 in its various modes. The calibration equations which represent the CS5501/CS5503 transfer function are shown in Figure 11.

### Underrange And Overage Considerations

The input signal range of the CS5501/CS5503 will be determined by the mode in which the part is calibrated. Table 4 indicates the input signal range in the various modes of operation. If the input signal exceeds the full scale point the converter will output all ones. If the signal is less than the zero scale point (in unipolar) or more

CS5501

$$DOUT = \text{Slope} (AIN - \text{Bipolar Offset}) + 2^{15} + 0.5 \text{ LSB}_{16}$$

CS5503

$$DOUT = \text{Slope}(AIN - \text{Bipolar Offset}) + 2^{19} + 0.5 \text{ LSB}_{20}$$

b. Bipolar Calibration

**Figure 11. Calibration Equations**

Cal Mode	Zero Scale	Gain Factor	1LSB			
			Unipolar		Bipolar	
			CS5501	CS5503	CS5501	CS5503
Self-Cal	AGND	VREF	$\frac{VREF}{65,536}$	$\frac{VREF}{1,048,526}$	$\frac{2VREF}{65,536}$	$\frac{2VREF}{1,048,526}$
System Cal	SOFF	SGAIN	$\frac{SGAIN - SOFF}{65,536}$	$\frac{SGAIN - SOFF}{1,048,526}$	$\frac{2(SGAIN - SOFF)}{65,536}$	$\frac{2(SGAIN - SOFF)}{1,048,526}$

Table 3. Output Code Size After Calibration

Input Voltage, Unipolar Mode				Input Voltage, Bipolar Mode	
System-Cal	Self-Cal	Output Codes (Hex)		Self-Cal	System Cal
		CS5501	CS5503		
$>(SGAIN - 1.5 \text{ LSB})$	$>(VREF - 1.5 \text{ LSB})$	FFFF	FFFF	$>(VREF - 1.5 \text{ LSB})$	$>(SGAIN - 1.5 \text{ LSB})$
SGAIN - 1.5 LSB	VREF - 1.5 LSB	FFFF FFFE	FFFF FFFE	VREF - 1.5 LSB	SGAIN - 1.5 LSB
$(SGAIN - SOFF)/2 - 0.5 \text{ LSB}$	$VREF/2 - 0.5 \text{ LSB}$	$\frac{8000}{7FFF}$	$\frac{80000}{7FFFF}$	AGND - 0.5 LSB	SOFF - 0.5 LSB
SOFF + 0.5 LSB	AGND + 0.5 LSB	$\frac{0001}{0000}$	$\frac{00001}{00000}$	-VREF + 0.5 LSB	-SGAIN + 2SOFF + 0.5 LSB
$<(\text{SOFF} + 0.5 \text{ LSB})$	$<(\text{AGND} + 0.5 \text{ LSB})$	0000	00000	$<(-VREF + 0.5 \text{ LSB})$	$<(-SGAIN + 2SOFF + 0.5 \text{ LSB})$

Table 4. Output Coding

negative in magnitude than minus the full scale point (in bipolar) it will output all zeroes.

Note that the modulator-filter combination in the chip CS5501/CS5503 is designed to accurately convert and filter input signals with noise excursions which extend up to 100 mV below the analog value which produces all zeros out or above the analog value which produces all ones out. Overrange noise excursions greater than 100 mV may increase output noise.

All pins of the CS5501/CS5503 include diodes which clamp the input signals to within the positive and negative supplies. If a signal on any pin (including AIN) exceeds the supply voltage (either + or -) a clamp diode will be forward-biased. Under these fault conditions the CS5501/CS5503 might be damaged. Under normal operating con-

ditions (with the power supplies established), the device will survive transient currents through the clamp diodes up to 100 mA and continuous currents up to 10 mA. The drive current into the AIN pin should be limited to a safe value if an overvoltage condition is likely to occur. See the application note "Buffer Amplifiers for the CS501X Series of A/D Converters" for further discussion on the clamp diode input structure and on current limiting circuits.

### System Synchronization

If more than one CS5501/CS5503 is included in a system which is operating from a common clock, all of the devices can be synchronized to sample and output at exactly the same time. This can be accomplished in either of two ways. First, a single CAL signal can be issued to all the

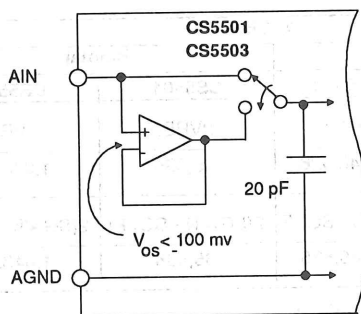


Figure 12. Analog Input Model

CS5501/CS5503's in the system. To insure synchronization on the same clock signal the CAL signal should go low on the falling edge of CLKIN. Or second, a common SLEEP control signal can be issued. If the SLEEP signal goes positive with the appropriate set up time to CLKIN, all parts will be synchronized on the same clock cycle.

### Analog Input Impedance Considerations

The analog input of the CS5501/CS5503 can be modeled as illustrated in Figure 12. A 20 pF capacitor is used to dynamically sample the input signal. Every 64 CLKIN cycles the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge ( a dynamic demand of current) will be required from the input source to settle the voltage on the sample capacitor to its final value. The voltage at the output of the buffer may differ up to 100 mV from the actual input voltage due to the offset voltage of the buffer. Timing allows 64 cycles of master clock (CLKIN) for the voltage on the sample capacitor to settle to its final value. The equation which defines settling time is:

$$V_o = V_{in} [1 - e^{-t/RC}]$$

Where  $V_o$  is the final settled value,  $V_{in}$  is the value of the input signal,  $R$  is the value of the

input source resistance,  $C$  is the 20 pF sample capacitor plus the value of any stray or additional capacitance at the input pin. The value of  $t$  is equal to  $64/CLKIN$ .

From this basic equation the following equation can be developed which indicates the maximum acceptable source resistance ( $R_{sMAX}$ ) for an error of  $V_e$ :

$$R_{smax} = \frac{64}{CLKIN(20pF + C_{str}) \ln \left[ \frac{100 \text{ mV}}{V_e} \right]}$$

This equation assumes that the offset voltage of the buffer is 100 mV, which is the worst case. The value of  $V_e$  is the maximum error voltage which is acceptable.

For a maximum error voltage ( $V_e$ ) of 10  $\mu$ V in the CS5501 (1/4LSB at 16-bits) and 600 nV in the CS5503 (1/4LSB at 20-bits), the above equation indicates that when operating from a 4.096 MHz CLKIN, source resistances up to 75 k $\Omega$  in the CS5501 or 60 k $\Omega$  in the CS5503 are acceptable in the absence of stray capacitance ( $C_{str} = 0$ ). If higher input source resistances are desired the master clock rate can be reduced to yield a longer settling time for the 64 cycle period.

An RC filter may be added in front of the CS5503 to reduce high frequency noise (see Figure 1). With an external capacitor added (from AIN to AGND) the following equation will specify the maximum allowable source resistance:

$$R_{smax} = \frac{64}{CLKIN(20pF + C_{ext}) \ln \left[ \frac{20pF(100 \text{ mV})}{(20pF + C_{ext}) V_e} \right]}$$

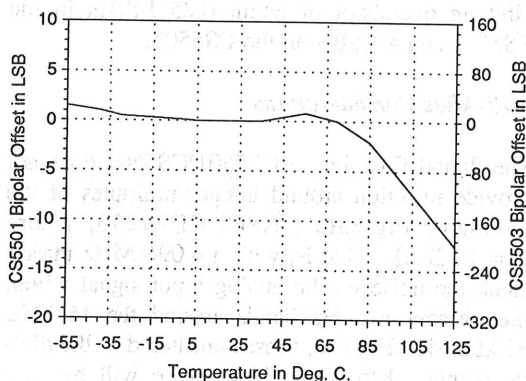


Figure 13. Typical Self-Cal Bipolar Offset vs. Temperature After Calibration at 25 °C

## Analog Input Drift Considerations

The CS5501/CS5503 analog input uses chopper-stabilization techniques to minimize input offset drift. Charge injection in the analog switches and leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. Figure 13 indicates the typical offset drift due to temperature changes experienced after calibration at 25 °C. Drift is relatively flat up to about 75 °C. Above 75 °C leakage current becomes the dominant source of offset drift. Leakage currents approximately double with each 10 °C of temperature increase. Therefore the offset drift due to leakage current increases as the temperature increases. The value of the voltage on the sample capacitor is updated at a rate determined by the master clock, therefore the amount of offset drift which occurs will be proportional to the elapsed time between samples. In conclusion, the offset drift increases with temperature and is inversely proportional to the CLKIN rate. To minimize offset drift with increased temperature, higher CLKIN rates are desirable. At temperatures above 100 °C, a CLKIN rate above 1 MHz is recommended. The effects of offset drift due to temperature changes can be eliminated by recalibrating the CS5501/CS5503 whenever the temperature has changed.

Gain drift within the converter depends predominately upon the temperature tracking of internal capacitors. Gain drift is not affected by leakage currents, therefore gain drift is significantly less than comparable offset errors due to temperature increases. The typical gain drift over the specified temperature range is less than 2.5 LSBs for the CS5501 and less than 40 LSBs for the CS5503.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. The CS5501/CS5503 can be recalibrated at any temperature to remove the effects of these errors.

Linearity and differential non linearity are not significantly affected by temperature changes.

## Filtering

At the system level, the digital filter in the CS5501/CS5503 can be modeled exactly like an analog filter with a few minor differences. Digital filtering resides *behind* the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself). Analog filtering cannot.

Also, since digital filtering resides behind the A/D converter, noise riding unfiltered on a near-full-scale input could potentially over-range the ADC. In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS5501/CS5503 each contain an analog modulator and digital filter which reserve headroom such that the device can process signals with 100mV "excursions" above full-scale and still output accurately converted and filtered data. Filtered input signals above full-scale still result in an output of all ones.

The digital filter's corner frequency occurs at  $CLKIN/409,600$ , where  $CLKIN$  is the master clock frequency. With a 4.096MHz clock, the filter corner is at 10Hz and the output register is updated at a 4kHz rate.  $CLKIN$  frequency can be reduced with a proportional reduction in the filter corner frequency and in the update rate to the output register. A plot of the filter response is shown in the specification tables section of this data sheet.

Both the CS5501/CS5503 employ internal digital filtering which creates a 6-pole Gaussian relationship. With the corner frequency set at 10Hz for minimized settling time, the CS5501/CS5503 offer approximately 55dB rejection at 60Hz to signals coming into either the AIN or VREF pins. With a 5Hz cut-off, 60Hz rejection increases to more than 90dB.

The digital filter (rather than the analog modulator) dominates the converters' settling for step-function inputs. Figure 14 illustrates the settling characteristics of the filter. The vertical axis is normalized to the input step size. The horizontal axis is in filter cycles. With a full scale input step (2.5 V in unipolar mode) the output will ex-

hibit an overshoot of about 0.25 LSB<sub>16</sub> in the CS5501 and 4 LSB<sub>20</sub> in the CS5503.

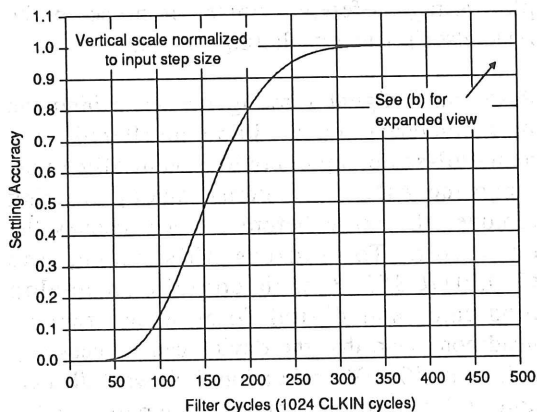
### Anti-Alias Considerations

The digital filter in the CS5501/CS5503 does not provide rejection around integer multiples of the oversampling rate  $[(N*CLKIN)/256]$ , where  $N = 1, 2, 3, \dots$ . That is, with a 4.096 MHz master clock the noise on the analog input signal within the narrow  $\pm 10$  Hz bands around the 16 kHz, 32 kHz, 48 kHz, etc., passes unfiltered to the digital output. Most broadband noise will be very well filtered because the CS5501/CS5503 use a very high oversampling ratio of 800 (16 kHz:  $2 \times 10$  Hz). Broadband noise is reduced by:

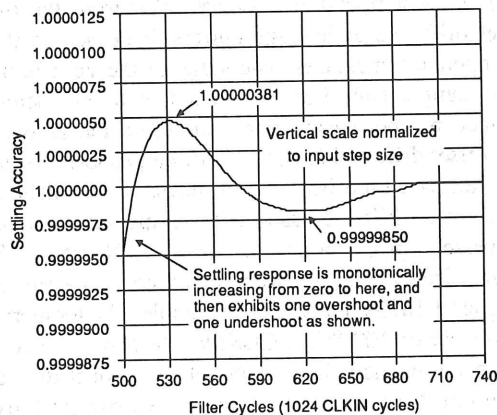
$$e_{out} = e_{in} \sqrt{2f_{-3dB}/f_s}$$

$$e_{out} = 0.035 e_{in}$$

where  $e_{in}$  and  $e_{out}$  are rms noise terms referred to the input. Since  $f_{-3dB}$  equals  $CLKIN/409,600$  and  $f_s$  equals  $CLKIN/256$ , the digital filter reduces white, broadband noise by 96.5% independent of the  $CLKIN$  frequency. For example, a typical operational amplifier's 50 $\mu$ V rms noise would be reduced to 1.75 $\mu$ V rms (0.035 LSB's rms at the 16-bit level in the CS5501 and 0.4 LSB's rms at the 20-bit level in the CS5503).



(a) Settling Time Due to Input Step Change



(b) Expanded Version of (a)

Figure 14. Output Settling



Bits of Output Accuracy	Filter Cycles	CLKIN Cycles
9	340	348,160
10	356	364,544
11	389	398,336
12	435	445,440
13	459	470,016
14	475	486,400
15	486	497,664
16	495	506,880
17	500	512,000
18	504	516,096
19	506	518,144
20	507	519,168

**Table 5. Settling Time of the 6 Pole Low Pass Filter in the CS5501 to 1/2 LSB Accuracy with a Full Scale Step Input**

Simple high frequency analog filtering in the signal conditioning circuitry can aid in removing energy at multiples of the sampling rate.

## Post Filtering

Post filtering is useful to enhance the noise performance of the CS5503. With a constant input voltage the output codes from the CS5503 will exhibit some variation due to noise. The CS5503 has typically 1.6 LSB<sub>20</sub> rms noise in its output codes. Additional variation in the output codes can arise due to noise from the input signal source and from the voltage reference. Post filtering (digital averaging) will be necessary to achieve less than 1 LSB p-p noise at the 20-bit level. The CS5503 has peak noise less than the 18-bit level without additional filtering if care is exercised in the design of the voltage reference and the input signal condition circuitry. Noise in the bandwidth from dc to 10 Hz on both the AIN and VREF inputs should be minimized to ensure maximum performance. As the amount of noise will be highly system dependent, a specific recommendation for post filtering for all applications cannot be stated. The following guidelines are helpful. Realize that the digital filter in the CS5503, like any other low pass filter, acts as an information storage unit. The filter retains past information for

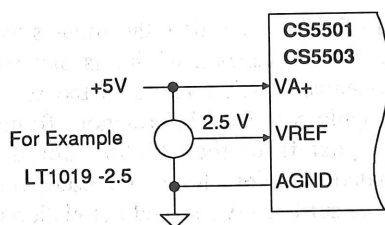
a period of time even after the input signal has changed. The implication of this is that immediately sequential 20-bit updates to the serial port contain highly correlated information. To most efficiently post filter the CS5503 output data, uncorrelated samples should be used. Samples which have sufficiently reduced correlation can be obtained if the CS5503 is allowed to execute 200 filter cycles between each subsequent data word collected for post filtering.

The character of the noise in the data will influence the post filtering requirements. As a general rule, averaging N uncorrelated data samples will reduce noise by  $1/\sqrt{N}$ . While this rule assumes that the noise is white (which is true for the CS5503 but not true for all real system signals between dc and 10Hz), it does offer a starting point for developing a post filtering algorithm for removing the noise from the data. The algorithm will have to be empirically tested to see if it meets the system requirements. It is recommended that any testing include input signals across the entire input span of the converter as the signal level will affect the amount of noise from the reference input which is transferred to the output data.

## Voltage Reference

The voltage reference applied to the VREF input pin defines the analog input range of the CS5501/CS5503. The preferred reference is 2.5V, but the device can typically accept references from 1V to 3V. Input signals which exceed 2.6V (+ or -) can cause some linearity degradation. Figure 15 illustrates the voltage reference connections to the CS5501/CS5503.

The circuitry inside the VREF pin is identical to that as seen at the AIN pin. The sample capacitor (see Figure 13) requires packets of charge from the external reference just as the AIN pin does. Therefore the same settling time requirements apply. Most reference IC's can handle this dynamic load requirement without inducing er-



**Figure 15. Voltage Reference Connections**

rors. They exhibit sufficiently low output impedance and wide enough bandwidth to settle to within the necessary accuracy in the requisite 64 CLKIN cycles.

Noise from the reference is filtered by the digital filter, but the reference should be chosen to minimize noise below 10 Hz. The CS5501/CS5503 typically exhibit 0.1 LSB rms and 1.6 LSB rms noise respectively. This specification assumes a clean reference voltage. Many monolithic band-gap references are available which can supply 2.5 V for use with the CS5501/CS5503. Many of these devices are not specified for noise, especially in the 0.1 to 10 Hz bandwidth. Some of these devices may exhibit noise characteristics which degrade the performance of the CS5501/CS5503.

### **Power Supplies And Grounding**

The CS5501/CS5503 use the analog ground connection, AGND, as a measurement reference node. It carries no power supply current. The AGND pin should be used as the reference node for both the analog input signal and for the reference voltage which is input into the VREF pin.

The analog and digital supply inputs are pinned out separately to minimize coupling between the analog and digital sections of the chip. To achieve maximum performance, all four supplies for the CS5501/CS5503 should be decoupled to their respective grounds using 0.1  $\mu$ F capacitors. This is illustrated in the System Connection

Diagram, Figure 1, at the beginning of this data sheet.

As CMOS devices, the CS5501/CS5503 require that the positive analog supply voltage always be greater than or equal to the positive digital supply voltage. If the voltage on the positive digital supply should ever become greater than the voltage on the positive analog supply, diode junctions in the CMOS structure which are normally reverse-biased will become forward-biased. This may cause the part to draw high currents and experience permanent damage. The connections shown in Figure 1 eliminate this possibility.

To ensure reliable operation, be certain that power is applied to the part before signals at AIN, VREF, or the logic input pins are present. If current is supplied into any pin before the chip is powered-up, latch-up may result. As a system, it is desirable to power the CS5501/CS5503, the voltage reference, and the analog signal conditioning circuitry from the same primary source. If separate supplies are used, it is recommended that the CS5501/CS5503 be powered up first. If a common power source is used for the analog signal conditioning circuitry as well as the A/D converter, this power source should be applied before application of power to the digital logic supply.

The CS5501/CS5503 exhibit good power supply rejection for frequencies within the passband (dc to 10 Hz). Any small offset or gain error caused by long term drift of the power supplies can be removed by recalibration. Above 10 Hz the digital filter will provide additional rejection. When the benefits of the digital filter are added to the regular power supply rejection the effects of line frequency variations (60 Hz) on the power supplies will be reduced greater than 120 dB. If the supply voltages for the CS5501/CS5503 are generated with a dc-dc converter the operating frequency of the dc-dc converter should not operate at the sampling frequency of the CS5501/CS5503 or at integer multiples thereof.



At these frequencies the digital filter will not aid in power supply rejection. See *Anti-Alias Considerations* section of this data sheet.

The recommended system connection diagram for the CS5501/CS5503 is illustrated in Figure 1. Note that any digital logic inputs which are to be unused should be tied to either DGND or the VD+ as appropriate. They should not be left floating; nor should they be tied to some other logic supply voltage in the system.

### Power-Up and Initialization

Upon power-up, a calibration cycle must be initiated at the CAL pin to insure a consistent starting condition and to initially calibrate the device. The CAL pin must be strobed high for a minimum of 4 clock cycles. The falling edge will initiate a calibration cycle. A simple power-on reset circuit can be built using a resistor and capacitor (see Figure 16). The resistor and capacitor values should allow for clock or oscillator startup time, and the voltage reference stabilization time.

Due to the devices' low power dissipation and low temperature drift, no warm-up time is required to accommodate any self-heating effects.

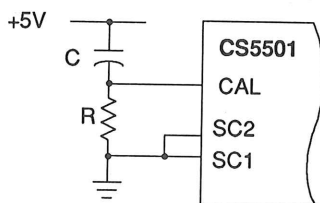


Figure 16. Power-On Reset Circuitry (Self-Calibration Only)

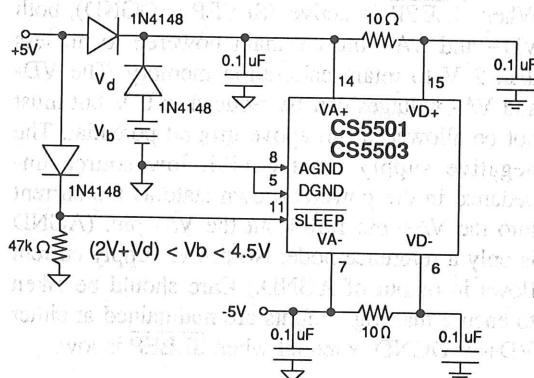


Figure 17. Example Calibration Memory Battery Back-Up Circuit

### Sleep Mode

The CS5501/CS5503 include a sleep mode ( $\overline{\text{SLEEP}} = \text{DGND}$ ) which shuts down the internal analog and digital circuitry reducing power consumption to less than 10  $\mu\text{W}$ . All calibration coefficients are retained in memory such that no time is required after "awakening" for recalibration. Still, the CS5501/CS5503 will require time for the digital filter to settle before an accurate reading will occur after a rising edge on  $\overline{\text{SLEEP}}$  occurs.

### Battery Backed-Up Calibrations

The CS5501/CS5503 use SRAM to store calibration information. The contents of the SRAM will be lost whenever power is removed from the chip. Figure 17 shows a battery back-up scheme that can be used to retain the calibration memory during system down time and/or protect it against intermittent power loss. Note that upon loss of power, the  $\overline{\text{SLEEP}}$  input goes low, reducing power consumption to just 10  $\mu\text{W}$ . Lithium cells of 3.6 V are available which average 1750 mA-hours before they drop below the typical 2 V memory-retention specification of the CS5501/CS5503.

When  $\overline{\text{SLEEP}}$  is active ( $\overline{\text{SLEEP}} = \text{DGND}$ ), both  $\text{VD}+$  and  $\text{VA}+$  must remain powered to no less than 2 V to retain calibration memory. The  $\text{VD}$ - and  $\text{VA}$ - voltages can be reduced to 0 V but must not be allowed to go above ground potential. The negative supply must exhibit low source impedance in the powered-down state as the current into the  $\text{VA}+$  pin flows out the  $\text{VA}$ - pin. (AGND is only a reference node. No power supply current flows in or out of AGND.) Care should be taken to ensure that logic inputs are maintained at either  $\text{VD}+$  or  $\text{DGND}$  potential when  $\overline{\text{SLEEP}}$  is low.

Note that battery life could be shortened if the +5 V supply drops slowly during power-down. As the supply drops below the battery voltage but not yet below the logic threshold of the  $\overline{\text{SLEEP}}$  pin, the battery will be supplying the CS5501/CS5503 at full power (typically 3 mA). Faster transitions at  $\overline{\text{SLEEP}}$  can be triggered using a resistive divider or a simple resistor network to generate the  $\overline{\text{SLEEP}}$  input from the +5 V supply.

### Output Loading Considerations

To maximize performance of the CS5501/CS5503, the output drive currents from the digital output lines should be minimized. It is recommended that CMOS logic gates (4000B, 74HC, etc.) be used to provide minimum loading. If it is necessary to drive an opto-isolator the outputs of the CS5501/CS5503 should be buffered. An easy means of driving the LED of an opto-isolator is to use a 2N7000 or 2N7002 low cost FET.

### PIN DESCRIPTIONS

SERIAL INTERFACE MODE SELECT	<b>MODE</b>	1	20	<b>SDATA</b>	SERIAL DATA OUTPUT
CLOCK OUT	<b>CLKOUT</b>	2	19	<b>SCLK</b>	SERIAL CLOCK INPUT/OUTPUT
CLOCK IN	<b>CLKIN</b>	3	18	<b>DRDY</b>	DATA READY
SYSTEM CALIBRATION 1	<b>SC1</b>	4	17	<b>SC2</b>	SYSTEM CALIBRATION 2
DIGITAL GROUND	<b>DGND</b>	5	16	<b>CS</b>	CHIP SELECT
NEGATIVE DIGITAL POWER	<b>VD-</b>	6	15	<b>VD+</b>	POSITIVE DIGITAL POWER
NEGATIVE ANALOG POWER	<b>VA-</b>	7	14	<b>VA+</b>	POSITIVE ANALOG POWER
ANALOG GROUND	<b>AGND</b>	8	13	<b>CAL</b>	CALIBRATE
ANALOG IN	<b>AIN</b>	9	12	<b>BP/UP</b>	BIPOLAR/UNIPOLAR SELECT
VOLTAGE REFERENCE	<b>VREF</b>	10	11	<b>SLEEP</b>	SLEEP

\* Pinout applies to both DIP and SOIC packages

3

### Clock Generator

#### CLKIN; CLKOUT -Clock In; Clock Out, Pins 3 and 2.

A gate inside the CS5501/CS5503 is connected to these pins and can be used with a crystal or ceramic resonator to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be input to the CLKIN pin as the master clock for the device. When not in SLEEP mode, a master clock (CLKIN) should be present at all times.

### Serial Output I/O

#### MODE -Serial Interface Mode Select, Pin 1.

Selects the operating mode of the serial port. If tied to VD- (-5V), the CS5501 will operate in the UART-compatible AC mode for Asynchronous Communication. The SCLK pin will operate as an *input* to set the data rate, and data will transmit *formatted* with one start and two stop bits. If MODE is tied to DGND, the CS5501/CS5503 will operate in the SEC (Synchronous External-Clocking) mode, with the SCLK pin operating as an *input* and the output appearing MSB-first. If MODE is tied to VD+ (+5V), the CS5501/CS5503 will operate in its SSC (Synchronous Self-Clocking) mode, with SCLK providing a serial clock *output* of CLKIN/4 (25% duty-cycle).

#### DRDY -Data Ready, Pin 18.

**DRDY** goes low every 1024 cycles of CLKIN to indicate that new data has been placed in the output port. **DRDY** goes high when all the serial port data is clocked out, when the serial port is being updated with new data, when a calibration is in progress, or when SLEEP is low.

#### CS -Chip Select, Pin 16.

An input which can be enabled by an external device to gain control over the serial port of the CS5501/CS5503.

**SDATA -Serial Data Output, Pin 20.**

Data from the serial port will be output from this pin at a rate determined by SCLK and in a format determined by the MODE pin. It furnishes a high impedance output state when not transmitting data.

**SCLK -Serial Clock Input/Output, Pin 19.**

A clock signal at this pin determines the output rate of the data from the SDATA pin. The MODE pin determines whether the SCLK signal is an input or output. SCLK may provide a high impedance output when data is not being output from the SDATA pin.

**Calibration Control Inputs****SC1; SC2 -System Calibration 1 and 2, Pins 4 and 17.**

Control inputs to the CS5501/CS5503's calibration microcontroller for calibration. The state of SC1 and SC2 determine which of the calibration modes is selected for operation (see Table 2).

**BP/ $\overline{\text{UP}}$  -Bipolar/Unipolar Select, Pin 12.**

Determines whether the CS5501/CS5503 will be calibrated to measure bipolar ( $\text{BP}/\overline{\text{UP}} = \text{VD}+$ ) or unipolar ( $\text{BP}/\overline{\text{UP}} = \text{DGND}$ ) input signals. Recalibration is necessary whenever the state of  $\text{BP}/\overline{\text{UP}}$  is changed.

**CAL -Calibrate, Pin 13.**

If brought high for 4 clock cycles or more, the CS5501/CS5503 will reset and upon returning low a full calibration cycle will begin. The state of SC1, SC2, and  $\text{BP}/\overline{\text{UP}}$  when CAL is brought low determines the type and length of calibration cycle initiated (see Table 2). Also, a single CAL signal can be used to strobe the CAL pins high on several CS5501/CS5503's to synchronize their operation. Any spurious glitch on this pin may inadvertently place the chip in Calibration mode.

**Other Control Input****SLEEP -Sleep, Pin 11.**

When brought low, the CS5501/CS5503 will enter a low-power state. When brought high again, the CS5501/CS5503 will resume operation without the need to recalibrate. After SLEEP goes high again, the device's output will settle to within  $\pm 0.0007\%$  of the analog input value within  $1.3/f_{3\text{dB}}$ , where  $f_{3\text{dB}}$  is the passband frequency. The SLEEP input can also be used to synchronize sampling and the output updates of several CS5501/CS5503's.

**Analog Inputs****VREF -Voltage Reference, Pin 10.**

Analog reference voltage input.

**AIN -Analog Input, Pin 9.**

## Power Supply Connections

### VD+ -Positive Digital Power, Pin 15.

Positive digital supply voltage. Nominally +5 volts.

### VD- -Negative Digital Power, Pin 6.

Negative digital supply voltage. Nominally -5 volts.

### DGND -Digital Ground, Pin 5.

Digital ground.

### VA+ -Positive Analog Power, Pin 14.

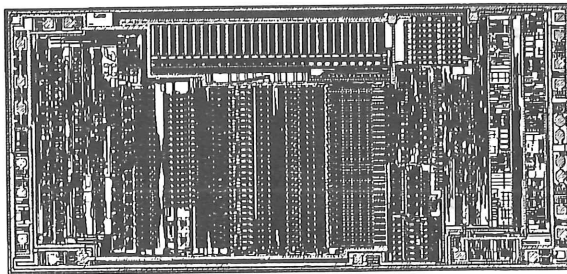
Positive analog supply voltage. Nominally +5 volts.

### VA- -Negative Analog Power, Pin 7.

Negative analog supply voltage. Nominally -5 volts.

### AGND -Analog Ground, Pin 8.

Analog ground.

**DIE INFORMATION**

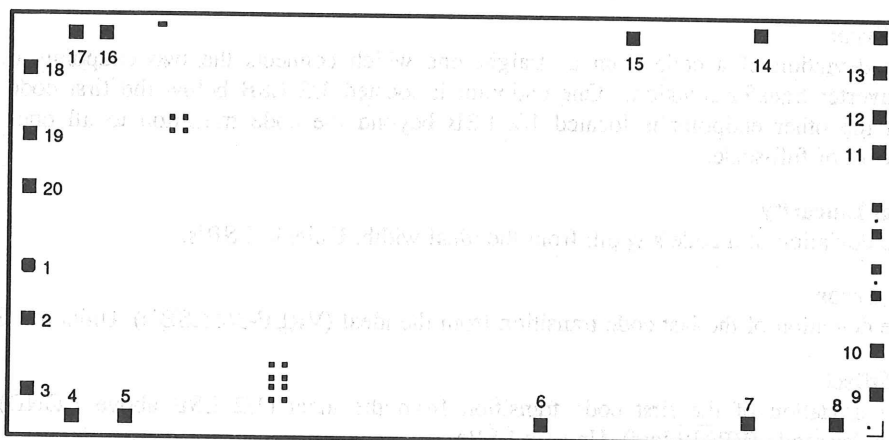
**CS5501-YU  
CS5503-YU**

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening and inspection procedures, packing, shipping, and change notification.

***Assembly Information***

1. Die size shall be 0.149" by 0.303" ( $\pm 0.002$ ")
2. The die are suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.
3. Die thickness shall be 0.0175"  $\pm 0.0035$ ". If tighter tolerances are required, contact the factory.
4. The maximum number of die per waffle pack carrier is 28.
5. The cavity dimensions for each die within the waffle pack are .180" by .330" (Waffle Pack Type H20-179329).
6. The die require no particular bonding sequence.
7. Each pin of the CS5501 and CS5503 has ESD and latch-up protection circuitry. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.
8. Technical constraints limit the viability of accurate performance measurements of precision analog IC's at wafer probe. Although high yield to the limits listed in the specification tables is anticipated, no guarantee is given for unpackaged die product.

**CS5501-YU, CS5503-YU Bonding Diagram**



3

1	-	MODE	11	-	<u>SLEEP</u>
2	-	CLKOUT	12	-	BP/UP
3	-	CLKIN	13	-	CAL
4	-	SC1	14	-	VA+
5	-	DGND	15	-	<u>VD+</u>
6	-	VD-	16	-	<u>CS</u>
7	-	VA-	17	-	<u>SC2</u>
8	-	AGND	18	-	<u>DRDY</u>
9	-	AIN	19	-	SCLK
10	-	VREF	20	-	SDATA



## **SPECIFICATION DEFINITIONS**

### **Linearity Error**

The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

### **Differential Linearity**

The deviation of a code's width from the ideal width. Units in LSB's.

### **Full-Scale Error**

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSBs.

### **Unipolar Offset**

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSBs.

### **Bipolar Offset**

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/UP high). Units in LSBs.

### **Bipolar Negative Full-Scale Error**

The deviation of the first code transition from the ideal when in bipolar mode (BP/UP high). The Ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSBs.

### **Positive Full-Scale Input Overrange**

The absolute maximum positive voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

### **Negative Full-Scale Input Overrange**

The absolute maximum negative voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

### **Offset Calibration Range**

The CS5501/CS5503 calibrate their offset to the voltage applied to the AIN pin when in system calibration mode. The first code transition defines Unipolar Offset when BP/UP is low and the mid-scale transition defines Bipolar Offset when BP/UP is high. The Offset Calibration Range specification indicates the range of voltages applied to AIN that the CS5501 or CS5503 can accept and still calibrate offset accurately. Units in volts.

### **Input Span**

The voltages applied to the AIN pin in system-calibration schemes define the CS5501/CS5503 analog input range. The Input Span specification indicates the minimum and maximum input spans from zero-scale to full-scale in unipolar, or from positive full scale to negative full scale in bipolar, that the CS5501/CS5503 can accept and still calibrate gain accurately. Units in volts.

### Ordering Guide

Model Number	No. of Bits	Linearity Error (Max)	Temperature Range	Package
CS5501-AS	16	0.003%	-40 to +85°C	20 Lead SOIC
CS5501-BS	16	0.0015%	-40 to +85°C	20 Lead SOIC
CS5501-AP	16	0.003%	-40 to +85°C	20 Pin Plastic DIP
CS5501-BP	16	0.0015%	-40 to +85°C	20 Pin Plastic DIP
CS5501-CP	16	0.0012%	-40 to +85°C	20 Pin Plastic DIP
CS5501-SD	16	0.003%	-55 to +125°C	20 Pin Cerdip
CS5501-TD	16	0.0015%	-55 to +125°C	20 Pin Cerdip
CS5501-YU	16			Unpackaged Die
CDB5501	Evaluation Board			
CS5503-AS	20	0.003%	-40 to +85°C	20 Lead SOIC
CS5503-BS	20	0.0015%	-40 to +85°C	20 Lead SOIC
CS5503-AP	20	0.003%	-40 to +85°C	20 Pin Plastic DIP
CS5503-BP	20	0.0015%	-40 to +85°C	20 Pin Plastic DIP
CS5503-CP	20	0.0012%	-40 to +85°C	20 Pin Plastic DIP
CS5503-SD	20	0.003%	-55 to +125°C	20 Pin Cerdip
CS5503-TD	20	0.0015%	-55 to +125°C	20 Pin Cerdip
CS5503-YU	20			Unpackaged Die
CDB5503	Evaluation Board			

## APPENDIX A: APPLICATIONS

### Parallel Interface

Figures A1 and A2 show two serial-to-parallel conversion circuits for interfacing the CS5501 in its SSC mode to 16- and 8-bit systems respectively. Each circuit includes an optional 74HCT74 flip-flop to latch  $\overline{\text{DRDY}}$  and generate a level-sensitive interrupt.

Both circuits require that the parallel read process be synchronized to the CS5501's operation. That is, the system must not try to enable the registers' parallel output while they are accepting serial data from the CS5501. The CS5501's  $\overline{\text{DRDY}}$  falls just prior to serial data transmission and

returns high as the last bit shifts out. Therefore, the  $\overline{\text{DRDY}}$  pin can be polled for a *rising* transition directly, or it can be latched as a level-sensitive interrupt.

With the  $\overline{\text{CS}}$  input tied low the CS5501 will shift out every available sample (4kHz word rate with a 4MHz master clock). Lower output rates (and interrupt rates) can be generated by dividing down the  $\overline{\text{DRDY}}$  output and applying it to  $\overline{\text{CS}}$ .

Totally asynchronous interfaces can be created using a *Shift Data* control signal from the system which enables the CS5501's  $\overline{\text{CS}}$  input and/or the shift registers' S1 inputs. The  $\overline{\text{DRDY}}$  output can then be used to disable serial data transmission once an output word has been fully registered.

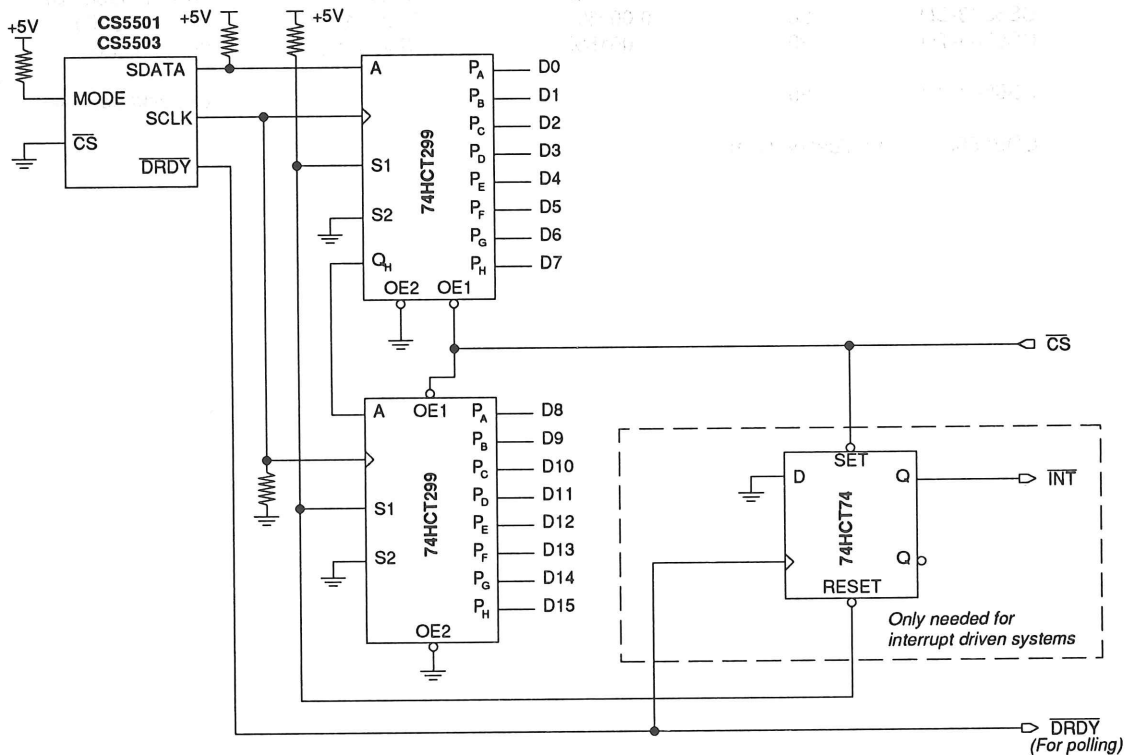


Figure A1. 16-bit Parallel Interface

In such asynchronous configurations the CS5501 is operated much like a successive-approximation converter with a *Convert* signal and a subsequent read cycle.

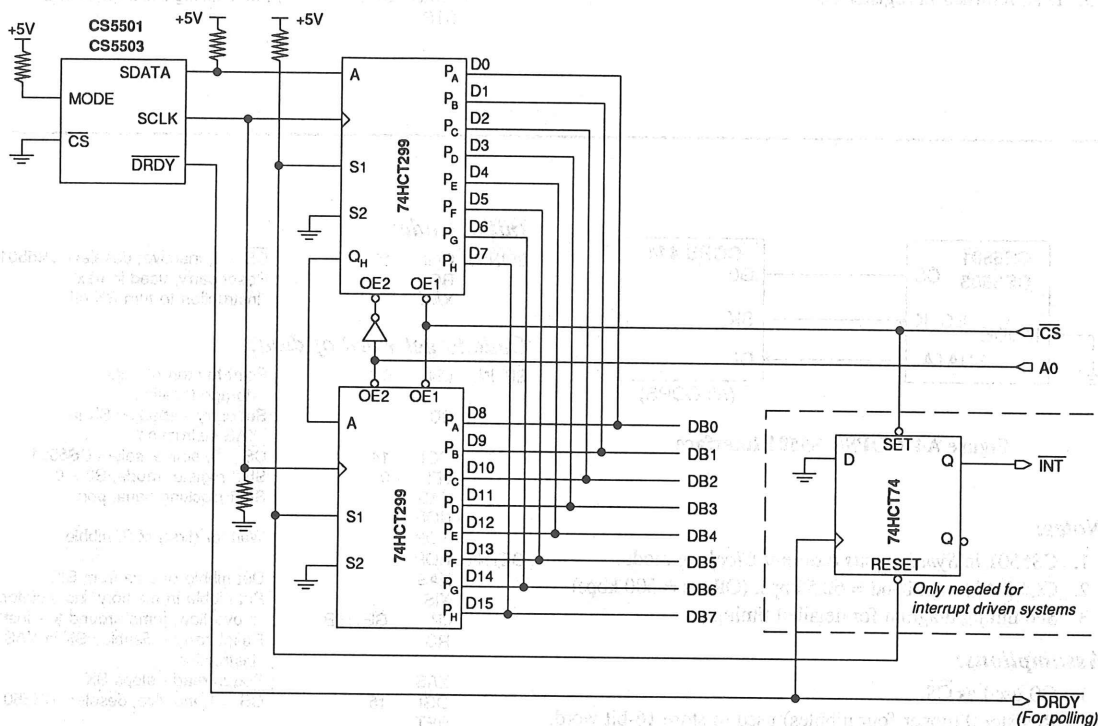
If it is required to latch the 16-bit data, then 2 74HC595 8-bit "shift register with latch" parts may be used instead of 74HC299's.

## Serial Interfaces

Figures A3 to A8 offer both the hardware and software interfaces to several industry-standard microcontrollers using the CS5501's SEC and AC output modes. In each instance a system initialization routine is provided which configures the controller's I/O ports to accept the CS5501's serial data and clock outputs and/or generate its

own serial clock. The routine also sets the CS5501 into a known state.

For each interface, a second subroutine is also provided which will collect one complete 16-bit output word from the CS5501. Figure A5 illustrates the detailed timing throughout the subroutine for one particular interface - the COPS family interface of Figure A4.



### Figure A2. 8-Bit Parallel Interface

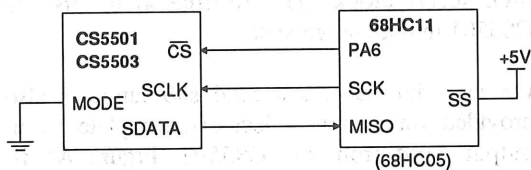


Figure A3. 68HC11/CS5501 Serial Interface

### Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. Using 68HC11's SPI port. (Can use SCI and CS5501's Asynchronous mode.)
3. Maximum bit rate is 1.05 Mbps.

### Assumptions:

1. PA6 used as  $\overline{CS}$ .
2. 68HC11 in single-chip mode.
3. Receive data via polling.
4. Normal equates for peripheral registers.
5. Data returned in register D.

### Initial Code:

```
SPINIT: PSHA          ; Store temporary copy of A
        LDAA  #0x1xxxxx ; Bit 6 = 1, all others are don't cares
        STAA  PORTA      ; CS = 1, inactive; deselect CS5501
        LDAA  #0x10
        STAA  SPCR        ; Disable serial port
        LDAA  #0xx0110xx ; SS-input, SCK-output,
                          ; MOSI-output, MISO-input
        STAA  DDRD        ; Data direction register for port D
        LDAA  #0x50       ; Enable serial port, CMOS outputs,
                          ; master, highest clock rate (int. clk/2)
        STAA  SPCR
        LDAA  SPSR
        LDAA  SPDR        ; Bogus read to clr port and SPIF flag
        PULA             ; Restore A
        RTS
```

### Code to get word of data:

```
SP_IN:  LDAA  #0x0xxxxxx ; CS = 0, active; select CS5501
        STAA  PORTA      ; Put data in serial port to start clk
        STAA  SPDR        ; Get port status
WAIT1:  LDAA  SPSR        ; If SPIF (MSB) 0, no data yet, wait
        BPL  WAIT1
        LDAA  SPDR        ; Put most significant byte in A
        STAA  SPDR        ; Start serial port for second byte
WAIT2:  LDAB  SPSR        ; Get port status
        BPL  WAIT2        ; If SPIF (MSB) 0, no data yet, wait
        LDAB  #0x1xxxxxx ; CS = 1, inactive; deselect CS5501
        STAB  PORTA      ; Put least significant byte in B
        LDAB  SPDR
        RTS
```

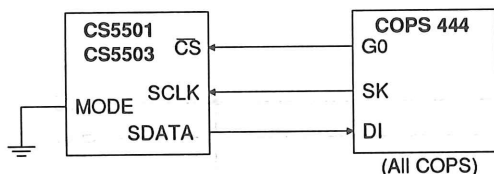


Figure A4. COPS/CS5501 Interface

### Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. COPS 444 max baud = 62.5 kbps. (Others = 500 kbps)
3. See timing diagram for detailed timing.

### Assumptions:

1. G0 used as  $\overline{CS}$ .
2. Register 0 (upper four nibbles) used to store 16-bit word.

### Initial Code:

```
SPINIT: OGI  15          ; CS = 1, inactive; deselect CS5501
        RC
        XAS             ; Reset carry, used in next
                          ; instruction to turn SK off
```

### Code to get word of data:

```
SP_IN:  LBI  0,12        ; Point to start of data
                          ; storage location
        SC              ; Set carry - enables SK in
                          ; XAS instruction
        OGI  14          ; CS = 0, active; select CS5501
        LEI  0           ; Shift register mode, S0 = 0
        XAS             ; Start clocking serial port
        NOP
        NOP              ; Wait for (first) M.S. nibble
GETNIB: NOP
        XAS
        XIS             ; Get nibble of data from SIO
        JP  GETNIB       ; Put nibble in memory, inc. pointer,
                          ; if overflow, jump around this inst.
        RC              ; Reset carry - disables SK in XAS
                          ; instruction
        XAS             ; Bogus read - stops SK
        OGI  15          ; CS = 1, inactive; deselect CS5501
        RET
```

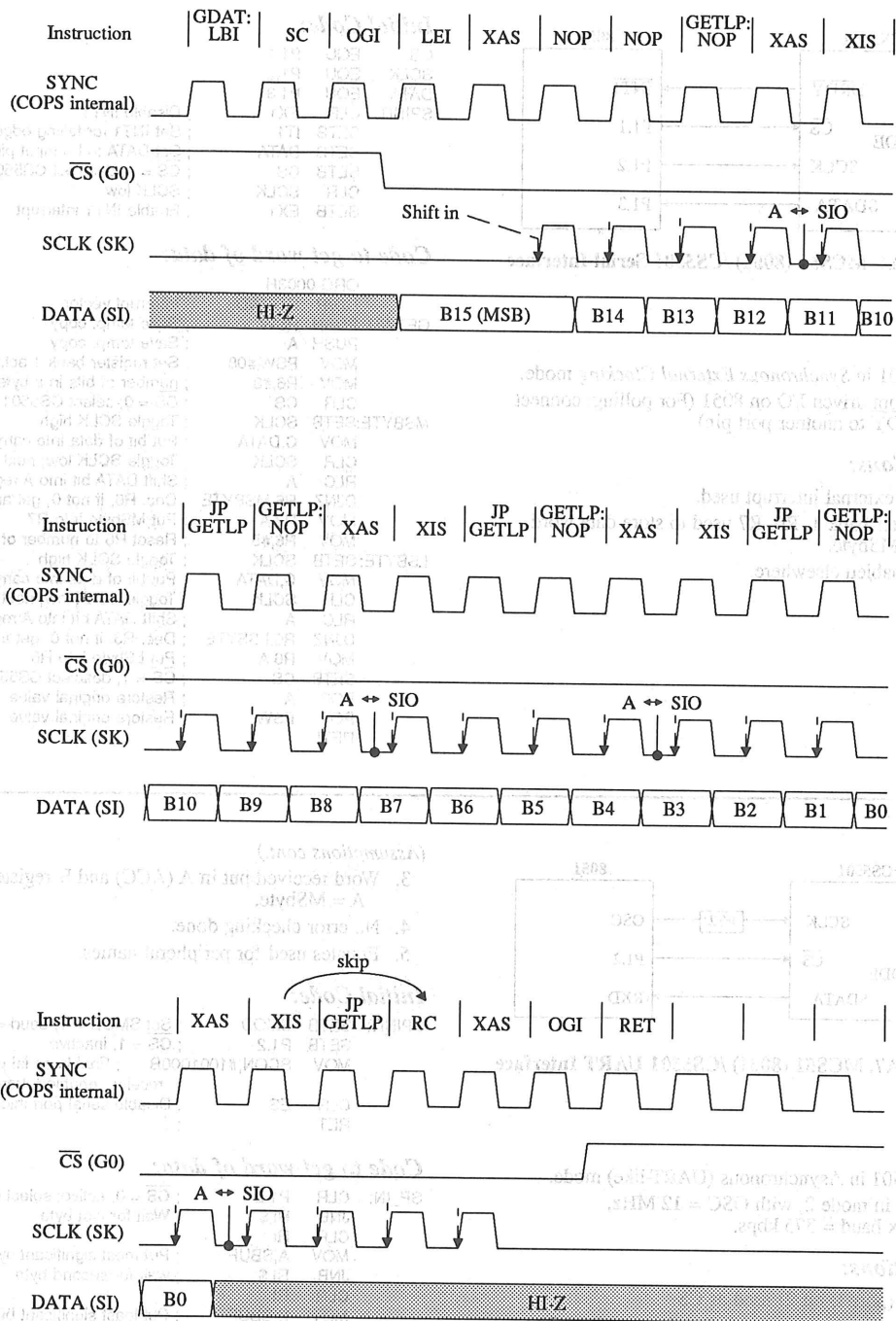


Figure A5. Serial Timing Example - COPS

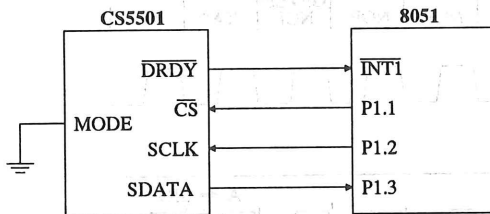


Figure A6. MCS51 (8051) /CS5501 Serial Interface

### Notes:

1. CS5501 in Synchronous External Clocking mode.
2. Interrupt driven I/O on 8051 (For polling, connect DRDY to another port pin).

### Assumptions:

1. INT1 external interrupt used.
2. Register bank 1, R6, R7 used to store data word, R7 MSbyte.
3. EA enabled elsewhere.

### Initial Code:

```
CS EQU P1.1
SCLK EQU P1.2
DATA EQU P1.3
SPINIT: CLR EX1 ; Disable INT1
        SETB IT1 ; Set INT1 for falling edge triggered
        SETB DATA ; Set DATA to be input pin
        SETB CS ; CS = 1; deselect CS5501
        CLR SCLK ; SCLK low
        SETB EX1 ; Enable INT1 interrupt
```

### Code to get word of data:

```
ORG 0003H
LJMP GETWD ; Interrupt vector
GETWD: PUSH PSW ; Save temp. copy
      PUSH A ; Save temp. copy
      MOV PSW,#08 ; Set register bank 1 active
      MOV R6,#8 ; number of bits in a byte
      CLR CS ; CS = 0; select CS5501
MSBYTE: SETB SCLK ; Toggle SCLK high
        MOV C,DATA ; Put bit of data into carry bit
        CLR SCLK ; Toggle SCLK low; next data bit
        RLC A ; Shift DATA bit into A register
        DJNZ R6,MSBYTE ; Dec. R6, if not 0, get another bit
        MOV R7,A ; Put MSbyte into R7
        MOV R6,#8 ; Reset R6 to number of bits in byte
LSBYTE: SETB SCLK ; Toggle SCLK high
        MOV C,DATA ; Put bit of data into carry bit
        CLR SCLK ; Toggle SCLK low; next data bit
        RLC A ; Shift DATA bit into A register
        DJNZ R6,LSBYTE ; Dec. R6, if not 0, get another bit
        MOV R6,A ; Put LSbyte into R6
        SETB CS ; CS = 1; deselect CS5501
        POP A ; Restore original value
        POP PSW ; Restore original value
        RETI
```

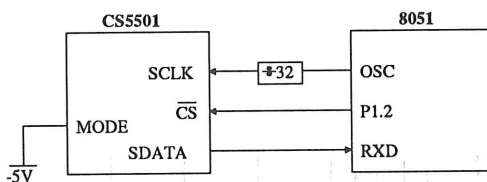


Figure A7. MCS51 (8051) /CS5501 UART Interface

### Notes:

1. CS5501 in Asynchronous (UART-like) mode.
2. 8051 in mode 2, with OSC = 12 MHz, max baud = 375 kbps.

### Assumptions:

1. P1.2 (port 1, bit 2) used as CS.
2. Using serial port mode 2, Baud rate = OSC/32.

### (Assumptions cont.)

3. Word received put in A (ACC) and B registers, A = MSbyte.
4. No error checking done.
5. Equates used for peripheral names.

### Initial Code:

```
SPINIT: SETB SMOD ; Set SMOD = 1, baud = OSC/32
        SETB P1.2 ; CS = 1, inactive
        MOV SCON,#1001000B ; Enable serial port mode 2,
        ; receiver enabled, transmitter disabled
        CLR ES ; Disable serial port interrupts (polling)
        RET
```

### Code to get word of data:

```
SP_IN: CLR P1.2 ; CS = 0, active; select CS5501
       JNB RI,$ ; Wait for first byte
       CLR RI
       MOV A,SBUF ; Put most significant byte in A
       JNB RI,$ ; wait for second byte
       CLR RI
       MOV B,SBUF ; Put least significant byte in B
       SETB P1.2 ; CS = 1, inactive; deselect CS5501
       RET
```



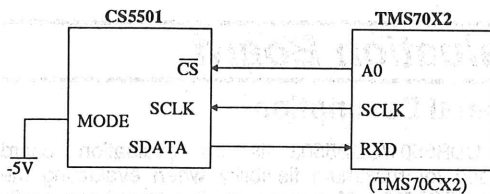


Figure A8. TMS70X2/CS5501 Serial Interface

### Initial Code:

```
SPINIT: DINT
        MOVP %1,ADDR      ; A port is output
        MOVP %1,APOINT    ; A0 = 1, (CS is inactive)
        MOVP %0,P17
        MOVP %>10,SCTLO    ; Resets port errors
        MOVP %?x1x01101,SMODE ; Set port for Isosync,
        MOVP %?00x1110x,SCTLO ; 8 bits, no parity
        MOVP %07,T3DATA ; Max baud rate
        MOVP %?01000000,SCTL1 ; No multiprocessor;
                                ; prescale = 4
        MOVP %0,IOCNT1    ; Disable INT4 - will poll port
        PUSH A             ; Store original
        MOVP RXBUF,A       ; Bogus read to clr receiver port flag
        POP A              ; Restore original
        EINT
        RET
```

### Code to get word of data:

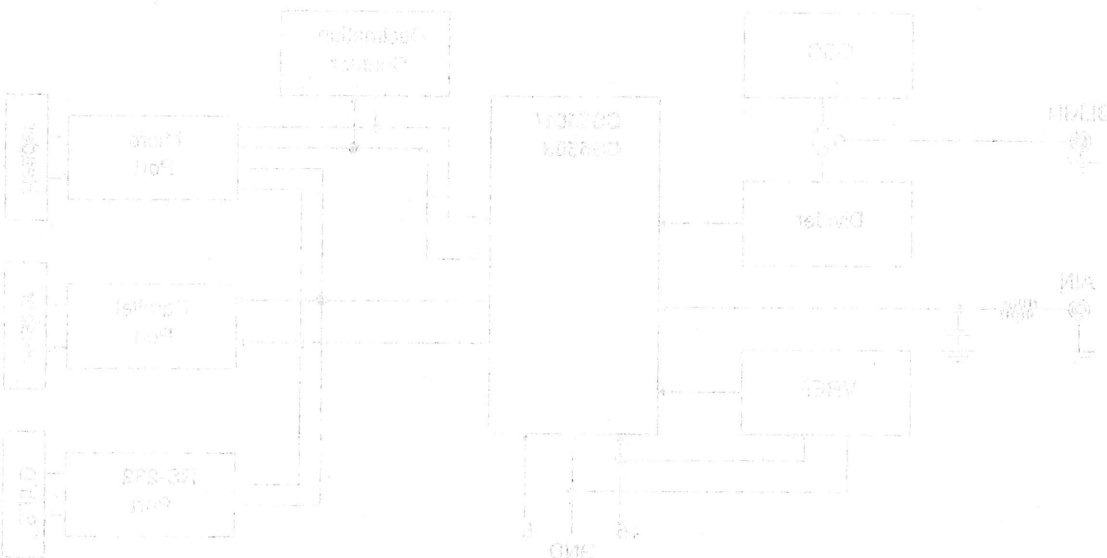
```
SP_IN:  MOVP %0,APOINT    ; CS active, select CS5501
WAIT1:  BTJZP %2,SSTAT,WAIT1 ; Wait to receive first byte
        MOVP RXBUF,A       ; Put most significant byte in reg. A
WAIT2:  BTJZP %2,SSTAT,WAIT2 ; Wait to receive second byte
        MOVP RXBUF,B       ; Put least significant byte in reg. B
        MOVP %1,APOINT    ; CS inactive, deselect CS5501
        RET
```

### Notes:

1. CS5501 in Asynchronous (UART-like) mode.
2. TMS70X2 in Isosynchronous mode.
3. TMS70X2 with 8 MHz master clock has max baud = 1.0 Mbps.

### Assumptions:

1. A0 used as CS.
2. Receive data via polling.
3. Word received put in A and B upon return, A = MS byte.
4. No error checking done.
5. Normal equates for peripheral registers.



## **CS5501 /CS5503 Evaluation Board**

### **Features**

- Operation with on-board clock generator, on-board crystal, or an off-board clock source.
- DIP switch selectable or micro port controllable:
  - Unipolar/Bipolar input range
  - Sleep Mode
  - All Cal Modes
- On-board Decimation Counter
- Multiple Data Output Interface Options:
  - RS-232 (CS5501)
  - Parallel Port (CS5501)
  - Micro Port (CS5501 & CS5503)

### **General Description**

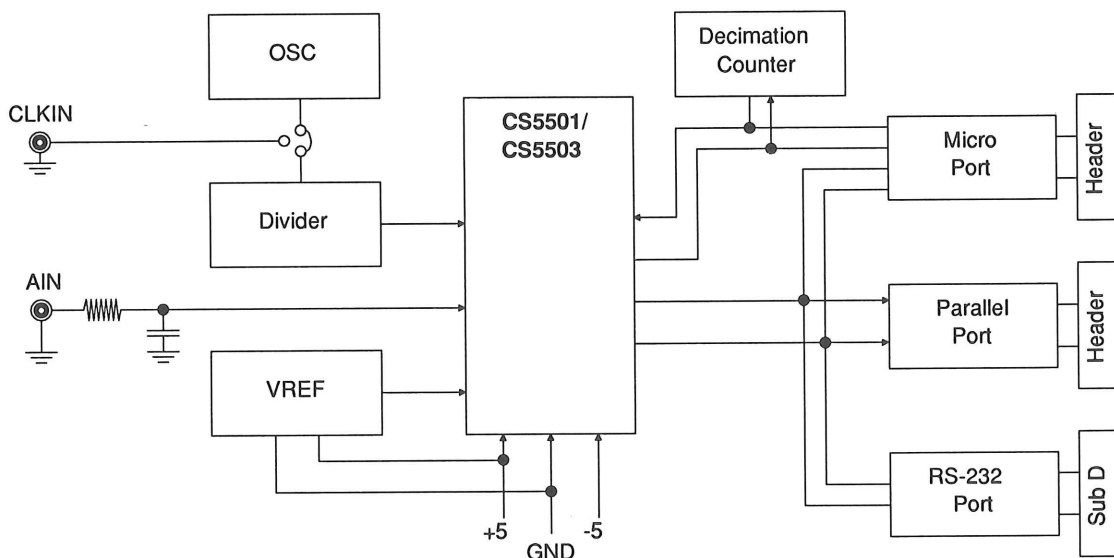
The CDB5501/CDB5503 is an evaluation board designed for maximum flexibility when evaluating the CS5501/CS5503 A/D converters. The board can easily be configured to evaluate all the features of the CS5501/CS5503, including changes in master clock rate, calibration modes, output decimation rates, and interface modes.

The evaluation board interfaces with most microcontrollers and allows full control of the features of the CS5501 or CS5503. DIP switch selectable control is also available in the event a microcontroller is not used. The evaluation board also offers computer data interfaces including RS-232 and parallel port outputs for evaluating the CS5501.

All calibration modes are selectable including Self-Cal, System Offset Cal, and System Offset and System Gain Cal. A calibration can be initiated at any time by pressing the CAL pushbutton switch.

**ORDERING INFORMATION:** CDB5501 or CDB5503

### **Block Diagram**



## INTRODUCTION

The CDB5501/CDB5503 evaluation board provides maximum flexibility for controlling and interfacing to the CS5501/CS5503 A/D converters. The CS5501 or the CS5503 require a minimal amount of external circuitry. The devices can operate with a crystal (or ceramic resonator) and a voltage reference.

The evaluation board includes several clock source options, a 2.5 volt trimmable reference, and circuitry to support several data interface schemes. The board operates from +5 and -5 volt power supplies.

### *Evaluation Board Overview*

The CDB5501/CDB5503 evaluation board includes extensive support circuitry to aid evaluation of the CS5501/CS5503. The support circuitry includes the following sections:

- 1) A clock generator which has an on-board oscillator and counter divider IC.
- 2) A 2.5 volt trimmable voltage reference.
- 3) A Decimation Counter.
- 4) A parallel output port (for CS5501 only).
- 5) An RS-232 interface (for CS5501 only).
- 6) A micro port (for CS5501 or CS5503).
- 7) DIP switch and CAL pushbutton.

### *Clock Generator*

The CS5501/CS5503 can operate off its on-chip oscillator or an off-chip clock source. The evaluation board includes a 4.9152 MHz gate oscillator and counter-divider chain as the primary clock source for the CS5501/CS5503. The counter-divider outputs offer several jumper-selectable frequencies as clock inputs to the CS5501/CS5503. The 4.9152 MHz crystal frequency was chosen to allow the counter-divider chain to also provide the common serial data rates

(1200, 2400, 4800, etc.) when the CDB5501 evaluation board is configured to provide RS-232 data output. If a different operating frequency for the CS5501/CS5503 is desired, three options exist. First, a BNC input is provided to allow an external CMOS (+5V) compatible clock to be used. Second, the crystal (Y1) in the on-board gate oscillator can be changed. Or, third, the on-chip oscillator of the CS5501/CS5503 can be used with a crystal connected in the Y2 position.

### *2.5 Volt Reference*

A 2.5 volt (LT1019CN8-2.5) reference is provided on the board. Potentiometer R9 allows the initial value of the reference to be accurately trimmed.

### *Decimation Counter*

The CS5501/CS5503 updates its internal output register with a 16-bit word every 1024 clock cycles of the master clock. Each time the output register is updated the  $\overline{\text{DRDY}}$  line goes low. Although output data is updated at a high rate it may be desirable in certain applications to activate the  $\overline{\text{CS}}$  to read the data at a much lower rate. A decimation counter is provided on the board for this purpose. The counter reduces the rate at which the  $\overline{\text{CS}}$  line of the CS5501 is activated by only allowing  $\overline{\text{CS}}$  to occur at a sub-multiple of the  $\overline{\text{DRDY}}$  rate.

### *Parallel Output Port (for CS5501 only)*

The output data from the CS5501/CS5503 is in serial form. Some applications may require the data to be read in parallel format. Therefore the evaluation board includes two 8-bit shift registers with three-state outputs. Data from the CS5501 is shifted into the registers and then read out in 16-bit parallel fashion. The parallel port comes set up for 16-bit parallel output but can be reconfigured to provide two 8-bit reads. The parallel port supports the CS5501 only, since the CS5503 outputs 20-bit words.



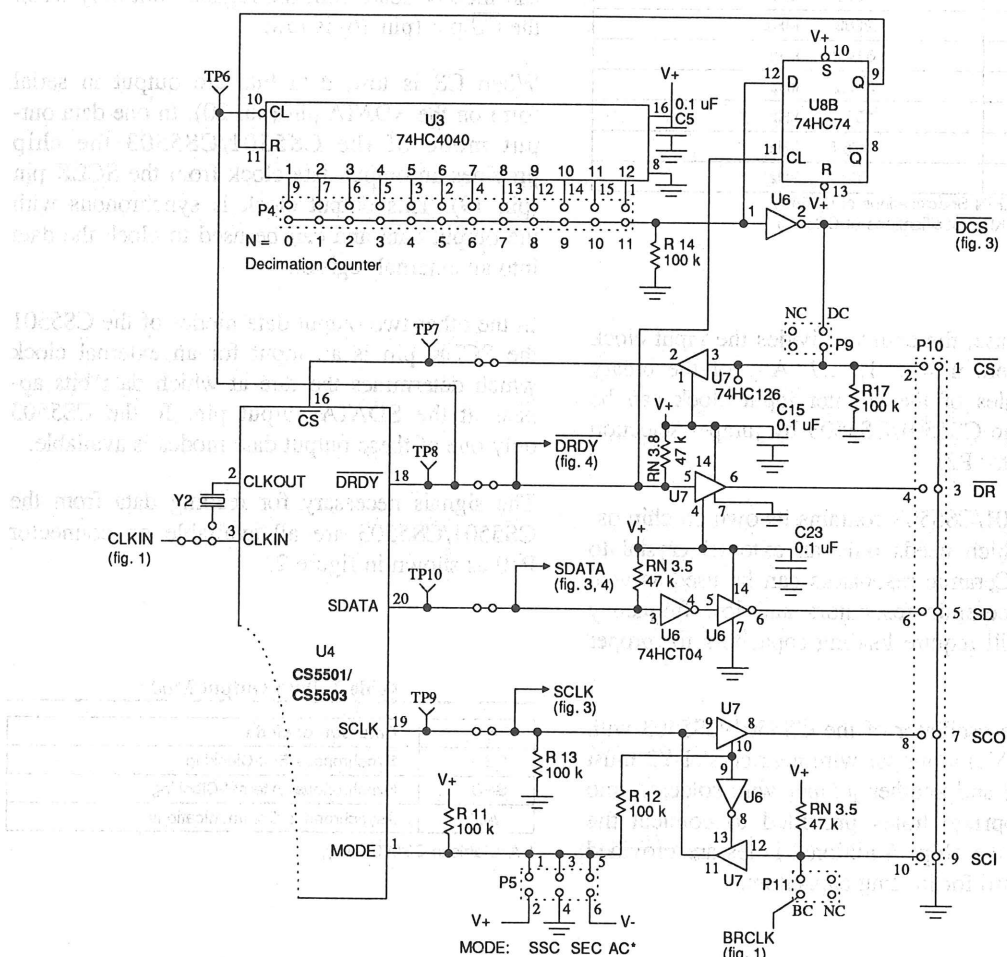
### *Clock Options*

Several clock source options are available. These include:

- 1) an external clock (+5 V CMOS-Compatible);
- 2) an on-board 4.9152 MHz crystal oscillator with a  $2^n$  divider ( $n = 1, 2, \dots, 7$ );
- 3) a 4.096 MHz crystal.

Connector P1 allows jumper selection of either an external clock or the on-board 4.9152 MHz crystal oscillator (See figure 1 for schematic) as the clock source for the CLKIN signal on pin 3 of the CS5501/CS5503 (shown in figure 2).

If the EXT position is selected, a CMOS-compatible clock signal (5 volt supply) should be input to the BNC connector labelled CLKIN. If the INT position is selected the 4.9152 MHz oscillator output is input to counter/divider IC U2.



**Figure 2. Decimation Counter / Microport**

Table 1. Clock Generator

P-1	CLKIN Source to CS5501/CS5503
INT CLK	On-Board 4.9152 MHz OSC
EXT CLK	+5 CMOS CLKIN BNC

CLKIN Rate Selection (CLK/2<sup>n</sup>) with INT CLK on P1 selected.  
CLK = 4.9152 MHz

P-2	CLKIN Rate
0	4.9152 MHz* +
1	2.4576 MHz
2	1.2288 MHz
3	614.4 kHz
4	307.2 kHz
5	153.6 kHz +
6	76.8 kHz +
7	38.4 kHz* +

\* Exceeds CLKIN Specifications of CS5501.

+ Exceeds CLKIN specifications of CS5503

In either case, the counter divides the input clock by 2<sup>n</sup> where n = 0, 1, ...7. Any of the binary sub-multiples of the counter input clock can be input to the CS5501/CS5503 by jumper selection on connector P2.

The CS5501/CS5503 contains its own on-chip oscillator which needs only an external crystal to function. Ceramic resonators can be used as well although ceramic resonators and low frequency crystals will require loading capacitors for proper operation.

To test the oscillator of the CS5501/CS5503 with a crystal (Y2) a jumper wire near crystal Y2 must be opened and another jumper wire soldered into the appropriate holes provided to connect the crystal to the chip. Additional holes are provided on the board for loading capacitors.

## Data Output from the CS5501/CS5503

The CS5501 has three available data output modes (The CS5503 has two available data output modes). The operating mode of the part is determined by the input voltage level to the MODE (pin 1) pin of the device. Once a mode is selected, four other pins on the device are involved in data output. The first of these is the DRDY pin (pin 18). It is an output from the chip which signals whenever a new data word is available in the internal output register of the CS5501/CS5503. Data can then be read from the register, but only when the CS pin (pin 16) is low.

When CS is low, data bits are output in serial form on the SDATA pin (pin 20). In one data output mode of the CS5501/CS5503 the chip provides an output data clock from the SCLK pin (pin 19). This output clock is synchronous with the output data and can be used to clock the data into an external register.

In the other two output data modes of the CS5501 the SCLK pin is an input for an external clock which determines the rate at which data bits appear at the SDATA output pin. In the CS5503 only one of these output data modes is available.

The signals necessary for reading data from the CS5501/CS5503 are all available on connector P10 as shown in figure 2.

Table 2. Data Output Mode

P-5	Data Output Mode
SSC	Synchronous Self-Clocking
SEC	Synchronous External-Clocking
AC*	Asynchronous Communications

\* Available in CS5501 only.

## CS5501 /CS5503 Data Output Mode Selection

Connector P5 (see figure 2) allows jumper selection of any one of the three data output modes. These modes are:

- 1) SSC (Synchronous Self-Clocking);
  - 2) SEC (Synchronous External Clocking);
  - 3) AC (Asynchronous Communication).
- (AC mode is available only in the CS5501)

### SSC (Synchronous Self-Clocking) Mode

The SSC mode is designed for interface to those microcontrollers which allow external clocking of their serial inputs. The SSC mode also allows easy connection to serial-to-parallel conversion circuitry.

In the SSC mode serial data and serial clock are output from the CS5501/CS5503 whenever the  $\overline{CS}$  line is activated. As illustrated in figure 2, all of the signals are available at connector P10. If the  $\overline{CS}$  signal is to be controlled remotely the jumper on P9 should be placed in the NC (No Connection) position. This removes the Decimation Counter output from controlling the  $\overline{CS}$  line.

### Data Output Interface: Parallel Port (for CS5501 evaluation only).

Whenever the CS5501 is operated in the SSC mode the 16-bit output data is clocked into two 8-bit shift registers. The registers have three-state parallel outputs which are available at P7 (see figure 3). A flip-flop (U8A) is used to signal the remote reading device whenever the registers are updated. The  $\overline{PDR}$  (Parallel Data Ready) signal from the flip-flop is available on P7. The Q-bar output from the flip-flop locks out any further updates to the registers until their data is read and a DACK (Data ACKnowledge) signal is received from the remote device.

Activation of the  $\overline{CS}$  line determines the rate at which the CS5501 will attempt to update the output shift registers. Data will be shifted into the

registers only if a DACK signal has occurred since the last update.

The  $\overline{CS}$  line can be controlled remotely at P10 or by the output of the Decimation Counter. If  $\overline{CS}$  is controlled remotely, the Decimation divide jumper on P4 should be placed in the "0" position. This insures that the  $\overline{DCS}$  signal will occur at the same rate  $\overline{CS}$  is activated. The positive going edge of  $\overline{DCS}$  toggles the U8A flip-flop which signals an update to the parallel port.

The parallel registers are set up to be read in 16-bit parallel fashion but can be configured to be read separately as two 8-bit bytes on an 8-bit bus. To configure the board for byte-wide reads, the byte-wide jumpers must be soldered in place. In addition, for proper "one byte at a time" address selection, a connection on the circuit board needs to be opened and a jumper wire soldered in the proper place to determine which register is to be read when A0 is a "1" and vice versa. See figure 3 for schematic details. The evaluation board component layout diagram, figure 7, indicates the location of the byte-wide jumpers and A0 address selection jumpers.

After data is read from the registers a DACK (Data Acknowledge) signal is required from the off-board controller to reset flip-flop U8A. This enables the registers to accept data input once again.

The DRB and CSB signals on connector P10 should be used to monitor and control the CS5501 output to the serial to parallel conversion registers. Be aware that an arbitrarily timed DACK signal may cause the output data registers to be enabled in the middle of an output word if the  $\overline{CS}$  signal to the CS5501 is not properly sequenced. This will result in incorrect data in the output registers.

If the Decimation Counter is used to control the output of the CS5501 (Jumper on P9 in the DC position), the CSB signal on P10 can be



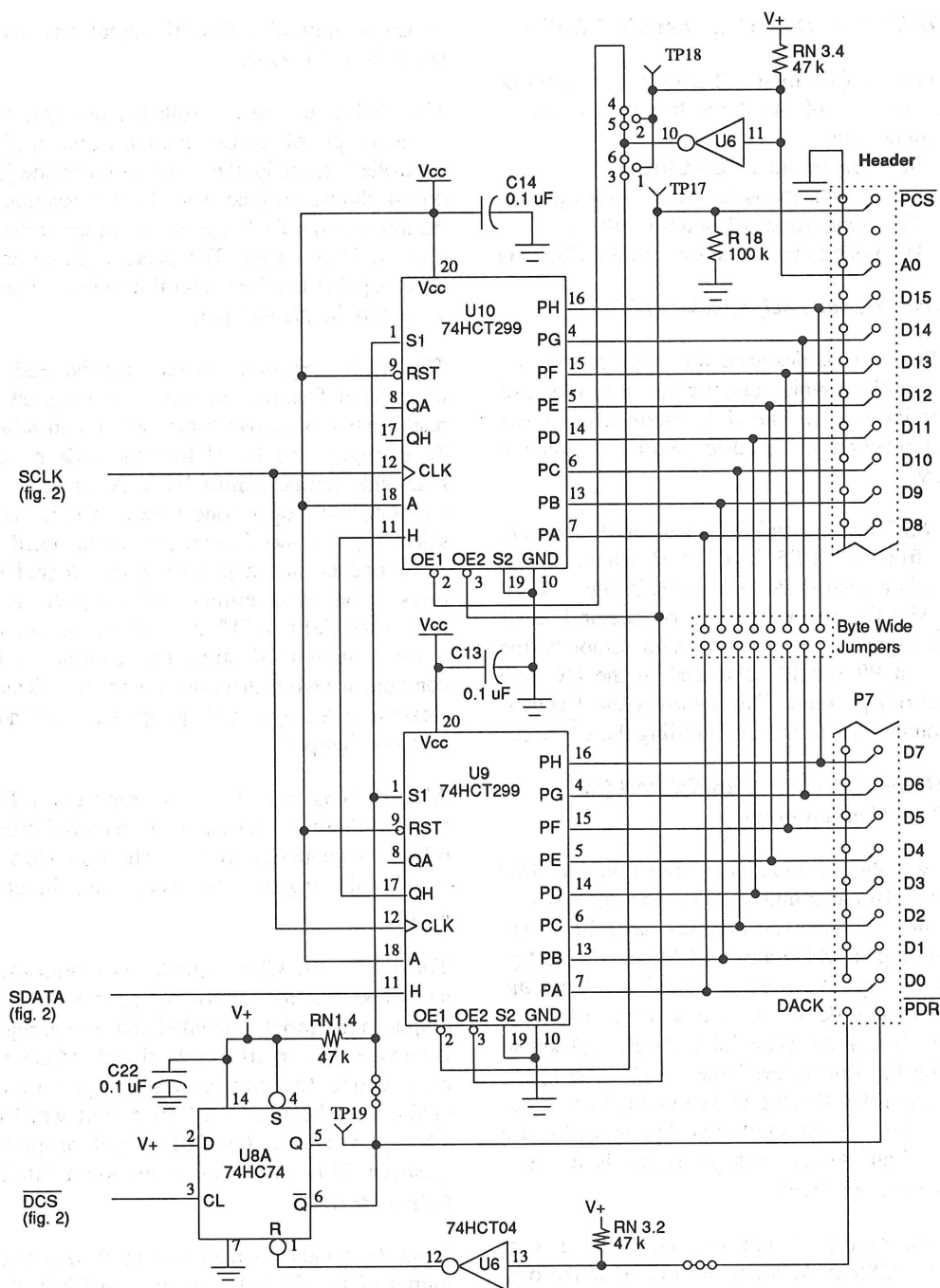


Figure 3. 16-Bit Parallel Port

monitored to signal when data into the output registers is complete (DCS returns high). The DACK signal is not needed in this mode and the lockout signal to the S1 inputs of registers U9 and U10 may be disabled by removing the connection on the circuit board. A place is provided on the board for this purpose. A pull-up resistor is provided on the S1 inputs of the registers if the connection is opened.

### SEC (Synchronous External Clocking) Mode

The SEC mode enables the CS5501/CS5503 to be directly interfaced to microcontrollers which output a clock signal to synchronously input serial data to an input port. The CS5501/CS5503 will output its serial data at the rate determined by the clock from the microcontroller.

Connector P10 allows a microcontroller access to the CS5501/CS5503 signal lines which are necessary to operate in the SEC mode.

The CSB (chip select bar  $\overline{CS}$ ) signal allows the microcontroller to control when the CS5501/CS5503 is to output data. The  $\overline{DRB}$  (data

ready bar) signal on P10 indicates to the microcontroller when data from the CS5501/CS5503 is available. Clock from the microcontroller is input into SCI (serial clock input) and data output from the CS5501/CS5503 is presented to the SD (serial data) pin of the P10 connector. Note that the jumpers on connectors P9 and P11 must be in the NC (no connection) position to allow the microcontroller full control over the signals on P10.

### AC (Asynchronous Communication) Mode (for CS5501 evaluation only)

The AC mode enables the CS5501 to output data in a UART-compatible format. Data is output as two characters consisting of one start bit, eight data bits, and two stop bits each.

The output data rate can be set by a clock input to the SCI input at connector P10 (see figure 2). The jumper on P11 must be in the NC position. Alternatively an output data bit rate can be selected as a sub-multiple of the external CLKIN signal to the board or as a sub-multiple of the on-board 4.9152 MHz oscillator. Counter IC U2 divides its input by  $2^n$  where  $n = 8, 9, \dots, 12$ . One of these outputs can be jumper selected at connector P3 (see figure 1). For example, if the 4.9152 MHz oscillator is selected as the input to IC U2 then a 1200 baud rate clock can be selected with the jumper at  $n = 12$ . Table 3 indicates the baud rates available at connector P3 when the 4.9152 MHz oscillator is used. If the on-board baud clock is to be used, the jumper on connector P11 should be in the BC (Baud Clock) position.

### Data Output Interface: RS-232 (for CS5501 evaluation only).

The RS232 port is depicted in figure 4. Sub-D connector P6 along with interface IC U11 provides the necessary circuitry to connect the CS5501 to an RS-232 input of a computer. For proper operation the AC (Asynchronous Communication) data output mode must be selected.

**Table 3. On-Board Baud Rate Generator**

Baud Rate Clock Divider ( $CLK/2^n$ ) with INT CLK on P1 selected.  
CLK = 4.9152 MHz

P-3	Baud Rate CLK Divider
8	19.2 kHz
9	9.6 kHz
10	4.8 kHz
11	2.4 kHz
12	1.2 kHz

On-Board Baud Rate Clock Input to CS5501/CS5503. SCLK Input.

P-11	SCLK Input to CS5501/CS5503
NC	No Connection
BC	Baud Clock

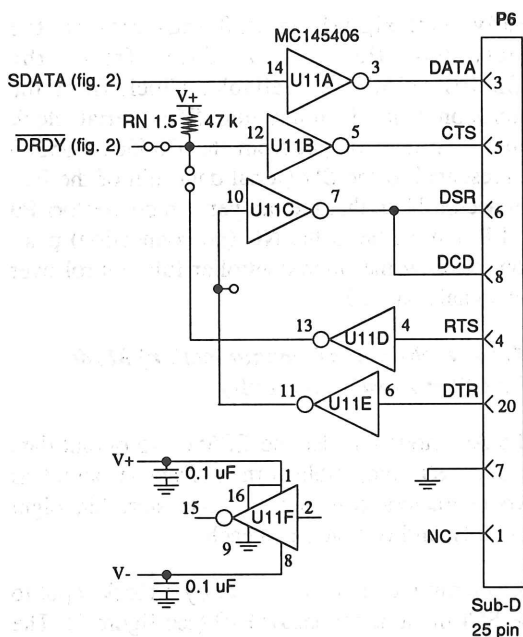


Figure 4. RS-232 Port

In addition, an appropriate baud clock needs to be input to the CS5501. See AC (Asynchronous Communication) mode mentioned earlier for an explanation of the baud rate clock generator and the data format of the output data in the AC mode.

The  $\overline{\text{DRDY}}$  output from the CS5501 signals the CTS (Clear To Send) line of the RS-232 interface when data is available. The Decimation Counter can be used to determine how frequently output data is to be transmitted.

The RS-232 interface on the evaluation card is functionally adequate but it is not compliant with the EIA RS-232 standard. When the MC145406 RS-232 receiver/driver chip is operated off of  $\pm 5$  volt supplies rather than  $\pm 6$  volts (see the MC145406 data sheet for details) its driver output swing is reduced below the EIA specified limits. In practical applications this signal swing limitation only reduces the length of cable the circuit is capable of driving.

## DECIMATION COUNTER

Each time a data word is available for output from the CS5501/CS5503, the  $\overline{\text{DRDY}}$  line goes low, provided the output port was previously emptied. If the  $\overline{\text{DRDY}}$  line is directly tied to the  $\overline{\text{CS}}$  input of the CS5501/CS5503, the converter will output data every time a data word is presented to the output pin. In some applications it is desirable to reduce the output word rate. The

Table 4. Decimation Counter Control

Decimation Counter Accumulates  $2^{n+1}$   $\overline{\text{DRDY}}$  Pulses Before  $\overline{\text{CS}}$  is Enabled.

P-4	$2^{n+1}$
0	2
1	4
2	8
3	16
4	32
5	64
6	128
7	256
8	512
9	1024
10	2048
11	4096

P-9	DC Output to $\overline{\text{CS}}$
NC	No Connection
DC	Decimation Counter

rate can be reduced by lowering the rate at which the  $\overline{\text{CS}}$  line to the chip is enabled. The CDB5501/CDB5503 evaluation board uses a counter, IC U3 for this purpose. It is known as a decimation counter (see figure 2). The outputs of the counter are available at connector P4. The counter accumulates  $2^{n+1}$  counts ( $n = 0, 2, \dots, 11$ ) at which time the selected output enables the  $\overline{\text{CS}}$  input to the CS5501/CS5503 (if the jumper in P9 is in the DC, Decimation Counter, position). The

Switch	ON	OFF
SW1-1	SC1 = 0	SC1 = 1
SW1-2	SC2 = 0	SC2 = 1
SW1-3	UNIPOLAR	BIPOLAR
SW1-4	SLEEP	AWAKE

Table 5. DIP Switch Selections

CAL	SC1	SC2	Cal Type	ZS Cal	FS Cal	Sequence
	0	0	Self-Cal	AGND	VREF	One Step
	1	1	System Offset & System Gain	AIN	-	1st Step
	0	1		-	AIN	2nd Step
	1	0	System Offset	AIN	VREF	One Step

Table 6. Calibration Mode Table

"D" input to flip-flop U8B is enabled to a "1" at the same time  $\overline{CS}$  goes low. When  $\overline{DRDY}$  returns high flip-flop U8B is toggled and resets the counter back to zero which terminates the  $\overline{CS}$  enable. The counter then accumulates counts until the selected output activates  $\overline{CS}$  low once again.

### DIP Switch Selections/Calibration Initiation

Several control pins of the CS5501/CS5503 can be level activated by DIP switch selection, or by microcontroller at P8, as shown in figure 5. DIP switch SW1 selections are depicted in tables 5 and 6. The CAL pushbutton is used to initiate a calibration cycle in accordance with DIP switch positions 1 and 2. The CAL pushbutton should be

activated any time power is first applied to the board or any time the conversion mode (BP/ $\overline{UP}$ ) is changed on the DIP switch. Remote control of the CAL signal is available on connector P8. Connector P8 also allows access to the DIP switch functions by a microcomputer/microcontroller. The DIP switches should be placed in the off position if off-board control of the signals on connector P8 is implemented.

### Voltage Reference

The evaluation board includes a 2.5 volt reference. Potentiometer R9 can be used to trim the reference output to a precise value.

### Analog Input Range: Unipolar Mode

The value of the reference voltage sets the analog input signal range. In unipolar mode the analog input range extends from AGND to VREF. If the analog input goes above VREF the converter will output all "1's". If the input goes below AGND, the CS5501/CS5503 will output all "0's".

### Analog Input Range: Bipolar Mode

The analog signal input range in the bipolar mode is set by the reference to be from +VREF to -VREF. If the input signal goes above +VREF, the CS5501/CS5503 will output all "1's". Input signals below -VREF cause the output data to be all "0's".

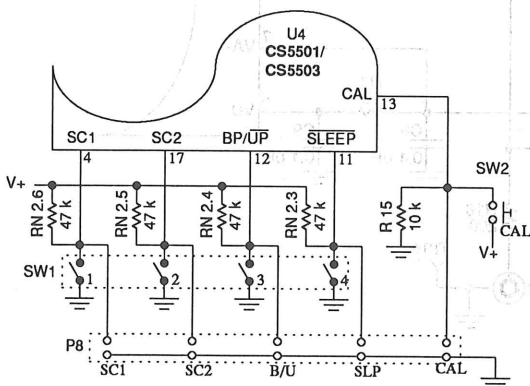
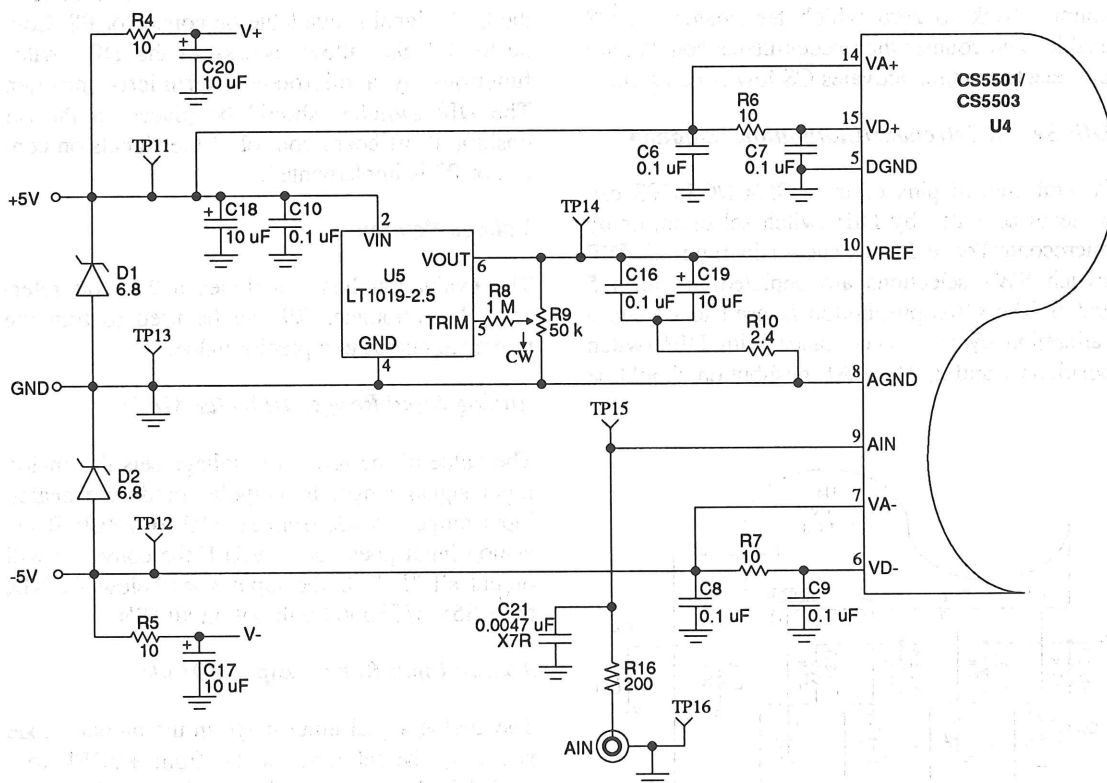


Figure 5. DIP Switch / Header Control Pin Selection

### Analog Input: Overrange Precautions

In normal operation the value of the reference voltage determines the range of the analog input signal. Under abnormal conditions the analog signal can extend to be equal to the VA+ and VA-supply voltages. In the event the signal exceeds these supply voltages the input current should be

limited to  $\pm 10$  mA as the analog input of the chip is internally diode clamped to both supplies. Excess current into the pin can damage the device. On the evaluation board, resistor R16 (see figure 6) does provide some current limiting in the event of an overrange signal which exceeds the supply voltage.



**Figure 6. Voltage Reference / Analog Input**

## Oscilloscope Monitoring of SDATA

The output data from either the CS5501 or the CS5503 can be observed on a dual trace oscilloscope with the following hook-up. Set the evaluation board to operate in the SSC mode. Connect scope probes to TP9 (SCLK) and TP10 (SDATA). Use a third probe connected to TP8 (DRDY) to provide the external trigger input to the scope (use falling edge of DRDY to trigger). With proper horizontal sweep, the SDATA output bits from the A/D converter can be observed. Note that if the input voltage to the CS5501 is adjusted to a mid-code value, the converter will remain stable on the same output code. This illustrates the low noise level of the CS5501. The CS5503 will exhibit a few LSB's of noise in its observed output in agreement with its noise specifications.

## Evaluation Board Component Layout and Design Considerations

Figure 7 is a reproduction of the silkscreen component placement of the PC board.

The evaluation board includes design features to insure proper performance from the A/D converter chip. Separate analog and digital ground planes have been used on the board to insure good noise immunity to digital system noise.

Decoupling networks (R6, C7, and R7, C9 in figure 6) have been used to eliminate the possibility of noise on the power supplies on the digital section from affecting the analog part of the A/D converter chip.

The RC network (R10, C16 and C19) on the output of the LT1019-2.5 reference may not be needed in all applications. It has been included to insure the best noise performance from the reference.

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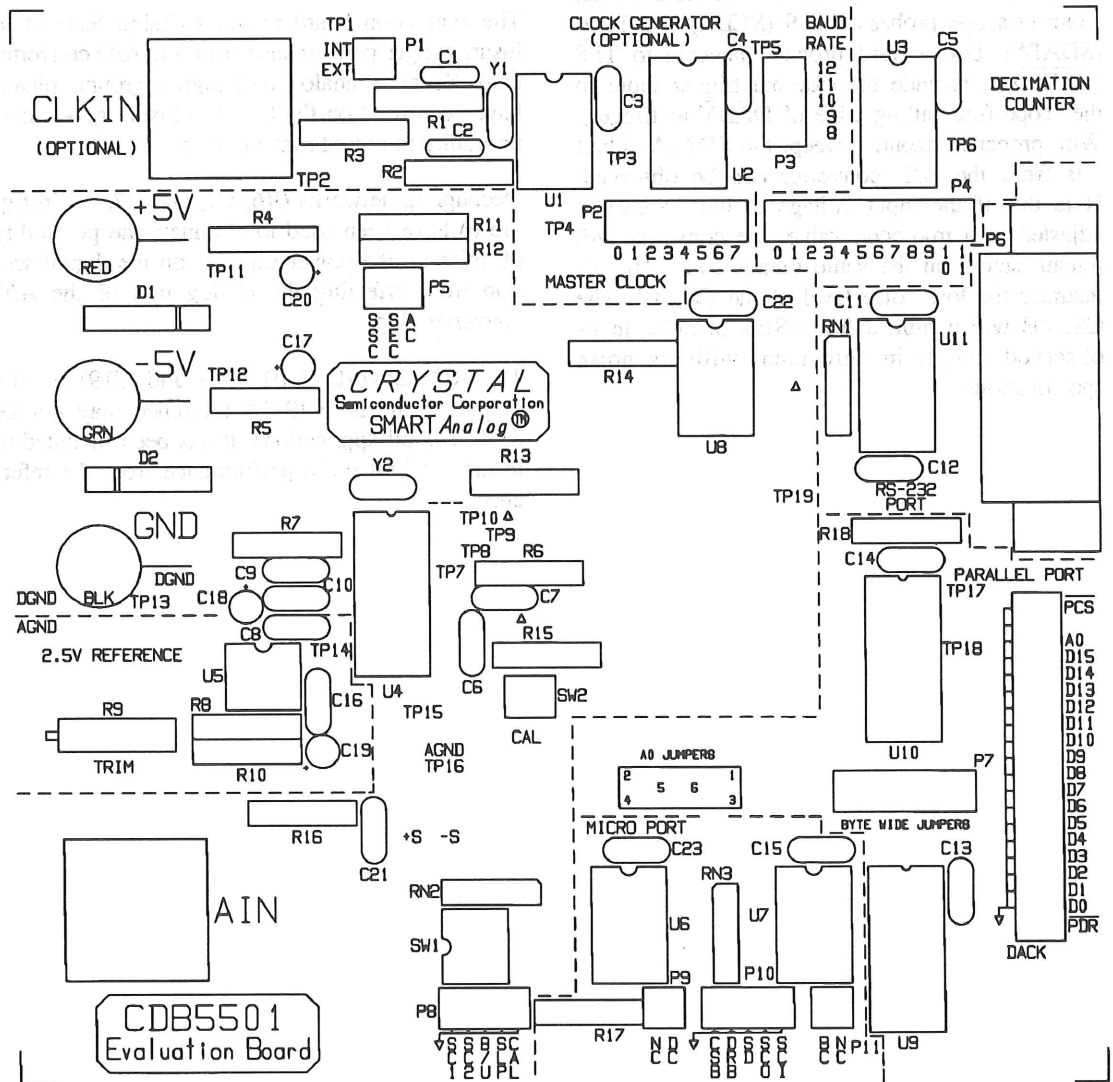


Figure 7. CDB5501/CDB5503 Component Layout



## Very Low Power, 16-Bit and 20-Bit A/D Converters

### Features

- Very Low Power Consumption  
Single supply +5V operation: 1.5 mW  
Dual supply  $\pm 5V$  operation: 3.0 mW
- Offers superior performance to VFCs and multi-slope integrating ADCs
- Differential Inputs  
Single Channel and Four-Channel pseudo-differential versions
- On Chip Self-Calibration Circuitry
- Linearity Error:  $\pm 0.0015\%$  FS
- Output update rates up to 100/second
- Flexible Serial Port
- Pin-Selectable Unipolar/Bipolar Ranges

### General Description

The CS5505/6/7/8 are a family of low power CMOS A/D converters which are ideal for measuring low-frequency signals representing physical, chemical, and biological processes.

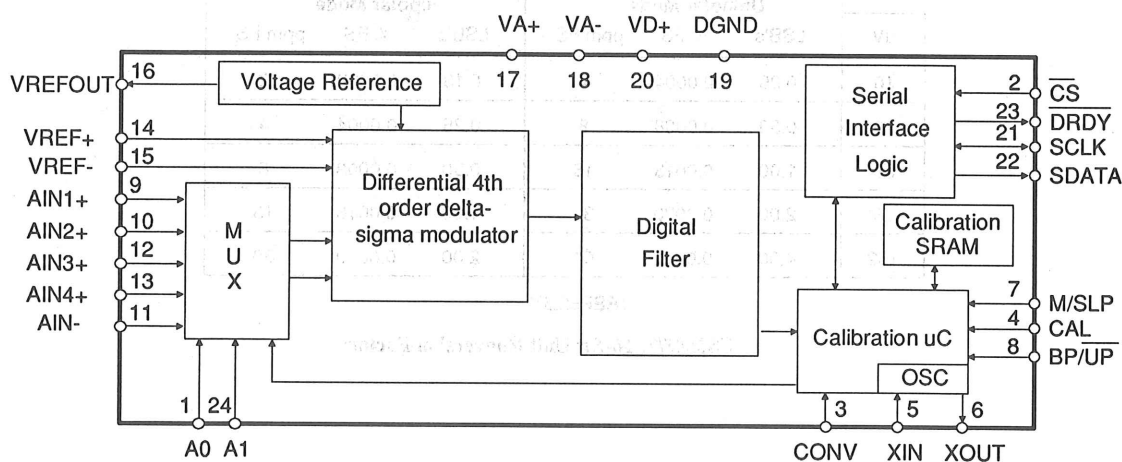
The CS5507/8 have single-channel differential analog and reference inputs while the CS5505/6 have four pseudo-differential analog input channels. The CS5505/7 have a 16-bit output word. The CS5506/8 have a 20-bit output word. The CS5505/7 sample upon command up to 100 output updates per second. The CS5506/8 sample up to 60 updates per second.

The on chip digital filter offers superior line rejection at 50 and 60Hz when the device is operated from a 32.768 kHz clock (output word rate=20 Hz.).

The CS5505/6/7/8 include on-chip self-calibration circuitry which can be initiated at any time or temperature to insure minimum offset and full-scale errors.

The CS5505/6/7/8 serial port offers two general-purpose modes for the direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers.

**Ordering Information:** Page 3-320



**ANALOG CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}, V_{D+} = 5V$ ;  $V_{A-} = -5V$ ;  $V_{REF+} = 2.5V$ (external);  $V_{REF-} = 0V$ ;  $f_{CLK} = 32.768kHz$ ; Bipolar Mode;  $R_{source} = 2k\Omega$  with a  $10nF$  to AGND at AIN (see Note 1); Analog input channel AIN1+ ; AIN- = AGND; unless otherwise specified.)

Parameter *	CS5505/7-A			CS5505/7-S			Units
	Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range	-40 to +85			-55 to +125			°C
<b>Accuracy</b>							
Linearity Error	-	0.0015	0.003	-	0.0015	0.003	±%FS
Differential Nonlinearity	-	±0.25	±0.5	-	±0.25	±0.5	LSB <sub>16</sub>
Full Scale Error (Note 2)	-	±0.25	±2	-	±0.5	±2	LSB <sub>16</sub>
Full Scale Drift (Note 3)	-	±0.5	-	-	±2	-	LSB <sub>16</sub>
Unipolar Offset (Note 2)	-	±0.5	±2	-	±1	±4	LSB <sub>16</sub>
Unipolar Offset Drift (Note 3)	-	±0.5	-	-	±1	-	LSB <sub>16</sub>
Bipolar Offset (Note 2)	-	±0.25	±1	-	±0.5	±2	LSB <sub>16</sub>
Bipolar Offset Drift (Note 3)	-	±0.25	-	-	±0.5	-	LSB <sub>16</sub>
Noise (Referred to Output)	-	0.12	-	-	0.12	-	LSB <sub>rms</sub> 16

- Notes: 1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the CS5505/6/7/8's source impedance requirements. For more information refer to the text section *Analog Input Impedance Considerations*.
2. Applies after calibration at the temperature of interest.
3. Total drift over the specified temperature range since calibration at power-up at 25°C. Recalibration at any temperature will remove these errors.

uV	Unipolar Mode			Bipolar Mode		
	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
10	0.26	0.0004	4	0.13	0.0002	2
19	0.50	0.0008	8	0.26	0.0004	4
38	1.00	0.0015	15	0.50	0.0008	8
76	2.00	0.0030	30	1.00	0.0015	15
152	4.00	0.0061	61	2.00	0.0030	30

**VREF=2.5V**

**CS5505/7; 16-Bit Unit Conversion Factors**

\* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

**ANALOG CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}, V_{D+} = 5V$ ;  $V_{A-} = -5V$ ;  $V_{REF+} = 2.5V$  (external);  $V_{REF-} = 0V$ ;  $f_{CLK} = 32.768kHz$ ; Bipolar Mode;  $R_{SOURCE} = 2k\Omega$  with a  $10nF$  to AGND at AIN (see Note 1); Analog input channel AIN1+; AIN- = AGND; unless otherwise specified.)

Parameter		CS5506/8-B			CS5506/8-S			Units
		Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range		-40 to +85			-55 to +125			°C
Accuracy								
Linearity Error		-	0.0007	0.0015	-	0.0015	0.003	±%FS
Differential Nonlinearity (No Missing Codes)	(Note 4)	18	19	-	18	19	-	Bits
Full Scale Error	(Note 2)	-	±4	±32	-	±8	±32	LSB <sub>20</sub>
Full Scale Drift	(Note 3)	-	±4	-	-	±8	-	LSB <sub>20</sub>
Unipolar Offset	(Note 2)	-	±8	±32	-	±16	±64	LSB <sub>20</sub>
Unipolar Offset Drift	(Note 3)	-	±8	-	-	±16	-	LSB <sub>20</sub>
Bipolar Offset	(Note 2)	-	±4	±16	-	±8	±32	LSB <sub>20</sub>
Bipolar Offset Drift	(Note 3)	-	±4	-	-	±8	-	LSB <sub>20</sub>
Noise (Referred to Output)		-	2	-	-	2	-	LSB <sub>rms</sub> 20

Notes: 4. The delta-sigma modulator in the CS5505/6/7/8 is monotonic. However, some missing codes and wide codes are possible due to accumulator truncation error in the digital filter. Contribution of accumulator truncation error to missing codes is a function of the gain slope calibration factor. Calibrations will normally achieve no missing codes to 19 bits, but it is statistically possible for a calibration to yield a few missing codes at 19 bits. Therefore, no missing code performance is guaranteed to only 18 bits.

uV	Unipolar Mode			Bipolar Mode		
	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
0.596	0.25	0.0000238	0.24	0.13	0.0000119	0.12
1.192	0.50	0.0000477	0.47	0.26	0.0000238	0.24
2.384	1.00	0.0000954	0.95	0.50	0.0000477	0.47
4.768	2.00	0.0001907	1.91	1.00	0.0000954	0.95
9.537	4.00	0.0003814	3.81	2.00	0.0001907	1.91

VREF=2.5V

CS5506/8; 20-Bit Unit Conversion Factors

**ANALOG CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}, V_{D+} = 5V$ ;  $V_{A-} = -5V$ ;  $V_{REF+} = 2.5V$  (external);  $V_{REF-} = 0V$ ;  $f_{CLK} = 32.768kHz$ ; Bipolar Mode;  $R_{source} = 2k\Omega$  with a  $10nF$  to AGND at AIN (see Note 1); Analog input channel AIN1+; AIN- = AGND; unless otherwise specified.)

Parameter	CS5505/7-A CS5506/8-B			CS5505/6/7/8-S			Units
	Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range	-40 to +85			-55 to +125			°C
<b>Analog Input</b>							
Analog Input Range: Unipolar (VAIN+)-(VAIN-) (Note 5) Bipolar	0 to +2.5 ±2.5			0 to +2.5 ±2.5			Volts Volts
Common Mode Rejection: dc 50,60 Hz (Note 6)	- 120	105 -	- -	- 120	105 -	- -	dB dB
Off Channel Isolation	-	120	-	-	120	-	dB
Input Capacitance	-	15	-	-	15	-	pF
DC Bias Current (Note 1)	-	5	-	-	5	-	nA
<b>Voltage Reference (Output)</b>							
VREFOUT Voltage	-	(VA+)-2.5	-	-	(VA+)-2.5	-	Volts
VREFOUT Voltage Tolerance	-	-	4.0	-	-	4.0	%
VREFOUT Voltage Temperature Coefficient	-	60	-	-	TBD	-	ppm/°C
VREFOUT Line Regulation	-	1.5	-	-	1.5	-	mV/Volt
VREFOUT Output Voltage Noise 0.1 to 10 Hz	-	50	-	-	50	-	μVp-p
VREFOUT: Source Current Sink Current	- -	- -	3 50	- -	- -	3 50	μA μA
<b>Power Supplies</b>							
DC Power Supply Currents: ITotal IAnalog IDigital	- - -	300 260 40	450 - -	- - -	300 260 40	450 - -	μA μA μA
Power Dissipation: (Note 7) SLEEP inactive SLEEP active	- -	3.0 5	4.5 10	- -	3.0 10	4.5 25	mW μW
Power Supply Rejection: Positive Supplies Negative Supplies	- -	80 80	- -	- -	80 80	- -	dB dB

Notes: 5. Common mode voltage may be at any value as long as AIN+ and AIN- remain within the VA+ and VA- supply voltages.

6. XIN = 32.768 kHz. Guaranteed by design and / or characterization.

7. All outputs unloaded. All inputs CMOS levels. SLEEP mode controlled by M/SLP pin.  
SLEEP active = M/SLP pin at (VD+)/2 input level.

## DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Modulator Sampling Frequency	$f_s$	$f_{clk}/2$	Hz
Output Update Rate (CONV = 1)	$f_{out}$	$f_{clk}/1622$	Hz
Filter Corner Frequency	$f_{-3dB}$	$f_{clk}/1928$	Hz
Settling Time to 1/2 LSB (FS Step)	$t_s$	$1/f_{out}$	s

## DIGITAL CHARACTERISTICS

( $T_A = T_{min}$  to  $T_{max}$ ;  $V_{A+}$ ,  $V_{D+} = 5V \pm 10\%$ ;  $V_{A-} = -5V \pm 10\%$ ;  $DGND = 0$ ). All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention Power Supply Voltage ( $V_{D+}$ and $V_{A+}$ )	$V_{MR}$	2.0	-	-	V
High-Level Input Voltage: XIN M/SLP All Pins Except XIN and M/SLP	$V_{IH}$	3.5	-	-	V
	$V_{IH}$	0.9VD+	-	-	V
	$V_{IH}$	2.0	-	-	V
Low-Level Input Voltage XIN M/SLP All Pins Except XIN and M/SLP	$V_{IL}$	-	-	1.5	V
	$V_{IL}$	-	-	0.1VD+	V
	$V_{IL}$	-	-	0.8	V
M/SLP SLEEP Active Threshold (Note 8)	$V_{SLP}$	0.45VD+	0.5VD+	0.55VD+	V
High-Level Output Voltage (Note 9)	$V_{OH}$	(VD+)-1.0	-	-	V
Low Level Output Voltage $I_{out} = 1.6mA$	$V_{OL}$	-	-	0.4	V
Input Leakage Current	$I_{in}$	-	1	10	$\mu A$
3-State Leakage Current	$I_{OZ}$	-	-	$\pm 10$	$\mu A$
Digital Output Pin Capacitance	$C_{out}$	-	9	-	pF

Notes: 8. Under normal operation this pin should be tied to  $V_{D+}$  or  $DGND$ . Anytime the voltage on the M/SLP pin enters the SLEEP active threshold range the device will enter the power down condition. Returning to the active state requires elapse of the power-on reset period, the oscillator to start-up, and elapse of the wake-up period.

9.  $I_{out} = -100 \mu A$ . This guarantees the ability to drive one TTL load. ( $V_{OH} = 2.4V @ I_{out} = -40 \mu A$ ).

## SWITCHING CHARACTERISTICS (TA = T<sub>min</sub> to T<sub>max</sub>; VA+, VD+ = 5V ± 10%; VA- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; CL = 50 pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock frequency:	Internal Oscillator: -A,B	30.0	32.768	53.0	kHz
	-S	30.0	32.768	34.0	kHz
	External Clock: CS5505/7	f <sub>clk</sub> 30	-	163	kHz
	CS5506/8	f <sub>clk</sub> 30	-	100	kHz
Master Clock Duty Cycle		40	-	60	%
Rise Times: (Note 10)	Any Digital Input	t <sub>rise</sub>	-	1.0	μs
	Any Digital Output		50	-	ns
Fall Times: (Note 10)	Any Digital Input	t <sub>fall</sub>	-	1.0	μs
	Any Digital Output		20	-	ns
<b>Start-Up</b>					
Power-On Reset Period (Note 11)	t <sub>res</sub>	-	10	-	ms
Oscillator Start-up Time (Note 12) XTAL=32.768 kHz	t <sub>osu</sub>	-	500	-	ms
Wake-up Period (Note 13)	t <sub>wup</sub>	-	1800	-	f <sub>clk</sub>
<b>Calibration</b>					
CONV Pulse Width (CAL=1) (Note 14)	t <sub>ccw</sub>	100	-	-	ns
CONV and CAL High to Start of Calibration	t <sub>scl</sub>	-	-	2/f <sub>clk</sub> +50	ns
Start of Calibration to End of Calibration	t <sub>cal</sub>	-	3246	-	f <sub>clk</sub>
<b>Conversion</b>					
Set Up Time A0, A1 to CONV High	t <sub>sac</sub>	50	-	-	ns
Hold Time A0, A1 after CONV High	t <sub>hca</sub>	100	-	-	ns
CONV Pulse Width	t <sub>cpw</sub>	100	-	-	ns
CONV High to Start of Conversion	t <sub>scn</sub>	-	-	2/f <sub>clk</sub> +50	ns
Set Up Time BP/UP stable prior to DRDY falling	t <sub>bus</sub>	82	-	-	f <sub>clk</sub>
Hold Time BP/UP stable after DRDY falls	t <sub>buh</sub>	0	-	-	ns
Start of Conversion to End of Conversion (Note 15)	t <sub>con</sub>	-	1624	-	f <sub>clk</sub>

Notes: 10. Specified using 10% and 90% points on waveform of interest.

11. An internal power-on-reset is activated whenever power is applied to the device, or when coming out of a SLEEP state.

12. Oscillator start-up time varies with the crystal parameters. This specification does not apply when using an external clock source.

13. The wake-up period begins once the oscillator starts; or when using an external f<sub>clk</sub>, after the power-on reset time elapses.

14. Calibration can also be initiated by pulsing CAL high while CONV=1.

15. Conversion time will be 1622 f<sub>clk</sub>'s if CONV remains high continuously.

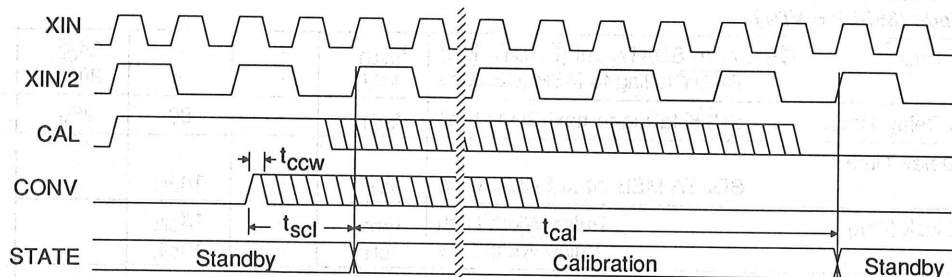


Figure 1. Calibration Timing (Not to Scale)

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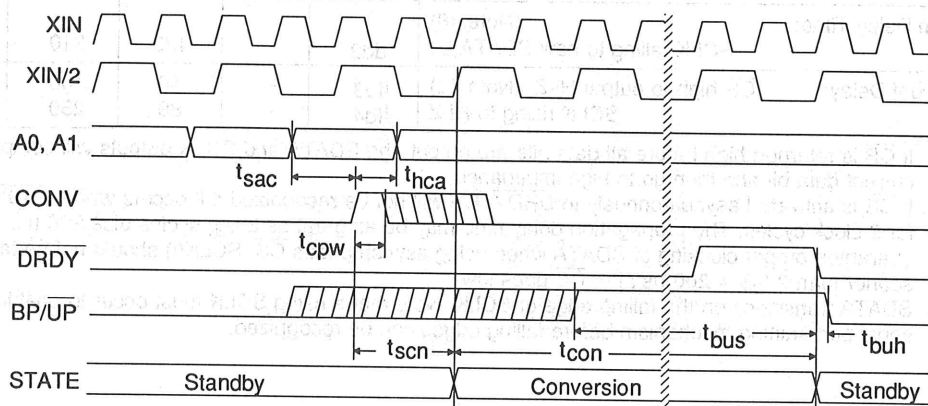


Figure 2. Conversion Timing (Not to Scale)



# SWITCHING CHARACTERISTICS (continued)

Parameter	Symbol	Min	Typ	Max	Units
<b>SSC Mode (M/SLP = VD+)</b>					
Access Time: $\overline{CS}$ Low to SDATA out ( $\overline{DRDY}$ = low) $\overline{DRDY}$ falling to MSB ( $\overline{CS}$ =low)	$t_{csd1}$	-	-	$2/f_{clk}$	ns
	$t_{dfd}$	-	-	$2/f_{clk}$	ns
SDATA Delay Time: SCLK falling to next SDATA bit	$t_{dd1}$	-	80	250	ns
SCLK Delay Time: SDATA MSB bit to SCLK rising	$t_{cd1}$	-	$1/f_{clk}$	-	ns
Serial Clock (Out) Pulse Width High Pulse Width Low	$t_{ph1}$	-	$1/f_{clk}$	-	ns
	$t_{pl1}$	-	$1/f_{clk}$	-	ns
Output Float Delay: $\overline{CS}$ high to output Hi-Z (Note 16) SCLK falling to Hi-Z	$t_{fd1}$	-	-	$2/f_{clk}$	ns
	$t_{fd2}$	-	$1/f_{clk}$	-	ns
<b>SEC Mode (M/SLP = DGND)</b>					
Serial Clock (In)	$f_{sclk}$	0	-	2.5	MHz
Serial Clock (In) Pulse Width High Pulse Width Low	$t_{ph2}$	200	-	-	ns
	$t_{pl2}$	200	-	-	ns
Access Time: $\overline{CS}$ Low to data valid (Note 17)	$t_{csd2}$	-	60	200	ns
Maximum Delay Time: (Note 18) SCLK falling to new SDATA bit	$t_{dd2}$	-	130	310	ns
Output Float Delay: $\overline{CS}$ high to output Hi-Z (Note 16) SCLK rising to Hi-Z	$t_{fd3}$	-	40	150	ns
	$t_{fd4}$	-	80	250	ns

- Notes: 16. If  $\overline{CS}$  is returned high before all data bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.
17. If  $\overline{CS}$  is activated asynchronously to  $\overline{DRDY}$ ,  $\overline{CS}$  will not be recognized if it occurs when  $\overline{DRDY}$  is high for 2 clock cycles. The propagation delay time may be as great as  $2 f_{clk}$  cycles plus 200 ns. To guarantee proper clocking of SDATA when using asynchronous  $\overline{CS}$ , SCLK(i) should not be taken high sooner than  $2 f_{clk} + 200$  ns after  $\overline{CS}$  goes low.
18. SDATA transitions on the falling edge of SCLK. Note that a rising SCLK must occur to enable the serial port shifting mechanism before falling edges can be recognized.

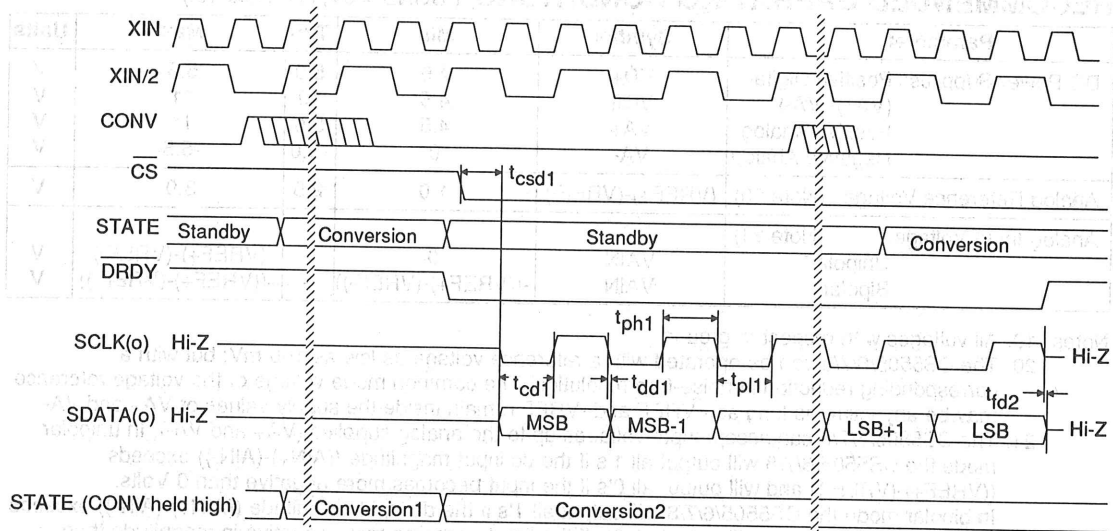


Figure 3. Timing Relationships; SSC Mode (Not to Scale)

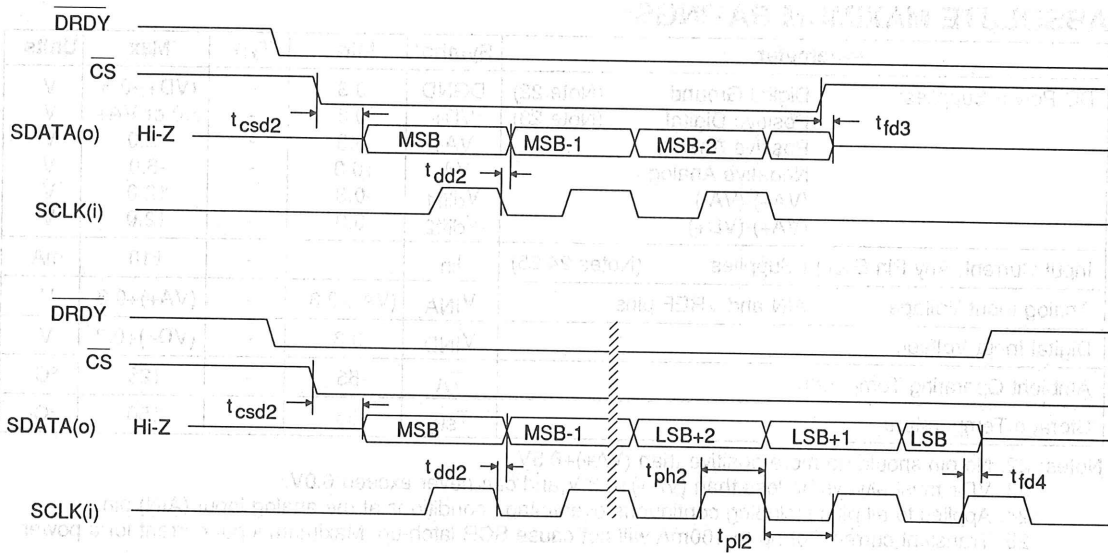


Figure 4. Timing Relationships; SEC Mode (Not to Scale)

**RECOMMENDED OPERATING CONDITIONS** ( DGND = 0V, see Note 19.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital (VA+)-(VA-)	VD+	4.5	5.0	5.5	V
	Vdiff	4.5	10	11	V
	VA+	4.5	5.0	11	V
	VA-	0	-5.0	-5.5	V
Analog Reference Voltage (Note 20)	(VREF+)-(VREF-)	1.0	2.5	3.0	V
Analog Input Voltage: (Note 21)	VAIN	0	-	(VREF+)-(VREF-)	V
	VAIN	-((VREF+)-(VREF-))	-	+((VREF+)-(VREF-))	V

Notes: 19. All voltages with respect to ground.

20. The CS5505/6/7/8 can be operated with a reference voltage as low as 100 mV; but with a corresponding reduction in noise-free resolution. The common mode voltage of the voltage reference may be any value as long as +VREF and -VREF remain inside the supply values of VA+ and VA-.

21. The CS5505/6/7/8 can accept input voltages up to the analog supplies (VA+ and VA-). In unipolar mode the CS5505/6/7/8 will output all 1's if the dc input magnitude ((AIN+)-(AIN-)) exceeds ((VREF+)-(VREF-)) and will output all 0's if the input becomes more negative than 0 Volts. In bipolar mode the CS5505/6/7/8 will output all 1's if the dc input magnitude ((AIN+)-(AIN-)) exceeds ((VREF+)-(VREF-)) and will output all 0's if the input becomes more negative in magnitude than -((VREF+)-(VREF-)).

**ABSOLUTE MAXIMUM RATINGS\***

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:	Digital Ground (Note 22)	DGND	-0.3	-	(VD+)-0.3 V
	Positive Digital (Note 23)	VD+	-0.3	-	6.0 or VA+ V
	Positive Analog	VA+	-0.3	-	12.0 V
	Negative Analog	VA-	+0.3	-	-6.0 V
	(VA+)-(VA-)	Vdiff1	-0.3	-	12.0 V
	(VA+)-(VD+)	Vdiff2	-0.3	-	12.0 V
Input Current, Any Pin Except Supplies (Notes 24,25)	Iin	-	-	±10	mA
Analog Input Voltage AIN and VREF pins	VINA	(VA-)-0.3	-	(VA+)+0.3	V
Digital Input Voltage	VIND	-0.3	-	(VD+)+0.3	V
Ambient Operating Temperature	TA	-55	-	125	°C
Storage Temperature	Tstg	-65	-	150	°C

Notes: 22. No pin should go more positive than (VA+)+0.3V.

23. VD+ must always be less than (VA+)+0.3 V, and can never exceed 6.0V.

24. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.

25. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

\* WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

### **GENERAL DESCRIPTION**

The CS5505/6/7/8 are very low power monolithic CMOS A/D converters designed specifically for measurement of dc signals. The CS5505/7 are 16-bit converters (a four channel and a single channel version). The CS5506/8 are 20-bit converters (a four channel and a single channel version). Each of the devices includes a delta-sigma charge-balance converter, a voltage reference, a calibration microcontroller with SRAM, a digital filter and a serial interface. The CS5505 and CS5506 include a four channel pseudo-differential (all four channels have the same reference measurement node) multiplexer.

The CS5505/6/7/8 include an on-chip reference but can also utilize an off-chip reference for precision applications. The CS5505/6/7/8 can be used to measure either unipolar or bipolar signals. The devices use self-calibration to insure excellent offset and gain accuracy.

The CS5505/7 are optimized to operate from a 32.768 kHz crystal but can be driven by an external clock whose frequency is between 30 kHz and 163 kHz (100 kHz for CS5506/8). When the digital filter is operated with a 32.768 kHz clock, the filter has zeros precisely at 50 and 60 Hz line frequencies and multiples thereof.

The CS5505/6/7/8 use a "start convert" command to latch the input channel selection and to start a convolution cycle on the digital filter. Once the filter cycle is completed, the output port is updated. When operated with a 32.768 kHz clock the ADC converts and updates its output port at 20 samples/sec. The throughput rate per channel is the output update rate divided by the number of channels being multiplexed. The output port includes a serial interface with two modes of operation.

The CS5505/6/7/8 can operate from dual polarity power supplies (+5 and -5), from a single +5

volt supply, or with +10 volts on the analog and +5 on the digital.

### **THEORY OF OPERATION FOR THE CS5505/6/7/8**

The front page of this data sheet illustrates the block diagram of the CS5505/6.

#### **Basic Converter Operation**

The CS5505/6/7/8 A/D converters have four operating states. These are standby, calibration, conversion and sleep. When power is first applied to the device a power-on reset delay of about 10 ms resets all of the logic in the device. The oscillator must then begin oscillating before the device can be considered functional. After power is applied or after waking from sleep, the device enters the standby state for 1800 clock cycles after clock is present. This allows the delta-sigma modulator and other circuitry (which are operating with very low currents) to reach a stable bias condition prior to entering into either the calibration or conversion states. During the 1800 cycle wake-up period, the device can accept an input command. Execution of this command will not occur until the complete wake-up period elapses.

#### **Calibration**

After the initial application of power, the CS5505/6/7/8 must enter the calibration state prior to performing accurate conversions. During calibration, the chip executes a two-step process. The device first performs an offset calibration and then follows this with a gain calibration. The two calibration steps determine the zero reference point and the full scale reference point of the converter's transfer function. From these points it calibrates the zero point and a gain slope to be used to properly scale the output digital codes when doing conversions.

The calibration state is entered whenever the CAL and CONV pins are high at the same time. The state of the CAL and CONV pins at power-on and when coming out of sleep are recognized as commands, but will not be executed until the end of the 1800 clock cycle wake-up period. Note that any time CONV transitions from low to high, the multiplexer inputs A0 and A1 are latched internal to the CS5505 and CS5506 devices. These latched inputs select the analog input channel which will be used once conversion commences.

If CAL and CONV become active (high) during the 1800 clock cycle wake-up time, the converter will wait until the wake-up period elapses before executing the calibration. If the wake-up time has elapsed, the converter will be in the standby mode waiting for instruction and will enter the calibration cycle immediately. The calibration lasts for 3246 clock cycles. Calibration coefficients are then retained in the SRAM (static RAM) for use during conversion.

At the end of the calibration cycle, the on-chip microcontroller checks the logic state of the CONV signal. If the CONV input is low the device will enter the standby state where it waits for further instruction. If the CONV signal is high at the end of the calibration cycle, the converter will enter the conversion state and perform a conversion on the input channel which was selected when CONV transitioned from low to high. The CAL signal can be returned low any time after calibration is initiated. CONV can also be returned low, but it should never be taken low and then taken back high until the calibration period has ended and the converter is in the standby state. If CONV is taken low and then high again with CAL high while the converter is calibrating, the device will interrupt the current calibration cycle and start a new one. If CAL is taken low and CONV is taken low and then high during calibration, the calibration cycle will continue as the conversion command is dis-

regarded. The states of A0, A1 and BP/UP are not important during calibrations.

If an "end of calibration" signal is desired, pulse the CAL signal high while leaving the CONV signal high continuously. Once the calibration is completed, a conversion will be performed. At the end of the conversion, DRDY will fall to indicate the first valid conversion after the calibration has been completed.

See Understanding Converter Calibration for details on how the converter calibrates its transfer function.

### Conversion

The conversion state can be entered at the end of the calibration cycle, or whenever the converter is idle in the standby state. If CONV is taken high to initiate a calibration cycle (CAL also high), and remains high until the calibration cycle is completed (CAL is taken low after CONV transitions high), the converter will begin a conversion upon completion of the calibration period. The device will perform a conversion on the input channel selected by the A0 and A1 inputs when CONV transitioned high. Table 1 indicates the multiplexer channel selection truth table for A0 and A1.

A1	A0	Channel addressed
0	0	AIN1
0	1	AIN2
1	0	AIN3
1	1	AIN4

**Table 1. Multiplexer Truth Table**

The A0 and A1 inputs are latched internal to the 4-channel devices (CS5505/6) when CONV rises. A0 and A1 have internal pull-down circuits which default the multiplexer to channel AIN1. The BP/UP pin is not a latched input. The BP/UP pin controls how the output word from the digital filter is processed. In bipolar mode

the output word computed by the digital filter is offset by 8000H in the 16-bit CS5505/7 or 80000H in 20-bit CS5506/8 (see Understanding Converter Calibration). BP/UP can be changed after a conversion is started as long as it is stable for 82 clock cycles of the conversion period prior to  $\overline{\text{DRDY}}$  falling. If one wishes to intermix measurement of bipolar and unipolar signals on various input channels, it is best to switch the BP/UP pin immediately after  $\overline{\text{DRDY}}$  falls and leave BP/UP stable until  $\overline{\text{DRDY}}$  falls again. If the converter is beginning a conversion starting from the standby state, BP/UP can be changed at the same time as A0 and A1.

The digital filter in the CS5505/6/7/8 has a Finite Impulse Response and is designed to settle to full accuracy in one conversion time. Therefore, the multiplexer can be changed at the conversion rate.

If CONV is left high, the CS5505/6/7/8 will perform continuous conversions on one channel. The conversion time will be 1622 clock cycles. If conversion is initiated from the standby state, there may be up to two XIN clock cycles of uncertainty as to when conversion actually begins. This is because the internal logic operates at one half the external clock rate and the exact phase of the internal clock may be 180° out of phase relative to the XIN clock. When a new conversion is initiated from the standby state, it will take up to two XIN clock cycles to begin. Actual conversion will use 1624 clock cycles before  $\overline{\text{DRDY}}$  goes low to indicate that the serial port has been updated. See the Serial Interface Logic section of the data sheet for information on reading data from the serial port.

In the event the A/D conversion command (CONV going positive) is issued during the conversion state, the current conversion will be terminated and a new conversion will be initiated.

### Voltage Reference

The CS5505/6/7/8 uses a differential voltage reference input. The positive input is VREF+ and the negative input is VREF-. The voltage between VREF+ and VREF- can range from 1 volt minimum to 3.0 volts maximum. The gain slope will track changes in the reference without recalibration, accommodating ratiometric applications.

The CS5505/6/7/8 include an on-chip voltage reference which outputs 2.5 volts on the VREFOUT pin. This voltage is referenced to the VA+ pin and will track changes relative to VA+. The VREFOUT output requires a 0.1  $\mu\text{F}$  capacitor connected between VREFOUT and VA+ for stability. When using the internal reference, the VREFOUT signal should be connected to the VREF- input and the VREF+ pin should be connected to the VA+ supply. The internal voltage reference is capable of sourcing 3  $\mu\text{A}$  maximum and sinking 50  $\mu\text{A}$  maximum. If a more precise reference voltage is required, an external voltage reference should be used. If an external voltage reference is used, the VREFOUT pin of the internal reference should be connected directly to VA-. It cannot be left open unless the 0.1  $\mu\text{F}$  capacitor is in place for stability.

External reference voltages can range from 1.0 volt minimum to 3.0 volts maximum. The common mode voltage range of the external

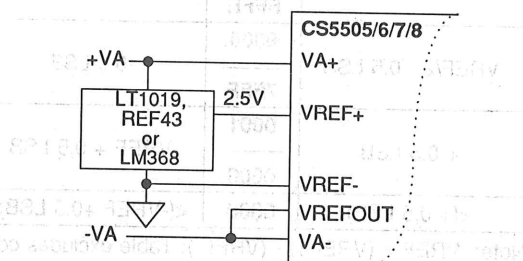


Figure 5. External Reference Connections



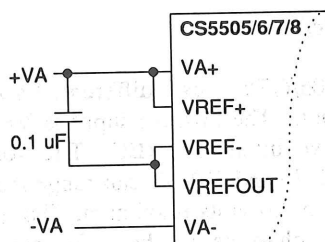


Figure 6. Internal Reference Connections

reference can allow the reference to lie at any voltage between the VA+ and VA- supply rails. Figures 5 and 6 illustrate how the CS5505/6/7/8 converters are connected for external and for internal voltage reference use, respectively.

### Analog Input Range

The analog input range is set by the magnitude of the voltage between the VREF+ and VREF- pins. In unipolar mode the input range will equal the magnitude of the voltage reference. In bipolar mode the input voltage range will equate to plus and minus the magnitude of the voltage reference. While the voltage reference can be as great as 3 volts, its common mode voltage can be any value as long as the reference inputs VREF+ and VREF- stay within the supply voltages for the A/D. The differential input voltage

can also have any common mode value as long as the maximum signal magnitude stays within the supply voltages.

The A/D converter is intended to measure dc or low frequency inputs. It is designed to yield accurate conversions even with noise exceeding the input voltage range as long as the spectral components of this noise will be filtered out by the digital filter. For example, with a 3.0 volt reference in unipolar mode, the converter will accurately convert an input dc signal up to 3.0 volts with up to 15% overrange for 60 Hz noise. A 3.0 volt dc signal could have a 60 Hz component which is 0.5 volts above the maximum input of 3.0 (3.5 volts peak; 3.0 volts dc plus 0.5 volts peak noise) and still accurately convert the input signal (XIN = 32.768 kHz). This assumes that the signal plus noise amplitude stays within the supply voltages.

The CS5505/6/7/8 converters output data in binary format when converting unipolar signals and in offset binary format when converting bipolar signals. Table 2 outlines the output coding for the 16-bit CS5505/7 and the 20-bit CS5506/8 in both unipolar and bipolar measurement modes.

CS5505 and CS5507 (16 Bit)			CS5506 and CS5508 (20 Bit)		
Unipolar Input Voltage	Output Codes	Bipolar Input Voltage	Unipolar Input Voltage	Output Codes	Bipolar Input Voltage
$>(\text{VREF} - 1.5 \text{ LSB})$	FFFF	$>(\text{VREF} - 1.5 \text{ LSB})$	$>(\text{VREF} - 1.5 \text{ LSB})$	FFFF	$>(\text{VREF} - 1.5 \text{ LSB})$
VREF - 1.5 LSB	FFFF FFFE	VREF - 1.5 LSB	VREF - 1.5 LSB	FFFF FFFE	VREF - 1.5 LSB
VREF/2 - 0.5 LSB	8000 7FFF	-0.5 LSB	VREF/2 - 0.5 LSB	8000 7FFFF	- 0.5 LSB
+ 0.5 LSB	0001 0000	-VREF + 0.5 LSB	+ 0.5 LSB	00001 00000	-VREF + 0.5 LSB
$<(+ 0.5 \text{ LSB})$	0000	$<(-\text{VREF} + 0.5 \text{ LSB})$	$<(+ 0.5 \text{ LSB})$	00000	$<(-\text{VREF} + 0.5 \text{ LSB})$

Note: VREF = (VREF+) - (VREF-); Table excludes common mode voltage on the signal and reference inputs.

Table 2. Output Coding



## **Understanding Converter Calibration**

Calibration can be performed at any time. A calibration sequence will minimize offset errors and set the gain slope scale factor. The delta-sigma modulator in the converter is a differential modulator. To calibrate out offset error, the converter internally connects the modulator differential inputs to an internal VREF- voltage and measures the 1's density output from the modulator. It stores the digital code representation for this 1's density in SRAM and remembers this code as being the zero scale point for the A/D conversion. The converter then connects the negative modulator differential input to the VREF- input and the positive modulator differential input to the VREF+ voltage. The 1's density output from the modulator is then recorded. The converter uses the digital representation of this 1's density along with the digital code for the zero scale point and calculates a gain scale factor. The gain scale factor is stored in SRAM and used for calculating the proper output codes during conversions.

The states of A0, A1 and BP/UP are ignored during calibration but should remain stable throughout the calibration period to minimize noise.

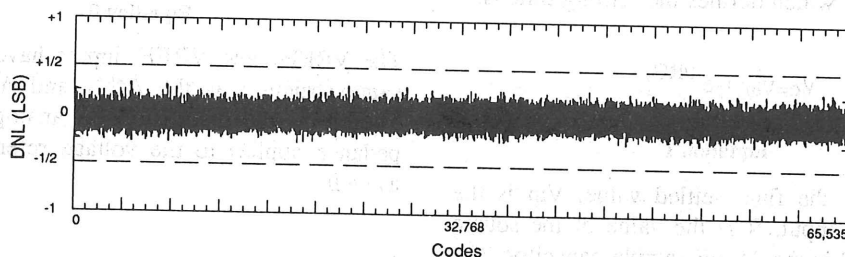
When conversions are performed in unipolar mode or in bipolar mode, the converter uses the same calibration factors to compute the digital output code. The only difference is that in bipolar mode the on-chip microcontroller offsets the computed output word by a code value of

8000H (16-bit) or 80000H (20-bit) and multiplies the LSB size by two. This means that the bipolar measurement range is not calibrated from full scale positive to full scale negative. Instead it is calibrated from the bipolar zero scale point to full scale positive. The slope factor is then extended below bipolar zero to accommodate the negative input signals. The converter can be used to convert both unipolar and bipolar signals by changing the BP/UP pin. Recalibration is not required when switching between unipolar and bipolar modes.

## **Converter Performance**

The CS5505/6/7/8 A/D converters have excellent linearity performance. Calibration minimizes the errors in offset and gain. The CS5505/7 devices have no missing code performance to 16-bits. The CS5506/8 devices have no missing codes guaranteed to 18-bits. Some codes may be missing in the CS5506/8 devices at the 20-bit level because of truncation in the digital computation of the output digital word. Only a few codes will be missing at the 19-bit level. Figure 7 illustrates the DNL of the 16-bit CS5505. The converters achieve Common Mode Rejection (CMR) at dc of 105 dB typical, and CMR at 50 and 60 Hz of 120 dB typical.

The CS5505/6/7/8 can experience some drift as temperature changes. The CS5505/6/7/8 use chopper-stabilized techniques to minimize drift. Measurement errors due to offset or gain drift can be eliminated at any time by recalibrating the converter.



**Figure 7. CS5505 Differential Nonlinearity plot.**

# Analog Input Impedance Considerations

The analog input of the CS5505/6/7/8 can be modeled as illustrated in Figure 8 (the model ig-

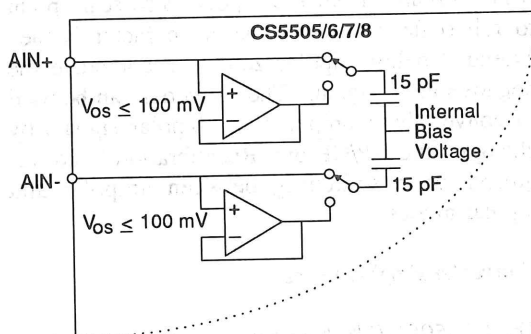


Figure 8. Analog Input Model

nores the multiplexer switch resistance as it is small relative to the other component values). Capacitors (15 pF each) are used to dynamically sample each of the inputs (AIN+ and AIN-). Every half XIN cycle the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge (a dynamic demand of current) is required from the input source to settle the voltage of the sample capacitor to its final value. The voltage on the output of the buffer may differ up to 100 mV from the actual input voltage due to the offset voltage of the buffer. Timing allows one half of a XIN clock cycle for the voltage on the sample capacitor to settle to its final value. The equation which defines the settling time is:

$$V_o = V_{in} [1 - e^{-t/RC}]$$

Equation 1

where  $V_o$  is the final settled value,  $V_{in}$  is the value of the input,  $R$  is the value of the source resistance,  $C$  is the 15 pF sample capacitor. The

value of  $t$  is  $1/(2XIN)$ . From this basic equation, Equation 2 can be developed:

$$R_{smax} = \frac{1}{2XIN(15pF + C_{ext}) \ln[(15pF/(15pF + C_{ext}))100mV/V_e]}$$

Equation 2

Equation 2 defines the maximum  $R_s$  which will still allow full settling when each charge packet is sourced onto the 15 pF sample capacitor.  $C_{ext}$  is any stray capacitance or external capacitance added to the AIN node.

Equation 2 assumes the offset voltage of the buffer is 100 mV, which is the worst case. The value of  $V_e$  is the maximum error voltage which is acceptable. For a maximum error of 1/4 LSB at 16-bits (Reference Voltage = 2.5, Unipolar mode) the above equation indicates that when operating from a 32.768 kHz XIN, source resistances up to 82 kΩ are acceptable in the presence of stray capacitance ( $C_{ext} = 5$  pF). Higher XIN rates will reduce the value of acceptable source resistance which allows full settling.

If the XIN operating frequency is much greater (10x) than  $1/(R_s C_{ext})$ , the charge packets will be averaged by the RC input filter. Under this condition, Equation 3 defines the maximum  $R_s$  for a given error voltage ( $V_e$ ):

$$R_{smax} = \frac{1}{2XIN(15pF) \ln[100mV/V_e]}$$

Equation 3

The VREF+ and VREF- inputs have nearly the same structure as the AIN+ and AIN- inputs. Therefore, the discussion on analog input impedance applies to the voltage reference inputs as well.

### Digital Filter Characteristics

The digital filter in the CS5505/6/7/8 is the combination of a comb filter and a low pass filter. The comb filter has zeros in its transfer function which are optimally placed to reject line interference frequencies (50 and 60 Hz and their multiples) when the CS5505/6/7/8 is clocked at 32.768 kHz. Figures 9, 10 and 11 illustrate the magnitude and phase characteristics of the filter. Figure 9 illustrates the filter attenuation from dc to 260 Hz. At exactly 50, 60, 100, and 120 Hz

the filter provides over 120 dB of rejection. Table 3 indicates the filter attenuation for each of the potential line interference frequencies when the converter is operating with a 32.768 kHz clock. The converter yields excellent attenuation of these interference frequencies even if the fundamental line frequency should vary  $\pm 1\%$  from its specified frequency. The -3 dB corner frequency of the filter when operating from a 32.768 kHz clock is 17 Hz. Figure 11 illustrates that the phase characteristics of the filter are precisely linear phase.

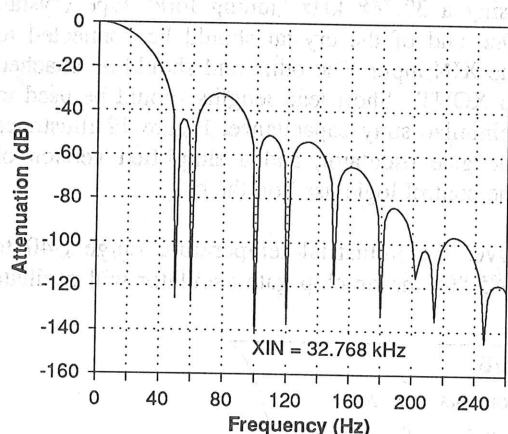


Figure 9. Filter Magnitude Plot to 260 Hz

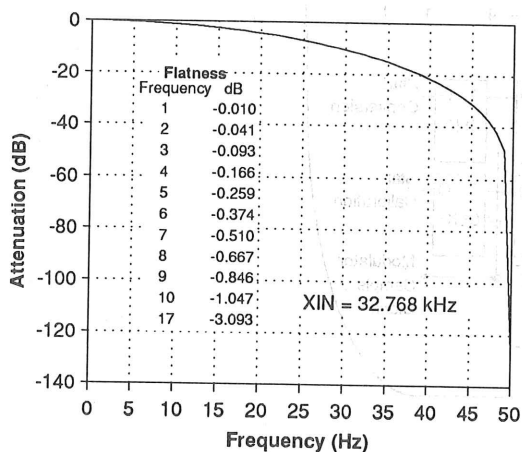


Figure 10. Filter Magnitude Plot to 50 Hz

Frequency (Hz)	Notch Depth (dB)	Frequency (Hz)	Minimum Attenuation (dB)
50	125.6	50 $\pm 1\%$	55.5
60	126.7	60 $\pm 1\%$	58.4
100	145.7	100 $\pm 1\%$	62.2
120	136.0	120 $\pm 1\%$	68.4
150	118.4	150 $\pm 1\%$	74.9
180	132.9	180 $\pm 1\%$	87.9
200	102.5	200 $\pm 1\%$	94.0
240	108.4	240 $\pm 1\%$	104.4

Table 3. Filter Notch Attenuation (XIN = 32.768 kHz)

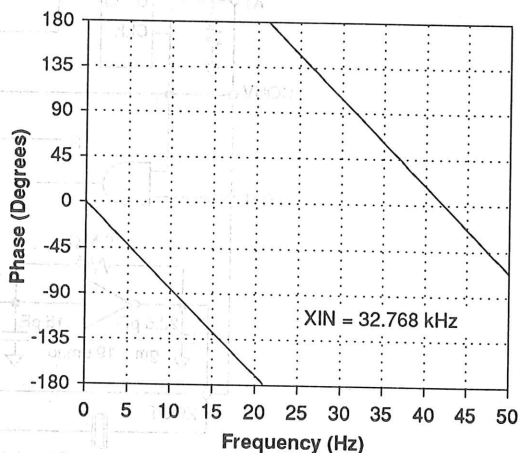


Figure 11. Filter Phase Plot to 50 Hz

If the CS5505/6/7/8 is operated at a clock rate other than 32.768 kHz, the filter characteristics, including the comb filter zeros, will scale with the operating clock frequency. Therefore, optimum rejection of line frequency interference will occur with the CS5505/6/7/8 running at 32.768 kHz. The CS5505/7 can be used with external clock rates from 30 kHz to 163 kHz (CS5506/8 to 100 kHz).

### Anti-Alias Considerations for Spectral Measurement Applications

Input frequencies greater than one half the output word rate (CONV = 1) may be aliased by the converter. To prevent this, input signals should be limited in frequency to no greater than one half the output word rate of the converter (when CONV = 1). Frequencies close to the modulator sample rate (XIN/2) and multiples thereof may also be aliased. If the signal source includes spectral components above one half the output

word rate (when CONV = 1) these components should be removed by means of low-pass filtering prior to the A/D input to prevent aliasing. Spectral components greater than one half the output word rate on the VREF inputs (VREF+ and VREF-) may also be aliased. Filtering of the reference voltage to remove these spectral components from the reference voltage is desirable.

### Crystal Oscillator

The CS5505/6/7/8 is designed to be operated using a 32.768 kHz "tuning fork" type crystal. One end of the crystal should be connected to the XIN input. The other end should be attached to XOUT. Short lead lengths should be used to minimize stray capacitance. Figure 12 illustrates the gate oscillator, and a simplified version of the control logic used on the chip.

Over the industrial temperature range (-40 to +85 °C) the on-chip gate oscillator will oscillate

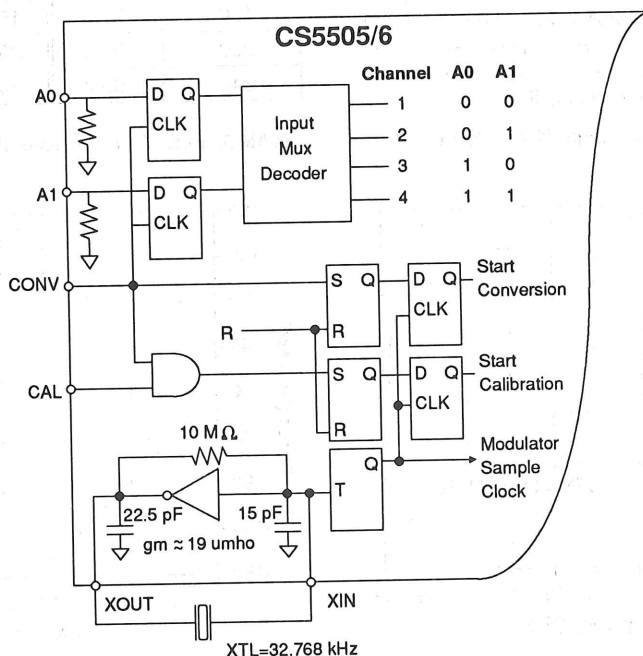


Figure 12. Gate Oscillator and Control Logic

with other crystals in the range of 30 kHz to 53 kHz. Over the military temperature range (-55 to +125 °C) the on-chip gate oscillator is designed to work only with a 32.768 kHz crystal. The chip will operate with external clock frequencies from 30 kHz to 100 kHz over all temperature ranges. The 32.768 kHz crystal is normally specified as a time-keeping crystal with tight specifications for both initial frequency and for drift over temperature. To maintain excellent frequency stability, these crystals are specified only over limited operating temperature ranges (i.e. -10 to +60 °C) by the manufacturers. Applications of these crystals with the CS5505/6/7/8 do not require tight initial tolerance or low tempco drift. Therefore, a lower cost crystal with looser initial tolerance and tempco will generally be adequate for use with the CS5505/6/7/8 converters. Also check with the manufacturer about wide temperature range application of their standard crystals. Generally, even those crystals specified for limited temperature range will operate over much larger ranges if frequency stability over temperature is not a requirement. The frequency stability can be as bad as  $\pm 3000$  ppm over the operating temperature range and still be typically better than the line frequency (50 or 60 Hz) stability over cycle to cycle during the course of a day. There are crystals available for operation over the military temperature range (-55 to +125 °C). See the Appendix for suppliers of 32.768 kHz crystals.

## Serial Interface Logic

The digital filter in the CS5505/6/7/8 takes 1624 clock cycles to compute an output word once a conversion begins. At the end of the conversion cycle, the filter will attempt to update the serial port. Two clock cycles prior to the update  $\overline{\text{DRDY}}$  will go high. When  $\overline{\text{DRDY}}$  goes high just prior to a port update it checks to see if the port is either empty or unselected ( $\overline{\text{CS}} = 1$ ). If the port is empty or unselected, the digital filter will update the port with a new output word.

When new data is put into the port  $\overline{\text{DRDY}}$  will go low.

Data can be read from the serial port in either of two modes. The M/SLP pin determines which serial mode is selected. Serial port mode selection is as follows:

SSC (Synchronous Self-Clocking) mode; M/SLP = VD+, or SEC (Synchronous External Clocking) mode; M/SLP = DGND. Timing diagrams which illustrate the SSC and SEC timing are in the tables section of this data sheet.

## Synchronous Self-Clocking Mode

The serial port operates in the SSC mode when the M/SLP pin is connected to the VD+ pin on the part. In SSC mode the CS5505/6/7/8 furnishes both the serial output data (SDATA) and the serial clock (SCLK). When the serial port is updated at the end of a conversion,  $\overline{\text{DRDY}}$  falls. If  $\overline{\text{CS}}$  is low, the SDATA and SCLK pins will come out of the high impedance state two XIN clock cycles after  $\overline{\text{DRDY}}$  falls. The MSB data bit will be presented for two cycles of XIN clock. The SCLK signal will rise in the middle of the MSB data bit. When SCLK then returns low the (MSB - 1) bit will appear. Subsequent data bits will be output on each falling edge of SCLK until the LSB data bit is output. After the LSB data bit is output, the SCLK will fall at which time both the SDATA and SCLK outputs will return to the high impedance output state.  $\overline{\text{DRDY}}$  will return high at this time.

If  $\overline{\text{CS}}$  is taken low after  $\overline{\text{DRDY}}$  falls, the MSB data bit will appear within two XIN clock cycles after  $\overline{\text{CS}}$  is taken low.  $\overline{\text{CS}}$  need not be held low for the entire data output. If  $\overline{\text{CS}}$  is returned high during a data bit the port will complete the output of that bit and then go into the Hi-Z state. The port can be reselected any time prior to the completion of the next conversion ( $\overline{\text{DRDY}}$  falling) to allow the remaining data bits to be output.

### Synchronous External-Clocking Mode

The serial port operates in the SEC mode when the M/SLP pin is connected to the DGND pin. SDATA is the output pin for the serial data. When  $\overline{CS}$  goes low after new data becomes available ( $\overline{DRDY}$  goes low), the SDATA pin comes out of Hi-Z with the MSB data bit present. SCLK is the input pin for the serial clock in the SEC mode. If the MSB data bit is on the SDATA pin, the first rising edge of SCLK enables the shifting mechanism. This allows the falling edges of SCLK to shift subsequent data bits out of the port. Note that if the MSB data bit is output and the SCLK signal is high, the first falling edge of SCLK will be ignored because the shifting mechanism has not become activated. After the first rising edge of SCLK, each subsequent falling edge will shift out the serial data. Once the LSB is present, the rising edge of SCLK will cause the SDATA output to go to Hi-Z and  $\overline{DRDY}$  to return high. The serial port register will be updated with a new data word upon the completion of another conversion if the serial port has been emptied, or if the  $\overline{CS}$  is inactive (high).

$\overline{CS}$  can be operated asynchronously to the  $\overline{DRDY}$  signal. The  $\overline{DRDY}$  signal need not be monitored as long as the  $\overline{CS}$  signal is taken low for at least two XIN clock cycles plus 200 ns prior to SCLK being toggled. This ensures that  $\overline{CS}$  has gained control over the serial port.

### Sleep Mode

The CS5505/6/7/8 devices offer two methods of putting the device into a SLEEP condition to conserve power. Calibration words will be retained in SRAM during either sleep condition. The M/SLP pin can be put into the SLEEP threshold to lower the operating power used by the device to about 1% of nominal. Alternately, the clock into the XIN pin can be stopped. This will lower the power consumed by the converter to about 30% of nominal. In both cases, the

converter must go through a wake-up sequence prior to conversions being initiated. This wake-up sequence includes the 10 msec. (typ.) power-on-reset delay, the start-up of the oscillator (unless an external clock is used), and the 1800 clock cycle wake-up delay after the clock begins. When coming out of the sleep condition, the converter will latch the A0 and A1 inputs.

Figure 13 illustrates how to use a gate and resistors to bias the M/SLP pin into the SLEEP threshold region when using the converter in the SSC mode. To use the SEC mode return resistor R1 to DGND instead of the supply. When in the SEC mode configuration the CS5505/6/7/8 will enter the SLEEP threshold when the logic control input is a logic 1 (VD+). Note that large resistors can be used to conserve power while in sleep. The input leakage of the pin is typically less than 1  $\mu$ A even at 125 °C, although the worst case specification tables indicate a leakage of 10  $\mu$ A maximum.

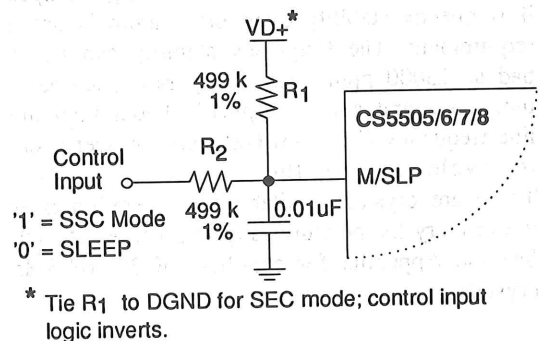


Figure 13. Sleep Threshold Control

### Power Supplies and Grounding

The CS5505/6/7/8 devices are very flexible in terms of power supply arrangements. The devices can operate from dual supplies of  $\pm 5$ V or from a single supply of +5V.

The analog and digital supply pins to the CS5505/6/7/8 devices are brought out on

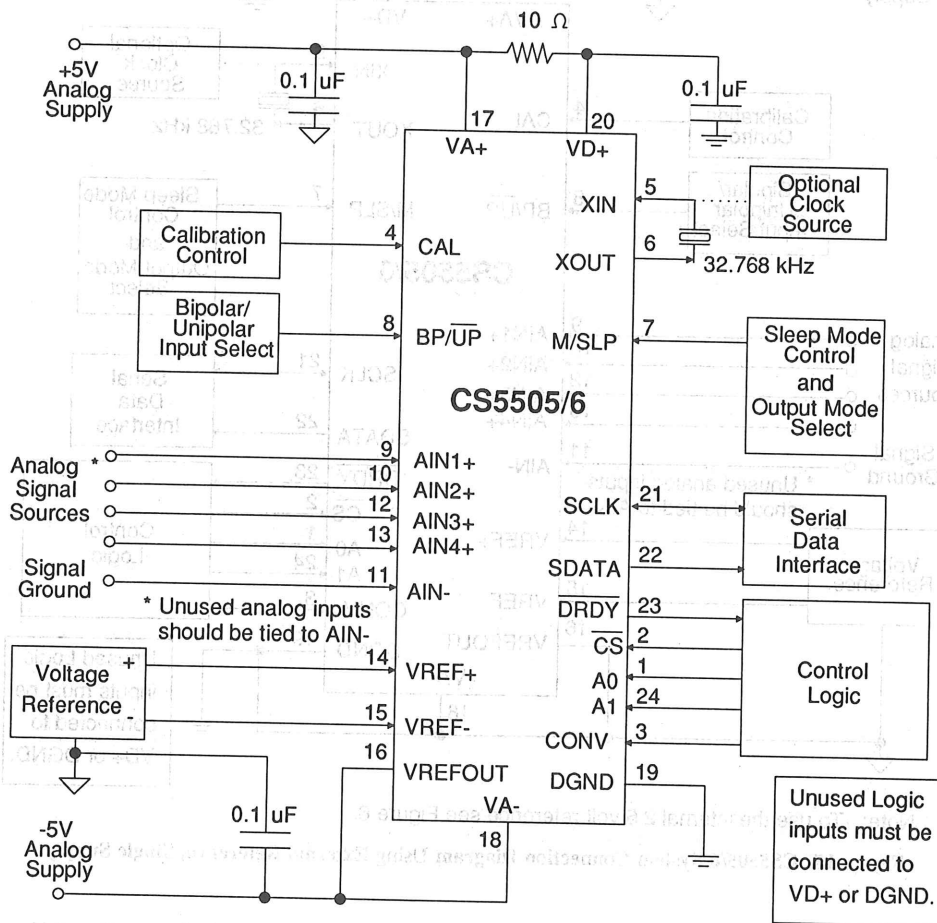


separate pins to minimize noise coupling between the analog and digital sections of the chip. Note that there is no analog ground pin. The analog supply current flows into the VA+ pin and out of the VA- pin. No analog ground pin is required because the inputs for measurement and for the voltage reference are differential and require no ground. In the digital section of the chip the supply current flows into the VD+ pin and out of the DGND pin. As a CMOS device, the CS5505/6/7/8 requires that the supply voltage on the VA+ pin always be more positive

than the voltage on any other pin of the device. If this requirement is not met, the device can latch-up or be damaged. In all circumstances the VA+ voltage must remain more positive than the VD+ or DGND pins; VD+ must remain more positive than the DGND pin; and VA- must never be taken more positive than DGND plus 0.3 volts.

Figure 14 illustrates the CS5505/6 powered with dual ( $\pm 5V$ ) supply voltages. Note that all supply pins are bypassed with 0.1  $\mu F$  capacitors and

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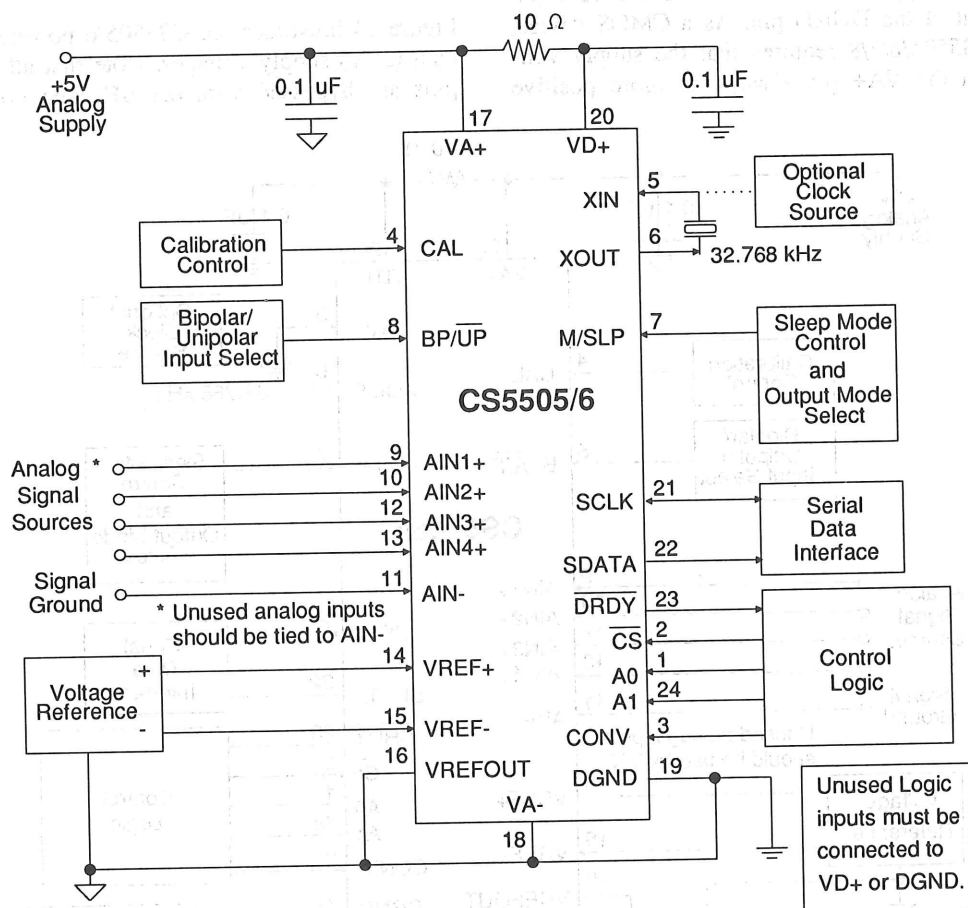


Note: To use the internal 2.5 volt reference see Figure 6.

Figure 14. CS5505/6 System Connection Diagram Using External Reference, Dual Supplies

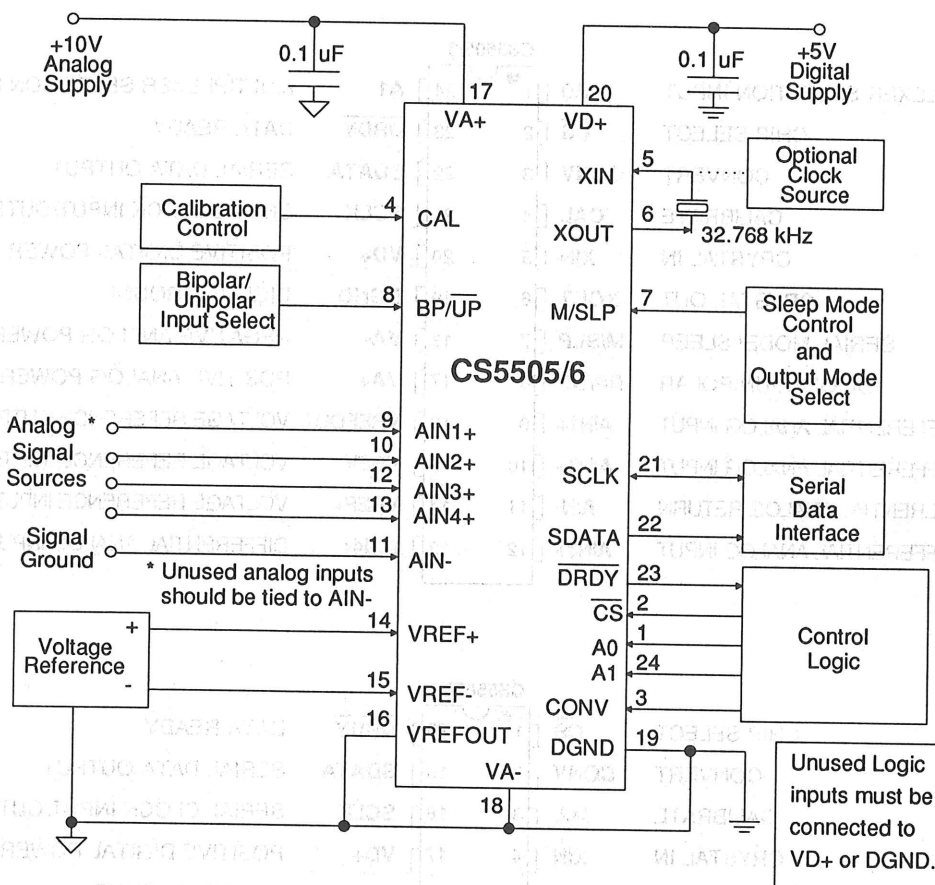


that the VD+ digital supply is derived from the VA+ supply. Figure 15 illustrates the CS5505/6 with a single supply arrangement. Figure 16 illustrates the CS5505/6 with dual (+10V Analog, +5V Digital) supplies. The VA+ supply can be any value from +10 volts to +5 volts, but must always be more positive or equal to the VD+ supply voltage.



Note: To use the internal 2.5 volt reference see Figure 6.

**Figure 15. CS5505/6 System Connection Diagram Using External Reference, Single Supply**



Note: To use the internal 2.5 volt reference see Figure 6.

**Figure 16. CS5505/6 System Connection Diagram Using External Reference, Dual Supply, +10V Analog, +5V Digital**

CS5505/6					
MULTIPLEXER SELECTION INPUT	A0	1	24	A1	MULTIPLEXER SELECTION INPUT
CHIP SELECT	$\overline{\text{CS}}$	2	23	$\overline{\text{DRDY}}$	DATA READY
CONVERT	CONV	3	22	SDATA	SERIAL DATA OUTPUT
CALIBRATE	CAL	4	21	SCLK	SERIAL CLOCK INPUT/OUTPUT
CRYSTAL IN	XIN	5	20	VD+	POSITIVE DIGITAL POWER
CRYSTAL OUT	XOUT	6	19	DGND	DIGITAL GROUND
SERIAL MODE/ SLEEP	M/SLP	7	18	VA-	NEGATIVE ANALOG POWER
BIPOLAR/UNIPOLAR	BP/ $\overline{\text{UP}}$	8	17	VA+	POSITIVE ANALOG POWER
DIFFERENTIAL ANALOG INPUT	AIN1+	9	16	VREFOUT	VOLTAGE REFERENCE OUTPUT
DIFFERENTIAL ANALOG INPUT	AIN2+	10	15	VREF-	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG RETURN	AIN-	11	14	VREF+	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG INPUT	AIN3+	12	13	AIN4+	DIFFERENTIAL ANALOG INPUT

CS5507/8					
CHIP SELECT	$\overline{\text{CS}}$	1	20	$\overline{\text{DRDY}}$	DATA READY
CONVERT	CONV	2	19	SDATA	SERIAL DATA OUTPUT
CALIBRATE	CAL	3	18	SCLK	SERIAL CLOCK INPUT/OUTPUT
CRYSTAL IN	XIN	4	17	VD+	POSITIVE DIGITAL POWER
CRYSTAL OUT	XOUT	5	16	DGND	DIGITAL GROUND
SERIAL MODE/ SLEEP	M/SLP	6	15	VA-	NEGATIVE ANALOG POWER
BIPOLAR/UNIPOLAR	BP/ $\overline{\text{UP}}$	7	14	VA+	POSITIVE ANALOG POWER
DIFFERENTIAL ANALOG INPUT	AIN+	8	13	VREFOUT	VOLTAGE REFERENCE OUTPUT
NO CONNECTION	NC	9	12	VREF-	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG INPUT	AIN-	10	11	VREF+	VOLTAGE REFERENCE INPUT

\*Pinout applies to both DIP and SOIC

**PIN CONNECTIONS\*****PIN DESCRIPTIONS**

Pin numbers for four channel devices are in parentheses.

**Clock Generator****XIN; XOUT - Crystal In; Crystal Out, Pins 4 (5) and 5 (6).**

A gate inside the chip is connected to these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into the XIN pin to provide the master clock for the device. Loss of clock will put the device into a lower powered state (approximately 70% power reduction).

**Serial Output I/O****M/SLP - Serial Interface Mode Select/ Sleep, Pin 6 (7).**

Dual function pin which selects the operating mode of the serial port and provides a very low power sleep function. When M/SLP is tied to the VD+ pin the serial port will operate in the Synchronous Self-Clocking (SSC) mode. When M/SLP is tied to the DGND pin the serial port will operate in the Synchronous External Clocking mode. When the M/SLP pin is tied half way between VD+ and DGND the chip will enter into a very low powered sleep mode in which its calibration data will be maintained.

 **$\overline{\text{CS}}$  - Chip Select, Pin 1 (2).**

This input allows an external device to access the serial port.

 **$\overline{\text{DRDY}}$  - Data Ready, Pin 20 (23)**

Data Ready goes low at the end of a digital filter convolution cycle to indicate that a new output word has been placed into the serial port.  $\overline{\text{DRDY}}$  will return high after all data bits are shifted out of the serial port or two master clock cycles before new data becomes available if the  $\overline{\text{CS}}$  pin is inactive (high).

**SDATA - Serial Data Output, Pin 19 (22).**

SDATA is the output pin of the serial output port. Data from this pin will be output at a rate determined by SCLK and in a format determined by the M/SLP pin. Data is output MSB first and advances to the next data bit on the falling edges of SCLK. SDATA will be in a high impedance state when not transmitting data.

**SCLK - Serial Clock Input/Output, Pin 18 (21).**

A clock signal on this pin determines the output rate of the data from the SDATA pin. The M/SLP pin determines whether SCLK is an input or and output. When used as an input, it must not be allowed to float.

### ***Control Input Pins***

#### **CAL - Calibrate, Pin 3 (4).**

When taken high the same time that the CONV pin is taken high the converter will perform a self-calibration which includes calibration of the offset and gain scale factors in the converter.

#### **CONV - Convert, Pin 2 (3).**

The CONV pin initiates a calibration cycle if it is taken from low to high while the CAL pin is high, or it initiates a conversion if it is taken from low to high with the CAL pin low. CONV latches the multiplexer selection when it transitions from low to high on the multiple channel devices. If CONV is held high (CAL low) the converter will do continuous conversions.

#### **A0, A1 - Multiplexer Selection Inputs, Pins (1, 24).**

A0 and A1 select the input channel for conversion on the multi-channel input devices. A0 and A1 are latched when CONV transitions from low to high. These two inputs have pull-down resistors internal to the chip.

#### **BP/ $\overline{\text{UP}}$ - Bipolar/Unipolar, Pin 7 (8).**

The BP/ $\overline{\text{UP}}$  pin selects the conversion mode of the converter. When high the converter will convert bipolar input signals; when low it will convert unipolar input signals.

### ***Measurement and Reference Inputs***

#### **AIN+, AIN-, (AIN1+, AIN2+, AIN3+, AIN4+, AIN-) - Differential Analog Inputs, Pins 8, 10 (9, 10, 12, 13, 11).**

AIN- in the CS5505/6 is a common measurement node for AIN1+, AIN2+, AIN3+ and AIN4+.

#### **VREF+, VREF- - Differential Voltage Reference Inputs, Pins 11, 12 (14, 15).**

A differential voltage reference on these pins operates as the voltage reference for the converter. The voltage between these pins can be any voltage between 1.0 and 3.0 volts.

### ***Voltage Reference***

#### **VREFOUT - Voltage Reference Output, Pin 13 (16).**

The on-chip voltage reference is output from this pin. The voltage reference has a nominal magnitude of 2.5 volts and is referenced to the VA+ pin on the converter.

### ***Power Supply Connections***

#### **VA+ - Positive Analog Power, Pin 14 (17).**

Positive analog supply voltage. Nominally +5 volts.

#### **VA- - Negative Analog Power, Pin 15 (18).**

Negative analog supply voltage. Nominally -5 volts when using dual polarity supplies; or 0 volts (tied to system analog ground) when using single supply operation.

## VD+ - Positive Digital Power, Pin 17 (20).

Positive digital supply voltage. Nominally +5 volts.

## DGND - Digital Ground, Pin 16 (19).

Digital Ground.

## Other

## NC - No Connection, Pin 9.

Pin should be left floating.

## SPECIFICATION DEFINITIONS

### Linearity Error

The deviation of a code from a straight line which extends between two fixed points on the A/D converter transfer function. In unipolar mode the straight line extends from one point located 1/2 LSB below the first code transition, one count above all zeros; to the second point located 1/2 LSB beyond the code transition to all ones. In bipolar mode the straight line extends from one point located 1/2 LSB beyond the code transition to all ones, passing through a point 1/2 LSB below code 8000(H) (16-bit); 80000(H) (20-bit); extending to beyond negative full scale. Units are in percent of full-scale.

### Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

### Full Scale Error

The deviation of the last code transition from the ideal  $[(VREF+) - (VREF-)] - 3/2 \text{ LSB}$ . Units are in LSBs.

### Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above the voltage on the AIN- pin.) when in unipolar mode (BP/UP low). Units are in LSBs.

### Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below the voltage on the AIN- pin.) when in bipolar mode (BP/UP high). Units are in LSBs

### ORDERING GUIDE

Model Number	# of Channels	Resolution	Linearity Error	Temperature Range (°C)	Package Type
CS5505-AP	4	16-Bits	0.0030%	-40 to +85	24-pin 0.3" Plastic DIP
CS5505-AS	4	16-Bits	0.0030%	-40 to +85	24-pin 0.3" SOIC
CS5505-SD	4	16-Bits	0.0030%	-55 to +125	24-pin 0.3" CerDip
CS5506-BP	4	20-Bits	0.0015%	-40 to +85	24-pin 0.3" Plastic DIP
CS5506-BS	4	20-Bits	0.0015%	-40 to +85	24-pin 0.3" SOIC
CS5506-SD	4	20-Bits	0.0030%	-55 to +125	24-pin 0.3" CerDIP
CS5507-AP	1	16-Bits	0.0030%	-40 to +85	20-pin 0.3" Plastic DIP
CS5507-AS	1	16-Bits	0.0030%	-40 to +85	20-pin 0.3" SOIC
CS5507-SD	1	16-Bits	0.0030%	-55 to +125	20-pin 0.3" CerDIP
CS5508-BP	1	20-Bits	0.0015%	-40 to +85	20-pin 0.3" Plastic DIP
CS5508-BS	1	20-Bits	0.0015%	-40 to +85	20-pin 0.3" SOIC
CS5508-SD	1	20-Bits	0.0030%	-55 to +125	20-pin 0.3" CerDIP
CDB5505	CS5505 Evaluation Board				
CDB5506	CS5506 Evaluation Board				
CDB5507	CS5507 Evaluation Board				
CDB5508	CS5508 Evaluation Board				



**APPENDIX**

The following companies provide 32.768 kHz crystals in many package varieties and temperature ranges.

**Fox Electronics**  
5570 Enterprise Parkway  
Fort Meyers, FL 33905  
(813) 693-0099

**Micro Crystal Division / SMH**  
702 West Algonquin Road  
Arlington Heights, IL 60005  
(708) 806-1485

**SaRonix**  
4010 Transport Street  
Palo Alto, California 94303  
(415) 856-6900

**Statek**  
512 North Main  
Orange, California 92668  
(714) 639-7810

**IQD Ltd.**  
North Street  
Crewkerne  
Somerset TA18 7AK  
England  
0460 77155

**Mr. Pierre Hersberger**  
Microcrystal/DIV. ETA S.A.  
Schild-Rust-Strasse 17  
Grenchen CH-2540  
Switzerland  
065 53 05 57

**Taiwan X'tal Corp.**  
5F. No. 16, Sec 2, Chung Yang S. RD.  
Reitou, Taipei, Taiwan R. O. C.  
Tel: 02-894-1202  
Fax: 02-895-6207

**Interquip Limited**  
24/F Million Fortune Industrial Centre  
34-36 Chai Wan Kok Street, Tsuen Wan N T  
Tel: 4135515  
Fax: 4137053

**S& T Enterprises, Ltd.**  
Rm 404 Blk B  
Sea View Estate  
North Point, Hong Kong  
Tel: 5784921  
Fax: 8073126

**Mr. Darren Mcleod**  
Hy-Q International Pty. Ltd.  
12 Rosella Road,  
FRANKSON, 3199  
Victoria, Australia  
Tel: 61-3-783 9611  
Fax: 61-3-783 9703

## ***Evaluation Board for CS5505/6/7/8 Series of ADC's***

### **Features**

- Operation with on-board 32.768 kHz crystal or off-board clock source
- Jumper selectable:  
SSC mode; SEC mode; Sleep
- DIP Switch Selectable:  
BP/UP mode; A0, & A1 channel selection
- On-board precision voltage reference
- Access to all digital control pins

### **General Description**

The CDB5505/5506/5507/5508 is a circuit board designed to provide quick evaluation of the CS5505/6/7/8 series of A/D converters. The board can be configured to evaluate the CS5505/6/7/8 in either SSC or SEC serial port mode.

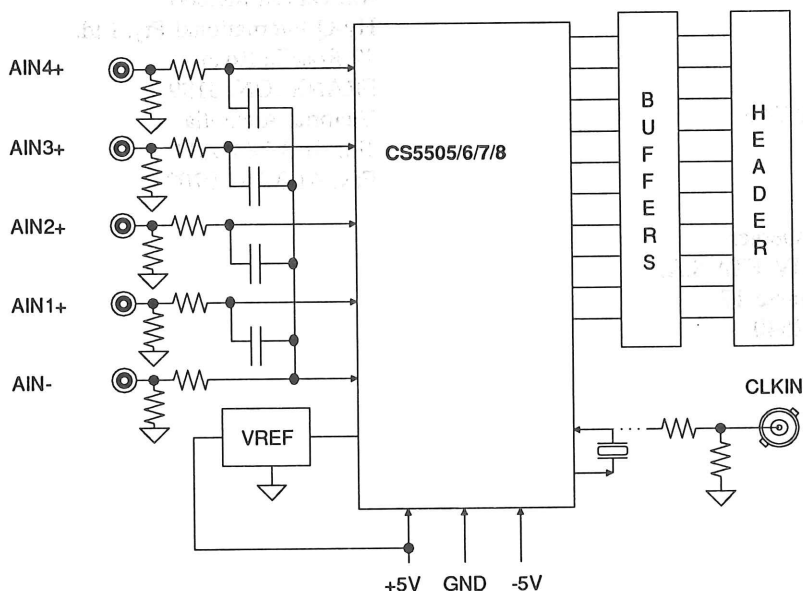
The board allows access to all of the digital interface pins of the CS5505/6/7/8 chip.

### **ORDERING INFORMATION**

CDB5505  
CDB5507

CDB5506  
CDB5508

### **Block Diagram**



### Introduction

The CDB5505/6/7/8 evaluation board provides a quick means of testing the CS5505/6/7/8 series A/D converters. The CS5505/6/7/8 converters require a minimal amount of external circuitry. The evaluation board comes configured with the A/D converter chip operating from a 32.768 kHz crystal and with an off-chip precision 2.5 volt reference. The board provides access to all of the digital interface pins of the CS5505/6/7/8 chip.

The board is configured for operation from +5 and -5 volt power supplies, but can be operated from a single +5 volt supply if the -5V binding post is shorted to the GND binding post.

### Evaluation Board Overview

The board provides a complete means of making the CS5505/6/7/8 A/D converter chip function. The user must provide a means of taking the output data from the board in serial format and using it in his system.

Figure 1 illustrates the schematic for the board. The board comes configured for the A/D converter chip to operate from the 32.768 kHz watch crystal. A BNC connector for an external clock is provided on the board. To connect the external BNC source to the converter chip, a circuit trace must be cut. Then a jumper must be inserted in the proper holes to connect the XIN pin of the converter to the input line from the BNC. The BNC input is terminated with a 50Ω resistor. Remove this resistor if driving from a logic gate. See the schematic in Figure 1.

The board comes with the A/D converter VREF+ and VREF- pins hard-wired to the 2.5 volt bandgap voltage reference IC on the board. The VREF+ and VREF- pins can be connected to either the on chip reference or an off-board reference if the connections (2A and 2B) to the bandgap IC are cut.

Note that the pin-out of the CS5505/6/7/8 series chips allows the 20-pin single channel devices to be plugged into the 24-pin, four channel footprint. See figure 2 which illustrates the footprint compatibility.

Prior to powering up the board, select the serial port operating mode with the appropriate jumper on the M/SLP header. The device can be operated in either the SSC (Synchronous Self-Clocking) or the SEC (Synchronous External Clocking) mode. See the device data sheet for an explanation of these modes.

All of the control pins of the CS5505/6/7/8 are available at the J1 header connector. Buffer ICs U2 and U3 are used to buffer the converter for interface to off-board circuits. The buffers are used on the evaluation board only because the exact loading and off-board circuitry is unknown. Most applications will not require the buffer ICs for proper operation.

To put the board in operation, select either bipolar or unipolar mode with DIP switch S2. Then press the CAL pushbutton after the board is powered up. This initiates calibration of the converter which is required before measurements can be taken.

To select an input channel on the four channel devices, use DIP switch S2 to select the inputs for A0 and A1 (see table 1). Once A0 and A1 are selected, the CONV switch (S2-3) must be switched on (closed) and then open to cause the

A1	A0	Channel addressed
0	0	AIN1
0	1	AIN2
1	0	AIN3
1	1	AIN4

Table 1. Multiplexer Truth Table

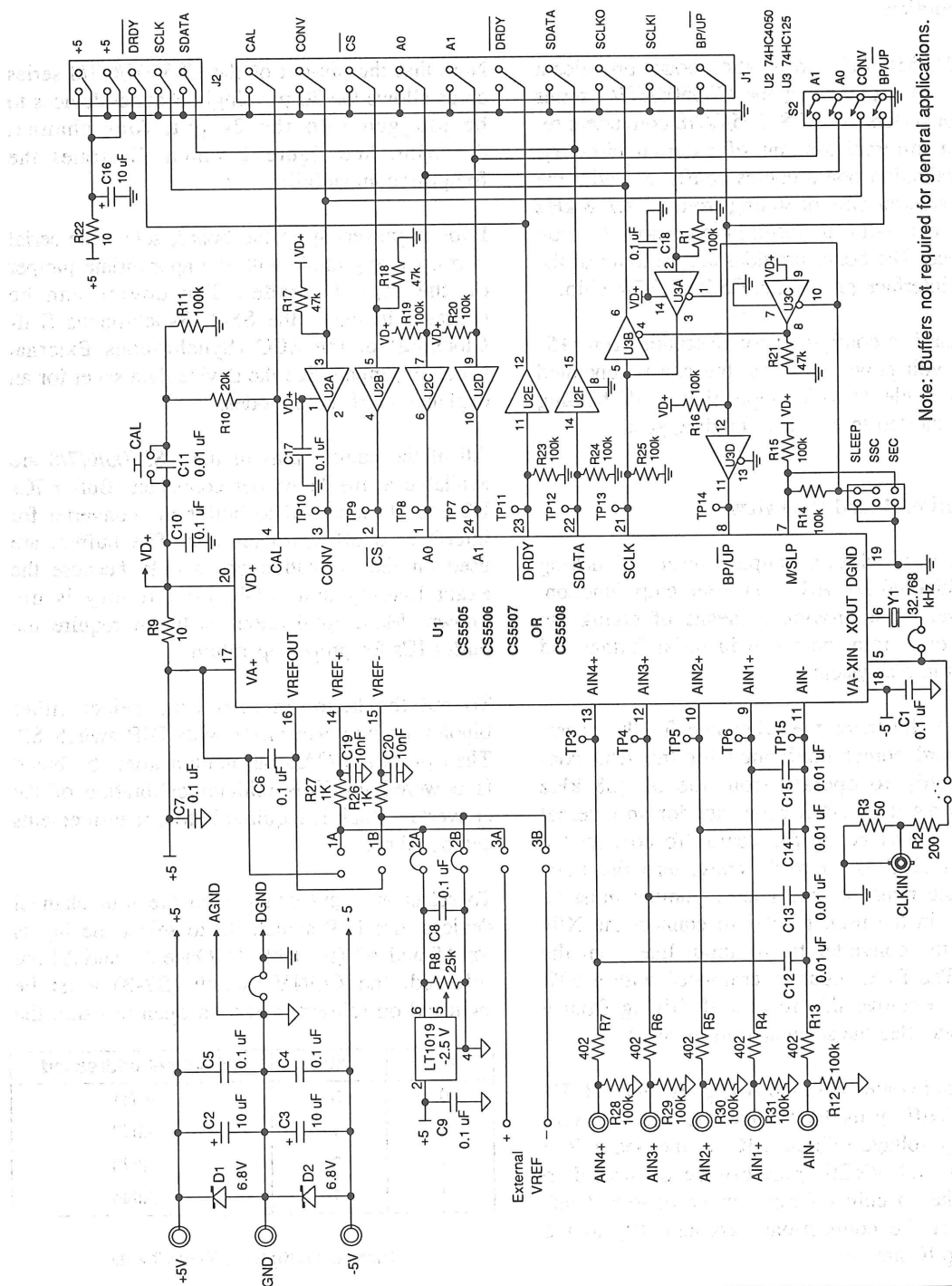
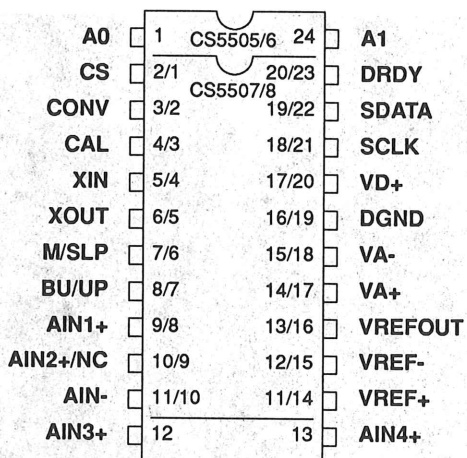


Figure 1. ADC Connections



**Figure 2. CS5505/6 and CS5507/8 Pin Layouts**

CONV signal to transition low to high. This latches the A0 and A1 channel selection into the converter. With CONV high (S2-3 open) the converter will convert continuously.

Figures 3 and 4 illustrate the evaluation board layout while Figure 5 illustrates the component placement (silkscreen) of the evaluation board.

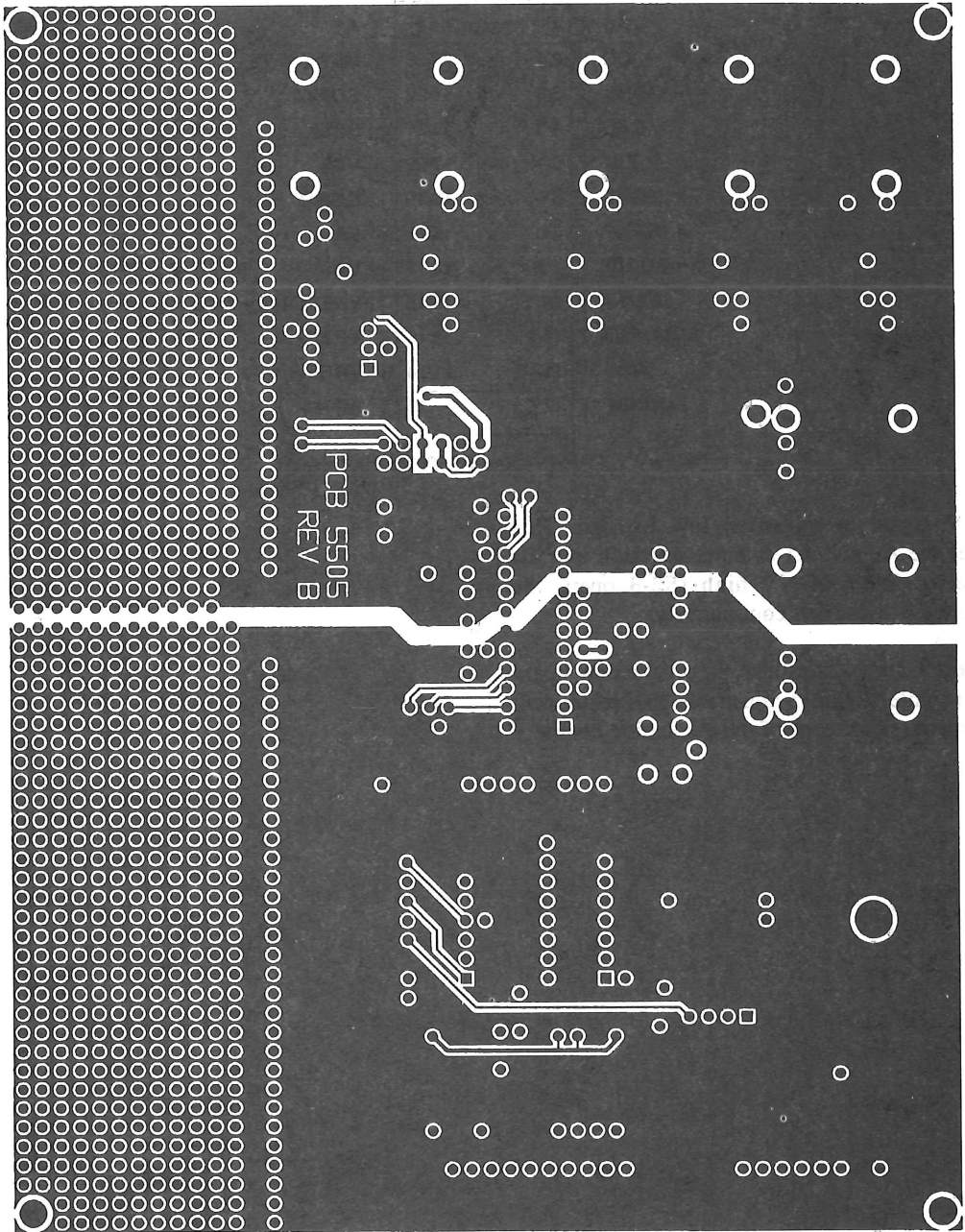
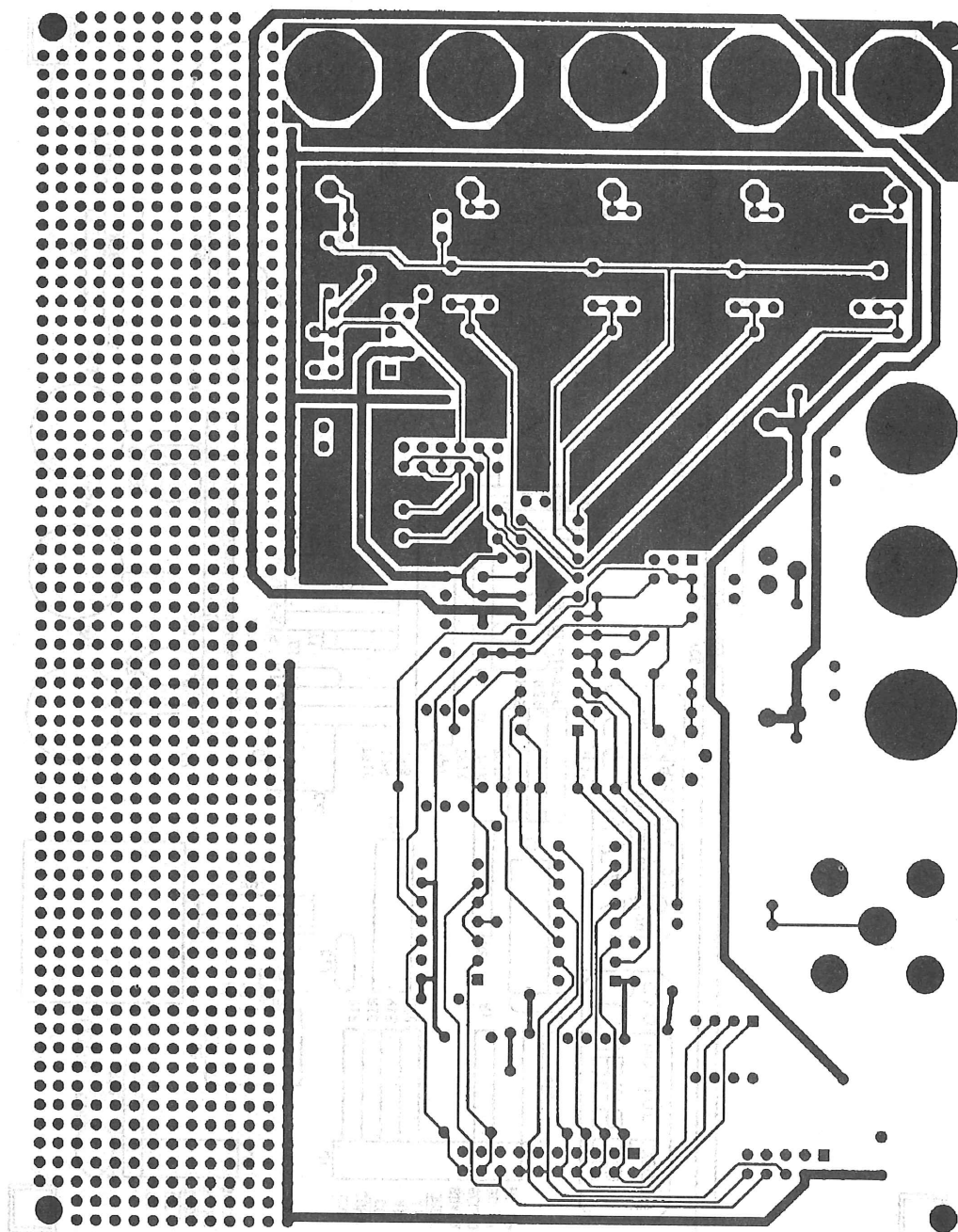


Figure 3. Top Ground Plane Layer (NOT TO SCALE)





3

Figure 4. Bottom Trace Layer (NOT TO SCALE)



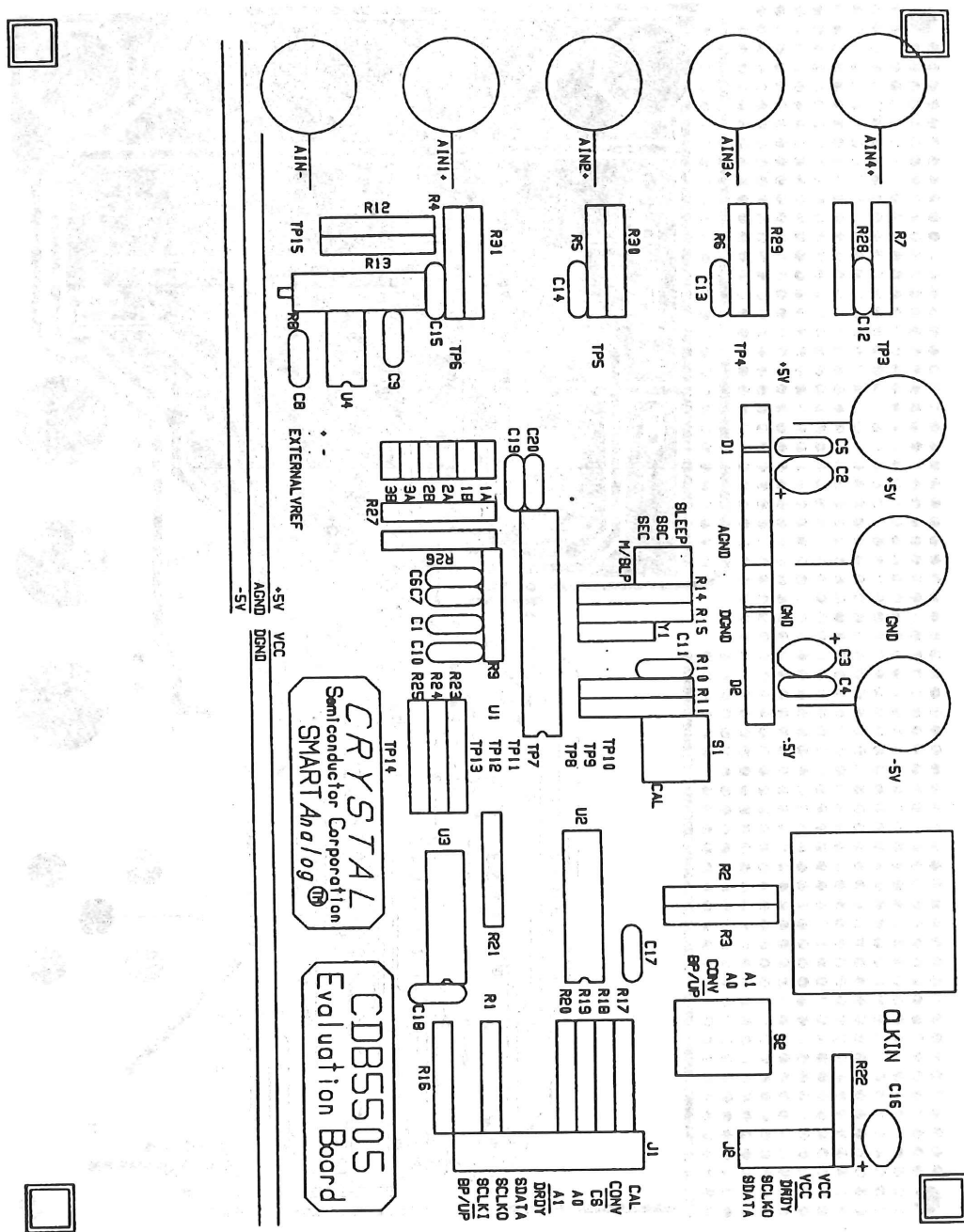


Figure 5. Silk Screen Layer (NOT TO SCALE)

## 16-Bit/20-Bit Bridge Transducer A/D Converters

### Features

- On-chip Instrumentation Amplifier
- On-chip Programmable Gain Amplifier
- On-Chip 4-Bit D/A For Offset Removal
- Dynamic Excitation Options
- Linearity Error:  $\pm 0.0015\%$  FS Max  
Offset and Full-Scale Errors:  $\pm 8$  LSB<sub>20</sub>  
20-Bit No Missing Codes
- CMRR at 50 / 60Hz >200dB
- System Calibration Capability with calibration read/write option
- 3, 4 or 5 wire Serial Communications Port
- Low Power Consumption: under 30mW  
10 $\mu$ W Standby Mode for Portable applications

### General Description

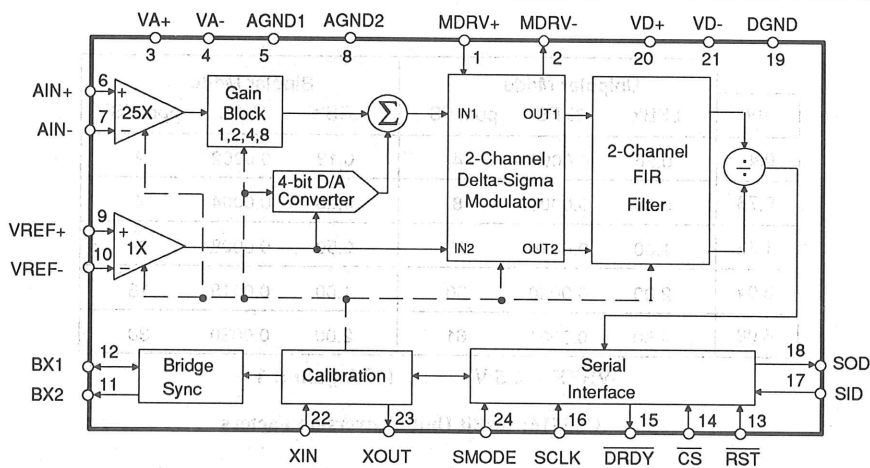
The CS5516 and CS5520 are complete solutions for digitizing low level signals from strain gauges, load cells, and pressure transducers. Any family of mV output transducers, including those requiring bridge excitation, can be interfaced directly to the CS5516 or CS5520. The devices offer an on-chip software programmable instrumentation amplifier block, choice of DC or AC bridge excitation, and software selectable reference and signal demodulation.

The CS5516 uses delta-sigma modulation to achieve 16-bit resolution at output word rates up to 60Hz. The CS5520 achieves 20-bit resolution at word rates up to 60Hz.

The CS5516 and CS5520 sample at a rate set by the user in the form of either an external CMOS clock or a crystal. On-chip digital filtering provides rejection of all frequencies above 12Hz for a 4.096 MHz clock.

The CS5516 and CS5520 include system calibration to null offset and gain errors in the input channel. The digital values associated with the system calibration can be written to, or read from, the calibration RAM locations at any time via the serial communications port. The 4-bit DC offset D/A converter, in conjunction with digital correction, is initially used to zero the input offset value.

**ORDERING INFORMATION:** Page 3-359



### Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation  
P.O. Box 17847, Austin, TX 78760  
(512) 445-7222 : Fax (512) 445-7581

APR '92  
DS74PP2  
3-329

**ANALOG CHARACTERISTICS** ( $T_A = T_{MIN}$  to  $T_{MAX}$ ;  $V_{A+}, V_{D+} = 5V$ ;  $V_{A-}, V_{D-} = -5V$ ;  $V_{REF} = 2.5V$ (external differential voltage across  $V_{REF+}$  and  $V_{REF-}$ );  $f_{CLK} = 4.9152$  MHz; AC Excitation 300 Hz; Gain = 25; Bipolar Mode;  $R_{source} = 300\Omega$  with a 4.7nF to AGND at AIN (see Note 1); unless otherwise specified.)

Parameter *		CS5516-A			CS5516-S			Units
		Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range		-40 to +85			-55 to +125			°C
Accuracy								
Linearity Error		0.0015 0.003			0.0015 0.003			±%FS
Differential Nonlinearity		±0.25 ±0.5			±0.25 ±0.5			LSB <sub>16</sub>
Unipolar Gain Error (Note 2)		±1 TBD			±1 TBD			LSB <sub>16</sub>
Bipolar Gain Error (Note 2)		±1			±1			LSB <sub>16</sub>
Unipolar/Bipolar Gain Drift		±1			±1			ppm/°C
Unipolar Offset (Note 2)		±1 TBD			±1 TBD			LSB <sub>16</sub>
Bipolar Offset (Note 2)		±1 TBD			±1 TBD			LSB <sub>16</sub>
Offset Drift		±0.005			±0.005			µV/°C
Noise (Referred to Input)		Gain = 25 (25 x 1)			250			nVrms
		Gain = 50 (25 x 2)			200			nVrms
		Gain = 100 (25 x 4)			150			nVrms
		Gain = 200 (25 x 8)			150			nVrms

- Notes: 1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the source impedance requirements of the CS5516 and CS5520.  
2. Applies after system calibration at the temperature of interest.

µV	Unipolar Mode			Bipolar Mode		
	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
0.4	0.26	0.0004	4	0.13	0.0002	2
0.76	0.50	0.0008	8	0.26	0.0004	4
1.52	1.00	0.0015	15	0.50	0.0008	8
3.04	2.00	0.0030	30	1.00	0.0015	15
6.08	4.00	0.0061	61	2.00	0.0030	30

VREF = 2.5 V

PGA gain = 1

CS5516; 16-Bit Unit Conversion Factors

\* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

## ANALOG CHARACTERISTICS (Continued)

Parameter*	CS5520-B		CS5520-S		Units	
	Min	Typ	Max	Min		Typ
Specified Temperature Range	-40 to +85		-55 to +125		°C	
<b>Accuracy</b>						
Linearity Error	0.0007 0.0015		0.0015 0.003		±%FS	
Differential Nonlinearity (No Missing Codes)	20		20		Bits	
Unipolar Gain Error (Note 2)	±16 TBD		±16 TBD		LSB <sub>20</sub>	
Bipolar Gain Error (Note 2)	±8		±8		LSB <sub>20</sub>	
Unipolar/Bipolar Gain Drift	±1		±1		ppm/°C	
Unipolar Offset (Note 2)	±16 ±TBD		±16 TBD		LSB <sub>20</sub>	
Bipolar Offset (Note 2)	±16 TBD		±16 TBD		LSB <sub>20</sub>	
Offset Drift	±0.005		±0.005		μV/°C	
Noise (Referred to Input)	Gain = 25 (25 x 1)	250		250		nVrms
	Gain = 50 (25 x 2)	200		200		nVrms
	Gain = 100 (25 x 4)	150		150		nVrms
	Gain = 200 (25 x 8)	150		150		nVrms

3

uV	Unipolar Mode			Bipolar Mode		
	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
0.025	0.26	0.0000238	0.25	0.13	0.0000119	0.125
0.047	0.50	0.0000477	0.50	0.26	0.0000238	0.25
0.095	1.00	0.0000954	1.0	0.50	0.0000477	0.5
0.190	2.00	0.0001907	2.0	1.00	0.0000954	1.0
0.380	4.00	0.0003814	4.0	2.00	0.0001907	2.0

VREF = 2.5 V PGA gain = 1

CS5520; 20-Bit Unit Conversion Factors

\* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

**ANALOG CHARACTERISTICS** (Continued)

Parameter		CS5516-A CS5520-B			CS5516-S CS5520-S			Units
		Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range		-40 to +85			-55 to +125			°C
<b>Analog Input</b>								
Analog Input Range:	Unipolar Bipolar	12.5, 25, 50, 100 ±12.5, ±25, ±50, ±100			12.5, 25, 50, 100 12.5, ±25, ±50, ±100			mV mV
Common Mode Rejection:	dc	165			165			dB
	50,60 Hz	200			200			dB
Input Capacitance		5			5			pF
Input Bias Current	(Note 1)	100			100			pA
<b>Instrumentation Amplifier</b>								
Gain		25			25			
Bandwidth		200			200			kHz
Unity Gain Bandwidth		5			5			MHz
Output Slew Rate		1.5			1.5			V/μsec
Noise @ 10 Hz BW		100			100			nVrms
PSRR @ 50/60 Hz	(Note 3)	120			120			dB
Common Mode Range	(Note 4)	±3			±3			V
Chopping Frequency		XIN/128			XIN/128			Hz
<b>Programmable Gain Amplifier</b>								
Gain Tracking	(Note 5)	±1			±1			%
<b>4-Bit Offset Trim DAC</b>								
Accuracy		±5			±5			%
<b>Voltage Reference Input</b>								
Range	(Note 6)	2.0	2.5	3.8	2.0	2.5	3.8	V
Common Mode Rejection:	dc	165			165			dB
	50,60 Hz	200			200			dB
Input Capacitance		15			15			pF
Input Bias Current	(Note 1)	100			100			pA

Notes: 3. This includes the on-chip digital filtering.

4. The maximum magnitude of the differential input voltage,  $V_{diff(in)}$  is determined by the following:  
 $V_{diff(in)} < 300 \text{ mV} - |V_{cm}/12.5|$

$V_{cm}$  is the common mode voltage which is applied to the instrumentation amplifier inputs.

The above equations should be used to calculate the allowable common mode voltage for a given differential voltage applied to the first gain stage inputs.

These limits ensure that the instrumentation amplifier does not saturate.

5. Gain tracking accuracy can be significantly improved by uploading a calibrated gain word to the gain register for each PGA gain selection.

6. The common mode voltage on the Voltage Reference Input, plus the reference range,  $[(V_{REF+}) - (V_{REF-})]/2$ , must not exceed ±3 volts.

## ANALOG CHARACTERISTICS (Continued)

Parameter		Min	Typ	Max	Min	Typ	Max	Units
<b>Modulator Differential Voltage Reference</b>								
Nominal Output Voltage		(MDRV+) - 3.75			(MDRV+) - 3.75			V
Initial Output Voltage Tolerance		100			100			mV
Temperature Coefficient		100			TBD			ppm/°C
Line Regulation (4.75V < VA < 5.25V)		1			1			mV/Volt
Output Voltage Noise 0.1 to 15 Hz		10			10			μVp-p
Output Current Drive:	Source Current	20			20			μA
	Sink Current	20			20			μA
<b>Power Supplies</b>								
DC Power Supply Currents:	IA+	2.5	TBD		2.5	TBD		mA
	IA-	2.5	TBD		2.5	TBD		mA
	ID+	0.5	TBD		0.5	TBD		mA
	ID-	0.1	TBD		0.1	TBD		mA
Power Dissipation: (Note 7)	Normal Operation	28	TBD		28	TBD		mW
	Standby Mode	10	TBD		10	TBD		μW
Power Supply Rejection:	Positive Supplies	90			90			dB
	Negative Supplies	90			90			dB
<b>System Calibration Specifications</b>								
Positive Full Scale Calibration Range (Note 8)	Unipolar Mode				0.8T	1.2T		V
	Bipolar Mode				0.8T	1.2T		V
Maximum Offset Calibration Range (Note 8)	Unipolar Mode				-2T	+2T		V
	Bipolar Mode				-2T	+2T		V
Differential Input Voltage Range (Notes 8, 9, 10)	Unipolar Mode				Voffset + (1.2T)			V
	Bipolar				Voffset ± (1.2T)			V

Notes: 7. All outputs unloaded. All inputs CMOS levels.

8.  $T = VREF / (G \times 25)$ , where T is the full scale span, where VREF is the differential voltage across VREF+ and VREF- in volts, and G is the gain setting of the second gain block. G can be set to 1, 2, 4, 8. This sets the overall gain to 25, 50, 100, 200. The gain can then be fine tuned by using the calibration of the full scale point.

9. When calibrated.

10. Voffset is the offset corrected by the offset calibration routine. Voffset may be as large as 2T.

## DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Modulator Sampling Frequency	$f_s$	$f_{clk}/256$	Hz
Output Update Rate	$f_{out}$	$f_{clk}/81,920$	Hz
Filter Corner Frequency	$f_{-3dB}$	$f_{clk}/341,334$	Hz
Settling Time to $\pm 0.0007\%$ (FS Step)	$t_s$	$6/f_{out}$	s

## DIGITAL CHARACTERISTICS

( $T_A = T_{min}$  to  $T_{max}$ ;  $V_{A+}, V_{D+} = 5V \pm 5\%$ ;  $V_{A-}, V_{D-} = -5V \pm 5\%$ ;  $DGND = 0$ ). All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage: XIN	$V_{IH}$	4.5			V
All Pins Except XIN	$V_{IH}$	2.0			V
Low-Level Input Voltage XIN	$V_{IL}$			0.5	V
All pins Except XIN	$V_{IL}$			0.8	V
High-Level Output Voltage (Note 11)	$V_{OH}$	$(V_{D+}) - 1.0$			V
Low Level Output Voltage $I_{out} = 1.6mA$	$V_{OL}$			0.4	V
Input Leakage Current	$I_{in}$		1	10	$\mu A$
3-State Leakage Current	$I_{OZ}$			$\pm 10$	$\mu A$
Digital Output Pin Capacitance	$C_{out}$		9		pF

11.  $I_{out} = -100 \mu A$ . This guarantees the ability to drive one TTL load. ( $V_{OH} = 2.4V @ I_{out} = -40 \mu A$ ).



### RECOMMENDED OPERATING CONDITIONS ( DGND = 0V, see Note 12.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	4.5	5.0	5.5	V
Negative Digital	VD-	-4.5	-5.0	-5.5	V
Positive Analog	VA+	4.5	5.0	5.5	V
Negative Analog	VA-	-4.5	-5.0	-5.5	V
Differential Analog Reference Voltage	(VREF+)-(VREF-)	2.0	2.5	3.8	V
Analog Input Voltage: (Note 13)					
Unipolar	VAIN	0		+T	V
Bipolar	VAIN	-T		+T	V

Notes: 12. All voltages with respect to ground.

13. The CS5516 and CS5520 can accept input voltages up to +T in unipolar mode and -T to +T in bipolar mode where  $T = VREF/(G \times 25)$ . G is the gain setting at the second gain block. When the inputs exceed these values, the CS5516 and CS5520 will output positive full scale for any input above T, and negative full scale for inputs below AGND in unipolar and -T in bipolar mode. This applies when the analog input does not exceed  $\pm 2T$  overrange..

3

### ABSOLUTE MAXIMUM RATINGS\*

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:					
Digital Ground (Note 14)	DGND	-0.3		(VA+)+0.3	V
Positive Digital (Note 15)	VD+	-0.3		(VA+)+0.3	V
Negative Digital	VD-	-0.3		-5.5	V
Positive Analog	VA+	-0.3		5.5	V
Negative Analog	VA-	+0.3		-5.5	V
Input Current, Any Pin Except Supplies (Notes 16, 17)	$I_{in}$			$\pm 10$	mA
Analog Input Voltage AIN and VREF pins	VINA	(VA-)-0.3		(VA+)+0.3	V
Digital Input Voltage	VIND	-0.3		(VD+)+0.3	V
Ambient Operating Temperature	$T_A$	-55		125	°C
Storage Temperature	$T_{stg}$	-65		150	°C

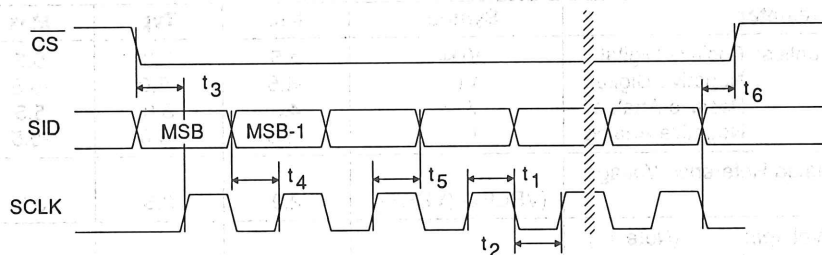
Notes: 14. No pin should go more positive than (VA+)+0.3V.

15. VD+ must always be less than (VA+)+0.3 V, and can never exceed 6.0V.

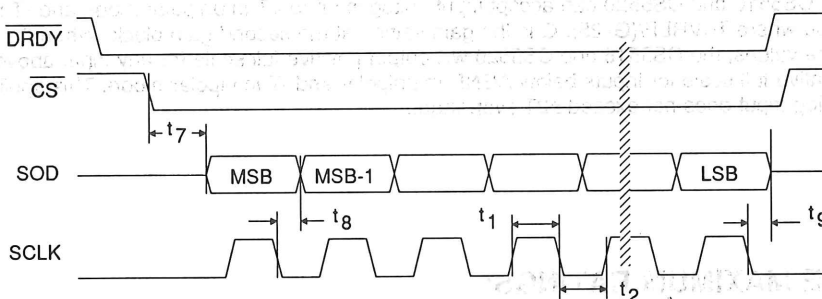
16. Applies to all pins including continuous overvoltage conditions at the analog input pins.

17. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is  $\pm 50$  mA.

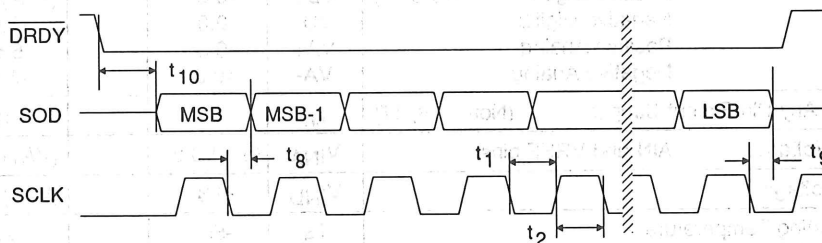
\* WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.



**SID Write Timing (Not to Scale)**



**SOD Read Timing (Not to Scale)**



**SOD Read Timing with  $\overline{CS} = 0$  (Not to Scale)**



**$\overline{CS}$  with Continuous SCLK (Not to Scale)**

**SWITCHING CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ;  $V_{A+}, V_{D+} = 5V \pm 5\%$ ;  
 $V_{A-}, V_{D-} = -5V \pm 5\%$ ; Input Levels: Logic 0 = 0V, Logic 1 =  $V_{D+}$ ;  $C_L = 50$  pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock frequency:	Internal Oscillator:	XIN or f <sub>clk</sub>	1.0	4.096	5.0 MHz
	External Clock:	TBD	4.096	5.0	MHz
Master Clock Duty Cycle		40		60	%
Rise Times: (Note 18)	Any Digital Input	t <sub>rise</sub>		1.0	μs
	Any Digital Output		50		ns
Fall Times: (Note 18)	Any Digital Input	t <sub>fall</sub>		1.0	μs
	Any Digital Output		50		ns
<b>Start-Up</b>					
Power-on Reset Period	t <sub>por</sub>		100		ms
Oscillator Start-up Time XTAL = 4.9152 MHz (Note 19)	t <sub>ost</sub>		60		ms
RST Pulse Width	t <sub>res</sub>	1/XIN			ns
<b>Serial Port Timing</b>					
Serial Clock Frequency	SCLK			2.4	MHz
Serial Clock	Pulse Width High	t <sub>1</sub>	200		ns
	Pulse Width Low	t <sub>2</sub>	200		ns
<b>SID Write Timing</b>					
$\overline{CS}$ Enable to Valid Latch Clock	t <sub>3</sub>	150			ns
Data Set-up Time prior to SCLK rising	t <sub>4</sub>	50			ns
Data Hold Time After SCLK Rising	t <sub>5</sub>	50			ns
SCLK Falling Prior to $\overline{CS}$ Disable	t <sub>6</sub>	50			ns
<b>SOD Read Timing</b>					
$\overline{CS}$ to Data Valid	t <sub>7</sub>			150	ns
SCLK Falling to New Data Bit	t <sub>8</sub>			150	ns
SCLK Falling to SOD Hi-Z	t <sub>9</sub>			150	ns
DRDY Falling to Valid Data ( $\overline{CS} = 0$ )	t <sub>10</sub>			150	ns
$\overline{CS}$ Rising to SOD Hi-Z	t <sub>11</sub>			150	ns
$\overline{CS}$ Disable Hold Time	t <sub>12</sub>	50			ns
$\overline{CS}$ Enable Set-up Time	t <sub>13</sub>	150			ns
$\overline{CS}$ Enable Hold Time	t <sub>14</sub>	50			ns
$\overline{CS}$ Disable Set-up Time	t <sub>15</sub>	150			ns

Notes: 18. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

19. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

## GENERAL DESCRIPTION

The CS5516 and CS5520 are monolithic CMOS A/D converters which include an instrumentation amplifier input, an on-chip programmable gain amplifier, and a DAC for offset trimming. While the devices are optimized for ratiometric measurement of Wheatstone bridge applications, they can be used for general purpose low level signal measurement.

Each of the devices includes a two-channel differential delta-sigma modulator (the signal measurement input and the reference input are digitized independently before a digital output word is computed), a calibration microcontroller, a two-channel digital filter, a programmable instrumentation amplifier block, a 4 bit DAC for

coarse offset trimming, circuitry for generation and demodulation of AC (actually switched DC) bridge excitation, and a serial port. The CS5516 outputs 16-bit words; the CS5520 outputs 20-bit words.

The CS5516/20 devices can measure either unipolar or bipolar signals. Self-calibration is utilized to maximize performance of the measurement system. To better understand the capabilities of the CS5516/20, it is helpful to examine some of the error sources in bridge measurement systems.

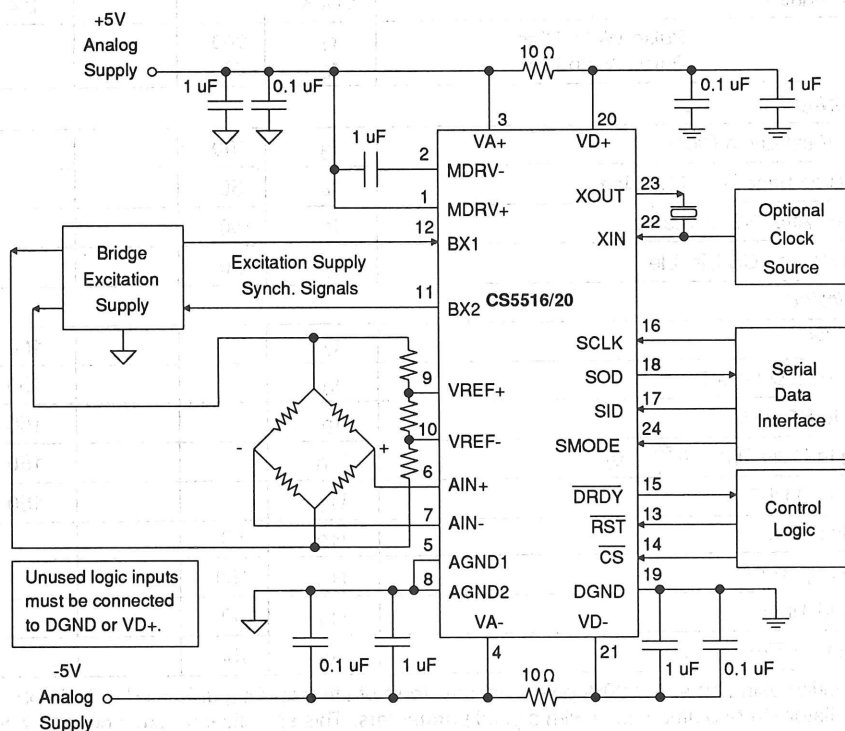


Figure 1. System Connection Diagram: AC Excitation Mode Using External Excitation

### ENEMIES OF THE STRAIN GAUGE

The CS5516 and CS5520 address many common error sources encountered when digitizing bridge transducers. The following sections describe these error sources and the CS5516/20 features which allow for their control.

#### IR Drops

Strain gauges are low impedance devices (300Ω typical) and the bridge may be connected to the excitation source by long wires ( $R_{p1}$  and  $R_{p2}$ ). This situation is illustrated in Figure 2.

Resistors  $R_{p1}$  and  $R_{p2}$  change the gain of the bridge,  $A_v$ :

$$A_v = \frac{(A_{IN+}) - (A_{IN-})}{(V_{EXC+}) - (V_{EXC-})} \quad (1)$$

Gauges are often purchased including interconnection cables, allowing errors due to  $R_{p1}$  and  $R_{p2}$  to be included in the gauge manufacturer's specification.

$R_{p1}$  and  $R_{p2}$  include parasitic resistances of copper wire and various interconnections. These parasitics will not track the gauge resistance over temperature, and  $A_v$  will drift as a result. Generally, a gauge with a lower  $A_v$  drift will be more expensive.

A six-wire gauge allows for force and sense (Kelvin connection) of the excitation voltage. This allows all errors due to  $R_{p1}$  and  $R_{p2}$  to be removed by the ratiometric conversion of the CS5516/20. Figure 3 illustrates the solution.

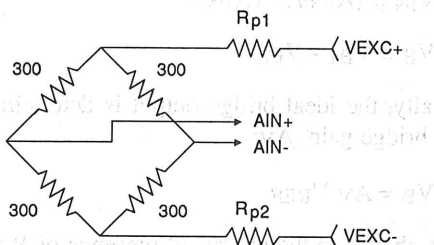


Figure 2. Four-Wire Bridge

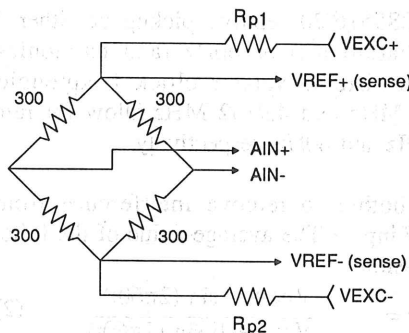


Figure 3. Six-Wire Bridge

Since the VREF inputs to the CS5516/20 provide very high impedance, no IR drops occur in the sense lines.

#### Pan Weight Offsets

Measuring zero weight in practice means measuring the weighing pan or surface itself. When the pan alone is measured, the bridge produces a differential output at AIN+ and AIN-.

At first glance, the CS5516's and CS5520's ratiometric offset calibration allows for easy removal of pan weight offsets. But the CS5516/20 is even more powerful than that. The internal 4-bit digital-to-analog converter allows for the removal of up to  $\pm 200\%$  of the selected range's full scale, avoiding loss of resolution due to pan weight offsets.

Of critical importance here is the feature that the pan weight subtraction automatically scales with VREF+ and VREF-. Ratiometric, non-reference-sensitive operation is preserved even when the pan weight removal DAC is utilized.

#### 50Hz/60Hz Pickup

Twisted pair interconnections should always be used to minimize 50/60Hz pickup into the VREF+, VREF- and AIN+, AIN- pairs. None the less, some 60Hz pickup into these pairs is inevitable.

The CS5516/20 remove pickup at either 50Hz (and harmonics) or 60Hz (and harmonics) by digital filters. Master clock frequencies of 4.096 MHz and 4.9152 MHz allow for removal of 50Hz and 60Hz, respectively.

Why bother to remove interference from the VREF input? The average value of the following expression:

$$V_{OUT} = \frac{V_{IN} + \alpha \sin(2\pi 60t)}{V_{REF} + \beta \sin(2\pi 60t)} \quad (2)$$

is NOT equal to  $V_{IN}/V_{REF}$ , so dc measurement errors result.

The CS5516 and CS5520 are different from most ADC systems because they convert both AIN and VREF with respect to an independent internal reference. Digital filters first remove the 50Hz and 60Hz (and harmonics). Then, and only then, is AIN ratioed to VREF. The result is significantly improved robustness when operating in harsh 50/60Hz environments.

#### Radio Frequency Interference (RFI)

The narrowband digital filters of the CS5516/20 also provide improved ADC performance in the presence of RFI. Just as 60Hz ac pickup into a traditional ADC reference input can cause shifts in the mean ADC output, RFI can produce the same effect.

The digital lowpass filters of the CS5516/20 remove all interference EXCEPT that present in narrow frequency bands centered around multiples of  $f_{CLK}/256$ , where  $f_{CLK}$  is the master clock to the converter. The delta-sigma modulator provides additional filtering at odd multiples of  $f_{CLK}/256$  and  $f_{CLK}/128$ . The converter passband is illustrated on a linear frequency scale in Figure 4.

If RFI energy is present on AIN or VREF at multiples of  $f_{CLK}/64$ , analog antialiasing filters should be evaluated for RFI control.

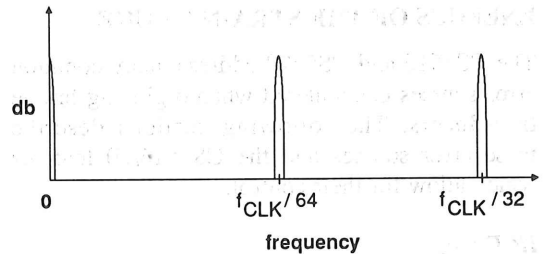


Figure 4. Filter Passband

#### Non-ratiometric Errors

For strain gauges operated with dc excitation voltages, voltage and current offsets impair measurement accuracy. The first such offset considered is shown as  $V_{OS}$  in Figure 5.

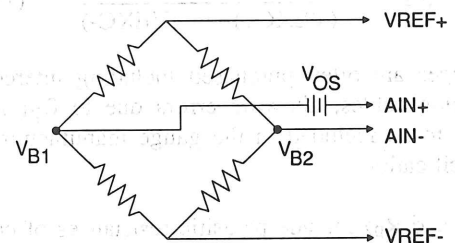


Figure 5. Vos Offset

The fixed offset voltage obviously produces a signal at AIN+ and AIN- that does not scale with the excitation voltage; hence, the name "non-ratiometric error". Let's examine the significance of these errors with a little algebra. First, for convenience, let:

$$V_{REF} \equiv (V_{REF+}) - (V_{REF-}) \quad (3)$$

$$V_{IN} \equiv (A_{IN+}) - (A_{IN-}) \quad (4)$$

$$V_B \equiv V_{B1} - V_{B2} \quad (5)$$

Finally, the ideal bridge output is determined by the bridge gain,  $A_V$ :

$$V_B = A_V V_{REF} \quad (6)$$

But, thanks to the unwanted presence of  $V_{OS}$ ,

$$V_{IN} = A_V V_{REF} + V_{OS} \quad (7)$$

If the strain gauge ADC were perfectly ratiometric, its digital output would represent:

$$V_{OUT} = V_{IN}/V_{REF} = A_V + V_{OS}/V_{REF} \quad (8)$$

When  $V_{OS} \neq 0$ , the value of  $V_{OUT}$  depends on  $V_{REF}$ . The sensitivity,  $S_1$ , is given by:

$$S_1 \equiv \frac{\delta V_{OUT}/V_{OUT}}{\delta V_{REF}/V_{REF}} = \frac{-V_{OS}}{A_V V_{REF} + V_{OS}} \quad (9)$$

Some practical values illustrate the significance of equation 9. Suppose  $A_V = 0.002$ , (2mV/volt sensitivity),  $V_{REF} = 10V$ , and  $V_{OS} = 100 \mu V$ . Then,  $S_1 \approx 5E-3$ , implying a 10% change in  $V_{REF}$  will cause a  $S_1 \times 10\% = 0.05\%$  change in  $V_{OUT}$ . A significant error indeed at the 16-bit level.

Equation 9 suggests three methods for reducing these non-ratiometric errors:

- 1) Buy a gauge with large  $A_V$ .
- 2) Use a large  $V_{REF}$ .
- 3) Measure  $V_{OS}$ , calibrate it out, and eliminate the problem.

The non-ratiometric offset calibration modes of the CS5520 make item #3 quite simple.

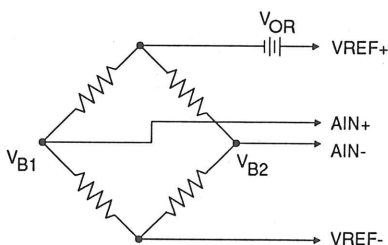


Figure 6.  $V_{OR}$  Offset

A second non-ratiometric error source is illustrated in Figure 6. The offset  $V_{OR}$  is picked up in the reference sense line. Thus,

$$V_B = A_V (V_{REF} - V_{OR}) \quad (10)$$

$$V_{OUT} = A_V - (A_V V_{OR})/V_{REF} \quad (11)$$

The sensitivity,  $S_2$  is given by:

$$S_2 \equiv \frac{\delta V_{OUT}/V_{OUT}}{\delta V_{REF}/V_{REF}} = \frac{-V_{OR}}{V_{REF} - V_{OR}} \quad (12)$$

Not surprisingly, in this case increasing  $A_V$  doesn't help. Using the values of the previous example,  $S_2 \approx 1E-5$ .

Sensitivities  $S_1$  and  $S_2$  simply confirm that, when non-ratiometric errors ( $V_{OS}$  and  $V_{OR}$ ) are non-zero, THE OUTPUT MEASUREMENT WILL VARY WITH VOLTAGE REFERENCE. A zero tempco, zero aging, perfect line regulation reference can avoid this variation, but one major advantage of ratiometric measurement techniques should be that no precise, stable reference is necessary.

The non-ratiometric offset and gain calibrations allow the user to "zero-out" the bridge excitation voltage and measure  $V_{OS}$  and  $V_{OR}$ , respectively. The voltages measured during this calibration step are subtracted from their respective inputs prior to the digital ratiometric operation. This calibration step can be performed whenever desired and contributes to the robustness of the CS5516/20 measurement system.

### Thermocouples

A common source of non-ratiometric error is parasitic thermocouples. The differential reference and analog input paths should keep such thermocouples common mode. Route differential inputs next to each other, use low thermal emf interconnections and relays, etc. While perfectly matched thermocouple chains produce zero differential inputs, thermal gradients exist in any "real world" measurement system. Temperature-dependent non-ratiometric offsets result.

Use of non-ratiometric offset calibrations can substantially reduce thermocouple errors. None-



theless, temperature gradient fluctuations are difficult to eliminate.

AC excitation, shown in Figure 7, alternately flips the excitation voltages at the top and bottom of the bridge.

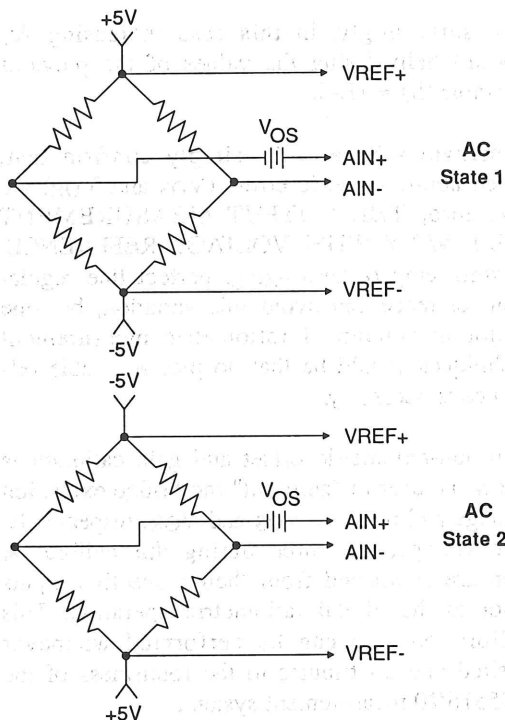


Figure 7. AC Excitation

With ac excitation, the desired signal  $V_B$  flips in polarity as the excitation voltage flips. The analog input becomes a square wave at the excitation frequency.  $V_{OS}$  doesn't flip. When the CS5516/20 synchronously demodulates the square wave in ac excitation mode,  $V_{OS}$  is modulated up into the digital filter's rejection band.  $V_{OS}$  problems are just filtered away.

Any systems designs that can exploit the benefits of ac excitation probably should. Accuracy fluctuations with temperature can be virtually eliminated. Any remaining non-ratiometric errors

can still be attacked with non-ratiometric calibrations when ac excitation is used. The CS5516/20's BX1 and BX2 pins provide for both internally and externally controlled excitation signals.

### Offsets due to leakages

Moisture or other contaminants in load cell cables or on the printed circuit board can cause current leakage paths, one of which is illustrated in Figure 8.

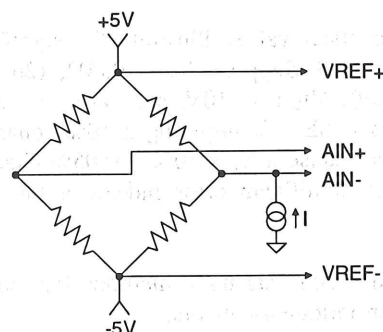


Figure 8. Leakage Effects Offset

The current source model is appropriate since the resistance of the leakage path is often much larger than that of the gauge. Comparison with Figure 7 reveals that both ac excitation and non-ratiometric calibration serve to reduce measurement errors due to these leakage current paths.

## THEORY OF OPERATION

The front page of this data sheet illustrates the block diagram of the CS5516 and CS5520 A/D converter. The device includes an instrumentation amplifier with a fixed gain of 25. This chopper-stabilized instrumentation amplifier is followed by a programmable gain stage with gain settings of 1, 2, 4, and 8. The sensitivity of the input is a function of the programmable gain setting and of the reference voltage connected between the VREF+ and VREF- pins of the device. The full scale sensitivity of the instrumentation amplifier is  $VREF/(G \times 25)$  in unipolar, or  $\pm VREF/(G \times 25)$  in bipolar, where VREF is the reference voltage between the VREF+ and VREF- pins, G is the gain setting of the programmable gain amplifier, and 25 is the gain of the instrumentation amplifier.

After the programmable gain block, the output of a 4-bit DAC is combined with the input signal. The DAC can be used to add or subtract offset from the analog input signal. Offsets as large as  $\pm 200\%$  of full scale can be trimmed from the input signal.

The CS5516 and CS5520 are optimized to perform ratiometric measurement of bridge-type transducers. The devices support dc bridge excitation or two modes of ac (switched dc) bridge excitation. In the switched-dc modes of operation the converter fully demodulates both the reference voltage and the analog input signal from the bridge.

The CS5516/20 includes a microcontroller which manages operation of the chip. Included in the microcontroller are eight different registers as-

3

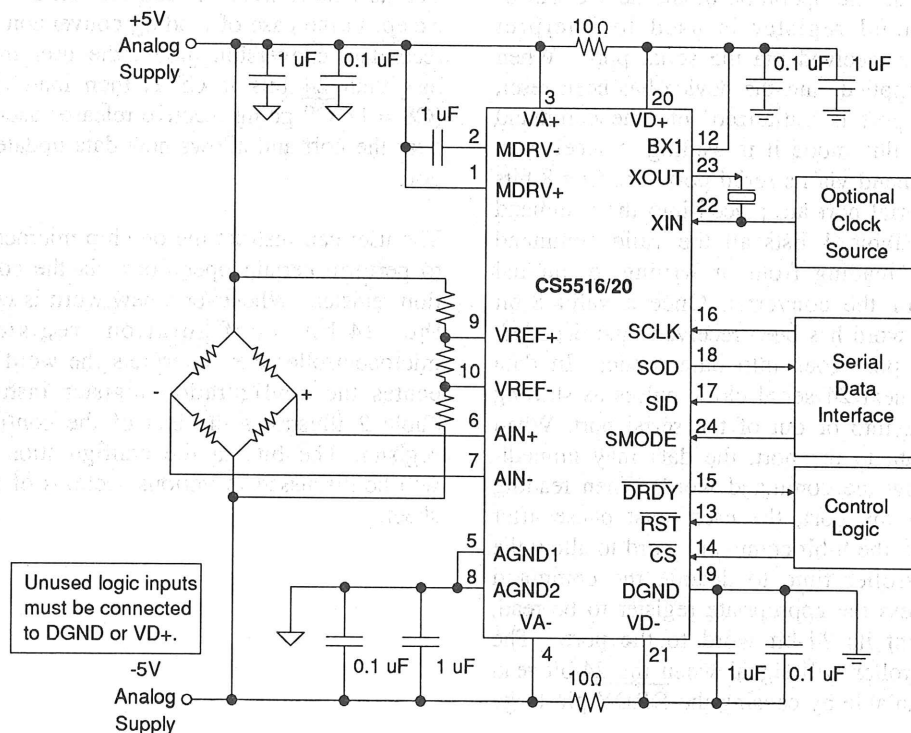


Figure 9. System Connection Diagram: DC Excitation Mode (EXC bit = 1)

Register <sup>1</sup>	Read	Write
Conversion Data Register <sup>2</sup>	88(H)	
Configuration Register	98(H)	90(H) <sup>3</sup>
DAC Register	B8(H)	B0(H)
Gain Register	A8(H)	A0(H)
AIN Ratiometric Offset Register	C8(H)	C0(H)
AIN Nonratiometric Offset Register	D8(H)	D0(H)
VREF Nonratiometric Offset Register	E8(H)	E0(H)

- Notes:
1. 24 SCLKs are required to read or write all registers.
  2. CS5516 has 16 data bits, CS5520 has 20 data bits.
  3. The four DAC bits cannot be overwritten by this command.

**Table 1. CS5516 and CS5520 Commands**

sociated with the operation of the device. An 8-bit command register is used to interpret instructions received via the serial port. When power is applied, and the device has been reset, the serial port is initialized into the command mode. In this mode it is waiting to receive an 8-bit command via its serial port. The first 8 bits into the serial port are placed into the command register. Table 1 lists all the valid command words for reading from or writing to internal registers of the converter. Once a valid 8-bit command word has been received and decoded, the serial port goes into data mode. In data mode the next 24 serial clock pulses as shifting data either into or out of the serial port. When writing data to the port, the data may immediately follow the command word. When reading data from the port, the user must pause after clocking in the 8-bit command word to allow the microcontroller time to decode the command word, access the appropriate register to be read, and present its 24-bit word to the port. The microcontroller will signal when the 24-bit read data is available by causing the DRDY pin to go low.

The user must write or read the full 24-bit word except in the case of reading conversion data. In read data conversion mode, the user may read less than 24 bits if CS is then made inactive (CS = 1). CS going inactive releases user control over the port and allows new data updates to the port.

The user can instruct the on-chip microcontroller to perform certain operations via the configuration register. Whenever a new word is written to the 24-bit configuration register, the microcontroller then interprets the word and executes the configuration register instructions. Table 2 illustrates the bits of the configuration register. The bits in the configuration register will be discussed in various sections of this data sheet.

### Configuration Register

#### DAC Bits, bits 23 - 20

23	22	21	20
D3	D2	D1	D0

D3-D0 Offset, increments of 25% of Full Scale  
D3 is sign bit (0 = add offset;  
1 = subtract offset)  
D2 is the MSB, D0 represents 25% F.S.  
e.g. 0001 = +25% F.S.  
0111 = +175% F.S.  
0000 = 0 % F.S.  
1111 = -175% F.S.

Note: The DAC bits can only be written into the DAC register, but can be read via the configuration or DAC register.

#### Bridge Excitation, Bits 19-16

19	18	17	16
EXC	F1	F0	0

EXC Selects external or internal mode.  
1 = External  
0 = Internal

F1-F0 Select Internal mode Frequency  
00 = dc  
10 = XIN/16384 kHz  
01 = XIN/8192 kHz  
11 = XIN/4096 kHz

Bit 16 must be set to a logic 0

#### PGA Gain, Unipolar/Bipolar, Awake/Sleep Bits 15-11

15	14	13	12	11
G1	G0	U/B	0	A/S

G1-G0 Select gain setting  
00 = 1 (x 25)  
10 = 2 (x 25)  
01 = 4 (x 25)  
11 = 8 (x 25)

U/B Unipolar/Bipolar mode select  
1 = Unipolar mode  
0 = Bipolar mode

Bit 12 must be set to a logic 0

A/S Awake/Sleep mode select  
0 = Awake mode  
1 = Sleep mode

#### Execute Calibration and Calibration Control, Bits 10-4

10	9	8	7	6	5	4
EC	0	0	CC3	CC2	CC1	CC0

EC Execute calibration, EC must be set to 1 to execute calibration. See text for explanation of calibration steps.  
Note: EC must be written back to 0 after calibration is completed.

Bits 9 and 8 must be set to 0.

#### CC3-CC0 Calibration Control Bits

1000 = Calibrate non-ratiometric offset, VREF  
0100 = Calibrate non-ratiometric offset, AIN  
0010 = Calibrate ratiometric offset, AIN  
0001 = Calibrate gain, AIN

#### Reset Filter, Bit 0

3	2	1	0
0	0	0	RF

Bits 3 through 1 must be set to 0.

RF 1 = Reset Filter  
0 = Normal Operation

MSB

23	22	21	20	19	18	17	16
D3	D2	D1	D0	EXC	F1	F0	0

15	14	13	12	11	10	9	8
G1	G0	U/B	0	A/S	EC	0	0

7	6	5	4	3	2	1	0
CC3	CC2	CC1	CC0	0	0	0	RF

Bits 16, 9, 8, 3, 2 and 1 must always be logic 0.

Table 2. Configuration Register

## System Initialization

Whenever power is applied to the CS5516/CS5520 A/D converters, the devices must be reset to a known condition before proper operation can occur. The devices include an internal power-on reset function that initializes the internal logic. The internal reset is applied after power is established and lasts for approximately 100 ms. The RST pin can also be used to establish a reset condition. The reset signal should remain low for at least one XIN clock cycle to ensure adequate reset time. It is recommended that the RST pin be used to reset the converter if the power supplies rise very slowly or with poor startup characteristics. The RST signal can be generated by a microcontroller output, or by use of an R-C circuit.

The reset function initializes the configuration register, all five of the calibration registers, and places the microcontroller in command mode ready to accept a command from the serial port. Whenever the device is reset the DRDY pin will be set to a logic 1 and the on-chip registers are initialized to the following states:

Configuration	000000(H)
Calibration registers:	
DAC	0(H)
Gain	800000(H)
AIN Ratiometric Offset	000000(H)
AIN Non-ratiometric Offset	000000(H)
VREF Non-ratiometric Offset	000000(H)

## CALIBRATION

After the CS5516/20 is reset, the device is functional and can perform measurements without being calibrated. The converter will utilize the initialized values of four of the five calibration registers to calculate output words.

The converter uses the two outputs (AIN & VREF) of the dual channel converter along with the contents of the calibration registers to compute the conversion data word. The following equation indicates the computation.

$$R0 = R4 \left[ \frac{DAIN - R1}{DVREF - R2} \right] - R3$$

Where R0 is the output data, DAIN and DVREF are the digital output words from the AIN and VREF digital filter channels, and R1, R2, R3 and R4 are the contents of the following calibration registers:

- R1 = AIN non-ratiometric offset
- R2 = VREF non-ratiometric offset
- R3 = AIN ratiometric offset
- R4 = Gain

The computed output word, R0, is a two's complement number which represents the percentage of full scale signal measured.

Calibration minimizes the errors in the converted output data. If calibration has not been performed, the measurements will include offset and gain errors of the entire system.

The converter may be calibrated each time it is used, or calibration words from a previous calibration may be uploaded into the appropriate calibration registers from some type of E<sup>2</sup>PROM by the system microcontroller.

The converter uses five different registers to store specific calibration information. Each of the calibration registers stores information pertinent to correcting a specific source of error

Configuration Register					CAL Type	Calibration Time
EC	CC3	CC2	CC1	CC0		
1	1	0	0	0	VREF Non-ratiometric Offset	573,440/fclk
1	0	1	0	0	AIN Non-ratiometric Offset	573,440/fclk
1	0	0	1	0	AIN Ratiometric Offset	2,211,840/fclk
1	0	0	0	1	AIN System Gain	573,440/fclk
1	1	1	0	0	VREF & AIN Non-Ratiometric Offset	573,440/fclk
0	X	X	X	X	End Calibration	-

DRDY remains high through calibration sequence. In all modes, DRDY falls immediately upon completion of the calibration sequence.

Table 3. CS5516/CS5520 Calibration Control

associated with either the converter or with the input transducer and its wiring. The method by which calibration is initiated is common to each of the calibration registers. The configuration register controls the execution of the calibration process. Bits CC3--CC0 in the configuration register determine which type of calibration will be performed and which of the five calibration registers will be affected. To execute a calibration will require that one of the bits (CC3--CC0) be set to a logic 1 to select the type of calibration to be performed. The EC bit of the same 24-bit configuration word is also set to a logic 1. On the falling edge of the 24th SCLK, the configuration word will be latched into the configuration register and the selected calibration will be executed. The time required to perform a calibration is listed in Table 3. The DRDY pin will remain a logic 1 during calibration, and will go low when the calibration step is completed.

The serial port should remain inactive while a calibration is in progress. The EC bit of the configuration register remains a logic 1 until it is overwritten by a new configuration word (EC = 0). Consequently, if EC is left active, any write (the falling edge of the 24th SCLK) to any register inside the converter will cause a re-execution of the calibration sequence. This occurs because the internal microcontroller executes the contents of the configuration register every time the 24th SCLK falls after writing a 24-bit word

to any internal register. To be certain that calibrations will not be re-executed each time a new word is written or read via the serial port, the EC bit of the configuration register must be written back to a logic 0 after the final calibration step has been completed.

The CC3--CC0 bits of the configuration register determine the type of calibration to be performed. The order in which the calibration steps are performed is important. A proper calibration sequence of all calibration steps should be performed in the following sequence. First, the non-ratiometric offset errors of the VREF and AIN input channels should be calibrated. Then the ratiometric offset of the AIN channel should be calibrated. And finally, the AIN channel gain should be calibrated.

To calibrate out the VREF and AIN non-ratiometric errors, the input channels to the VREF path into the converter and the AIN path into the converter must be grounded (this may occur at the pins of the IC, or at the bridge excitation as shown in Figure 10.). Then the EC, CC2 and CC3 bits of the configuration register must be set to logic 1. The converter will then perform a non-ratiometric calibration and place the proper 24 bit calibration words in the VREF and AIN non-ratiometric registers. Note that the two non-ratiometric offsets can be calibrated simultaneously or independently, but they must

be calibrated prior to the other calibration steps if the user wants to minimize the effect of these non-ratiometric offset errors. If the effects of the non-ratiometric errors are not significant enough to affect the user application, they can be left uncalibrated (after a reset, the non-ratiometric offset registers will contain 000000(H)).

Once the non-ratiometric errors have been calibrated, the ratiometric offset error of the AIN channel should be calibrated next. To perform this calibration step, a reference voltage must be applied to the VREF+ and VREF- pins. Then, place "zero" weight on the scale platform. This will result in an offset voltage into the converter which will represent the offset of the bridge, the wiring, and the AIN input of the converter itself. A configuration word with the EC and CC1 bits set to logic 1 is then written into the configuration register. During the ratiometric offset calibration of AIN the microcontroller first uses a successive approximation algorithm to compute the correct values for the D3-D0 bits of the DAC register. This accommodates any large offsets on the AIN input signal. Once the four DAC bits are computed, this amount of offset is removed from the input signal. The microcontroller then computes the appropriate 24

bit number to place in the AIN ratiometric offset register to calibrate out the remaining offset not removed by the DAC.

After the AIN ratiometric offset has been calibrated, the next step is to perform a gain calibration. Gain calibration is performed with "full scale" weight on the scale platform. The EC and CC0 bits of the configuration register are set to logic 1. The gain calibration of the AIN channel is the final calibration step. After DRDY falls to signal the completion of this calibration step, the EC bit of the configuration register must be set back to logic 0 to terminate the calibration mode. The calibration word in the gain register spans  $2^{-23}$  to 2 as illustrated.

MSB				LSB		
$2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$	$\cdot \cdot \cdot$	$2^{-22}$	$2^{-23}$

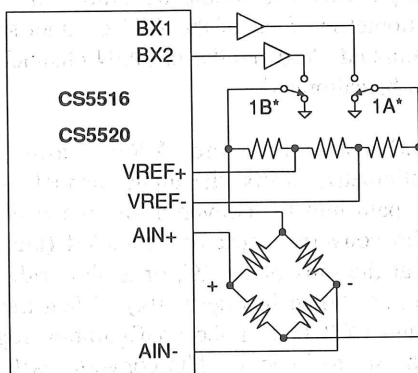
Range is from  $2^{-23}$  to 2

Figure 11. Gain Calibration Range

In a typical weigh scale application, the CS5516/CS5520 will be calibrated in combination with a load cell at the factory. Once calibrated, the calibration words are off-loaded from the converter and stored in E<sup>2</sup>PROM. When powered-up in the field the calibration words are up-loaded into the appropriate registers. This is viable because the AIN and VREF input to the converter are "chopper-stabilized" and maintain excellent stability when subjected to changes in temperature.

### Programmable Gain Amplifier

The programmable gain amplifier inside the CS5516/20 offers gains of 1, 2, 4, and 8. This is in addition to the fixed gain of  $\times 25$  in the input instrumentation amplifier. The gain tracking of the PGA is about one per cent between ranges. The user can remove this error by performing a gain calibration at the factory with a full scale signal on each range. The gain calibration word for each gain range can be off-loaded into E<sup>2</sup>PROM and uploaded into the gain register



\*Note: The bridge can be grounded with a relay or with jumpers to perform non-ratiometric calibration.

Figure 10. Non-ratiometric System Calibration using Internal Excitation



whenever a new gain setting is selected for the PGA. Gain stability over temperature for the converter itself is approximately 1 ppm/°C when the device is used ratiometrically.

### Serial Interface Modes

The CS5516/20 support either 5, 4 or 3 pin serial interfacing. The SMODE pin sets the operating mode of the serial interface. With SMODE = 0, the device assumes the user is operating with either a 5 or 4 wire interface. The five wire mode includes SOD, SID, SCLK, DRDY, and CS. In the four wire mode, CS is connected to DGND as a logic 0. The user would then interface to the SOD, SID, SCLK, and DRDY pins.

Reading a register in the converter requires a command word to be written to the SID pin. For example, to read the conversion data register, the following command sequence should be performed. First, the command word 88(H) would be issued to the port. In the 5 wire interface mode, this would involve activating CS low, followed by 8 SCLKs (note that SCLK must always start low and transition from low to high to latch the transmit data, and then back low again) to input the 8-bit command word. CS must be low for the serial port to recognize SCLKs during a write or a read, but it is actually the first rising SCLK during command time that gives the user control over the port. After writing the command word, the user must pause and wait until the CS5520 presents the selected register data to the serial port. The DRDY signal will fall when the data is available. When reading the conversion data register, it may take up to 112,000 XIN clock cycles for DRDY to fall after the 88(H) command word is recognized. See Figure 12 for an illustration of command and data word timing.

The conversion data register is actually the accumulator of the post-processor which computes the output data. At the end of each filter con-

volution cycle, the internal microcontroller checks to see if a read conversion data register command has been interpreted. If so, it transfers the accumulator result to the serial port.

Whenever registers other than the conversion data register are read, the DRDY pin will fall within 256 XIN clock cycles (62.5  $\mu$ s with XIN = 4.096 MHz) after the command word is recognized. When DRDY falls, 24 SCLKs are then issued to the port to read the 24-bit output data word. DRDY will return high after all 24 bits have been clocked out. The SOD pin will be in a Hi-Z state whenever CS is high, or after all 24 output data bits have been clocked out of the port.

If SMODE = 1 (tied to VD+), the interface operates as a 3 wire interface using only SOD, SID, and SCLK. In the 3 wire mode CS must be tied to DGND. DRDY operates normally but is not used. Instead, the DRDY signal modifies the behavior of the SOD signal, allowing it to signal to the user when data is available. To read data from the converter requires a command word to be written to the SID pin. The SOD output is normally high (never Hi-Z). When output data is available, the SOD signal will go low. The user would then issue 8 SCLKs to the SCLK pin to clear this data ready signal. On the falling edge of the 8th SCLK the SOD pin will present the first bit of the 24 bit output word.

The CS5516/20 is designed such that it can output conversion data words continuously, without issuing a new command word prior to each data read. Under the following circumstances, continuous conversion data can be read from the port after issuing only one 88(H) command word. Once the command to read the conversion data register is issued, DRDY must be allowed to go low, after which 24 SCLKs are issued to read the data. This will cause DRDY to return high.

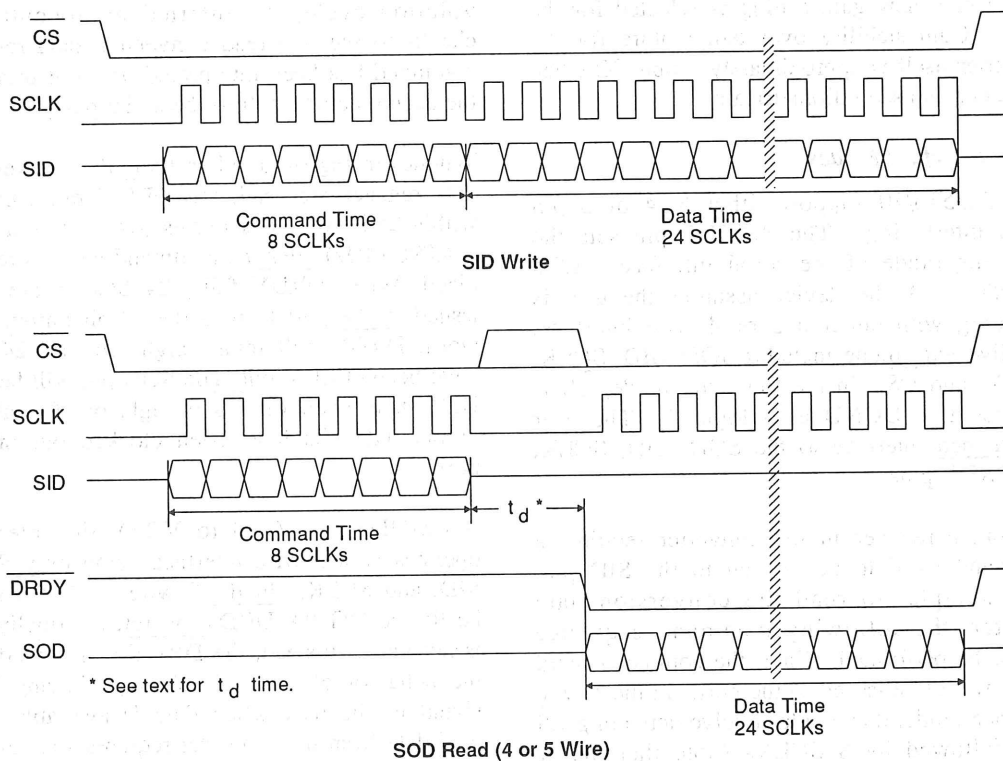


Figure 12. Command and Data Word Timing

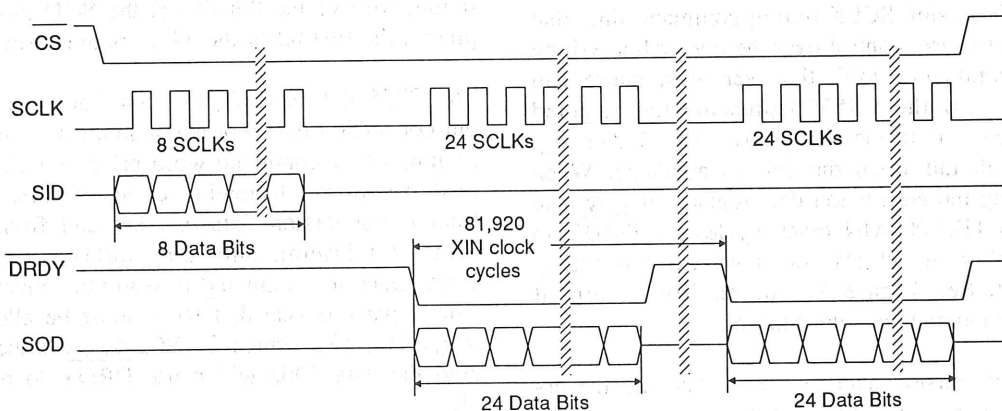


Figure 13. Continuous Read Conversion Data Mode (4 or 5 Wire)

The converter will continue to output conversion words at the update rate as long as a different command word is not started prior to DRDY falling again. The user is not required to read every output word to remain in the continuous update mode. DRDY will toggle high, and then low as each new output word becomes available. If a command word is issued immediately after a data word is read, the converter will end the read conversion mode. Figure 13 illustrates the continuous data mode.

The user should perform all data reads and command writes within 51,000 XIN clock cycles after DRDY falls to avoid ambiguity as to who controls the serial port.

### Serial Port Initialization

If for any reason the off-chip microcontroller fails to know whether the serial port of the CS5516/20 is in data mode or command mode the following initialization procedure can be issued to the port to force the CS5516/20 into the command mode. Write 128 or more 1's to the SID pin. Then issue a single 0 to the SID pin. The port will then be initialized into the command mode and will be waiting for an 8-bit command word.

### Bridge Excitation Options

The CS5516/CS5520 A/D converters are optimized for Wheatstone bridge applications. The converters support either dc or ac (switched dc) bridge excitation.

### DC Bridge Excitation

The CS5516/CS5520 can be configured for dc bridge excitation in either of two ways. The EXC bit of the configuration register can be set for either internal or for external excitation. If set to internally-controlled mode (EXC = 0), the F1 and F0 bits must be set to logic 0s. In this condition, the bridge can be excited from a dc supply with a resistor divider to develop the ap-

propriate reference voltage for the VREF+ and VREF- pins. Note that the bridge excitation should not be applied prior to the CS5516/CS5520 being powered-up. With EXC, F1, and F0 set to logic 0, the BX1 output will be logic 0 (0 volts) and the BX2 output will be a logic 1 (+5 volts).

A second method for configuring the converter for dc excitation is by setting EXC = 1, and connecting BX1 (pin 12) to VD+ (pin 20). This sets the converter for use with external excitation which uses the BX1 pin as an input to set the excitation frequency. With BX1 = VD+, the external excitation frequency is zero, or dc.

### AC Bridge Excitation

AC bridge excitation involves using a clock signal to generate a square wave which repetitively reverses the excitation polarity on the bridge. Advantages of this type of excitation are explained in the "Enemies of the Strain Gauge" section of the data sheet. To excite the bridge dynamically requires some type of bridge driver external to the CS5516/CS5520 converter. This driver is driven by a square wave clock. The source of this clock depends upon whether the converter is set for internal excitation or for external excitation. Figure 14 illustrates a sample bridge drive circuit when operating in the external AC mode.

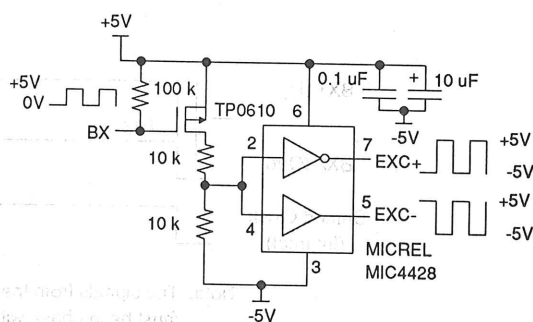


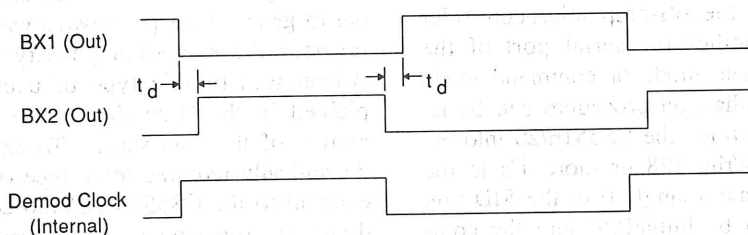
Figure 14. Sample AC Bridge Driver

Using internal excitation involves setting the EXC bit of the configuration register to 0, and setting the F1 and F0 bits to select the excitation frequency for the bridge. In this mode the excitation frequency is a sub-multiple of the XIN clock frequency. The excitation clock is output from the BX1 and BX2 pins of the converter in the form of a two-phase non-overlapping clock. The converter is capable of demodulating this clocked excitation. For proper operation the bridge must be driven so that its output signals into the AIN+ and VREF+ pins of the converter are in phase with the demodulation clock inside the converter (see Figure 15). The non-overlapping clock signals from BX1 and BX2 are CMOS level outputs (0 to VD+ volts) and are

capable of driving one TTL load. A buffer amplifier **MUST** be used to drive the bridge.

Whenever the internal mode is used for dynamic bridge excitation the signals are non-overlapping. The non-overlapping time is one XIN clock cycle.

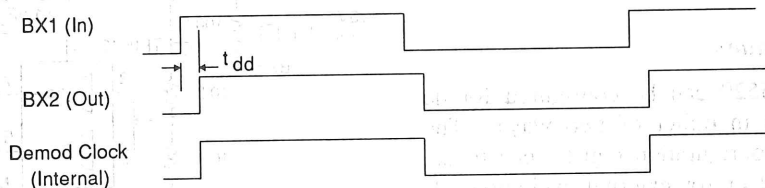
The converter can also be configured to provide dynamic bridge excitation when operating in the external-controlled bridge excitation mode. With the EXC bit of the configuration register set to logic 1, the BX1 pin becomes an input which determines the bridge excitation frequency and phase. BX1 should be near 50% duty cycle. The user can select the excitation frequency with the following restrictions. The excitation frequency



Note: The signals from the bridge into AIN+ and VREF+ of the converter must be in phase with the demodulation clock.

$t_d$  is 1 cycle of XIN clock.

**Figure 15. Internal Excitation Clock Phasing**



Note: The signals from the bridge into AIN+ and VREF+ of the converter must be in phase with the demodulation clock.

$t_{dd} \leq 64/XIN$ .

**Figure 16. External Excitation Space Clock Phasing**

must be synchronous with the XIN frequency of the converter and must be chosen using the following equation:

$$F_{exc} = (N \times XIN)/81,920$$

where N is an integer and lies in the range including 1 to 160.  $F_{exc}$  is the desired bridge excitation frequency. Other asynchronous frequencies are possible but may introduce a jitter component in the BX output signals. It is desirable not to choose an excitation frequency where interference components are present, such as 50 or 60 Hz or their harmonics. The XIN frequency would be divided down using a counter IC external to the A/D converter.  $F_{exc}$  would be input to the BX1 pin of the converter to synchronize the internal operations of the amplifiers and synchronous detection circuitry and to generate a clock output from the BX2 pin. The BX2 output is then used to drive the bridge amplifier with a signal of proper phase for detection by the converter. Figure 16 indicates the necessary phase of the signals to insure proper demodulation.

Whenever the dynamic excitation clock output from either the BX1 and BX2 pins (during internal excitation) or from the BX2 pin (during external excitation) changes states, the converter waits 64 XIN cycles before sampling the AIN and VREF signal inputs. The delay allows some time for the signal to settle from the modulation event.

### Input Filtering

Some load cells are located a distance from the input to the converter. Under these conditions, separate twisted pair cabling is recommended for the excitation drive to the bridge, the excitation sense leads (if used) and for the AIN± signal leads. If the AIN± leads to the converter and the VREF± leads to the converter are filtered, care should be exercised in the choice of components. With either dc or ac excitation, one should limit

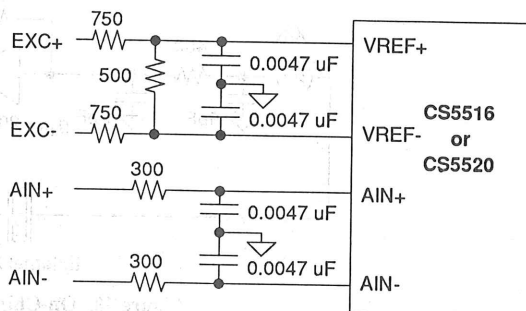


Figure 17. External AC Excitation Filter Components

any input filtering resistors on AIN or on VREF to below 1 kΩ. Values greater than this will degrade noise performance of the converter. In ac excitation applications, any filtering must be broadband enough that the switched dc excitation signal can settle within 10 μsecs. Failure to meet this settling requirement will affect measurement accuracy. Figure 17 illustrates acceptable filter components for ac excitation. If only differential filtering is required, a single capacitor can be placed between AIN+ and AIN- (and VREF+ and VREF-) in place of two capacitors to ground.

### Voltage Reference Considerations

The CS5516/20 include an on-chip voltage reference which is output on the MDRV- and referenced from the MDRV+ pin. The converter is designed to be operated as a ratiometric measurement device. The 2-channel delta-sigma converter uses the internal MDVR (Modulator Differential Voltage Reference) as its reference. Since the MDVR is used for converting both the AIN and VREF signals at the same time, the absolute value of the MDVR and its tempco are not important when the CS5516/20 is used in the ratiometric measurement mode. The voltage reference output, MDVR-, should be decoupled using a 1 uF capacitor which is connected to the MDRV+ supply line. Voltage reference decoupling is shown on the system connection diagrams.

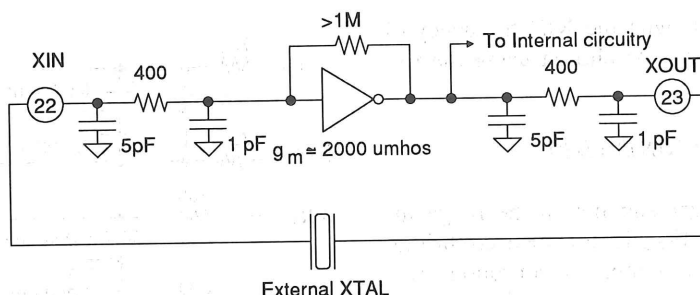


Figure 18. On-Chip Gate Oscillator Model

If absolute measurements are to be made by the CS5516/20, then a precision reference should be input into the VREF+ and VREF- terminals.

### Clock Generator

The CS5516/20 includes a gate which can be connected as a crystal oscillator to provide the master clock to run the chip. Alternatively, an external (CMOS compatible) clock can be input into the XIN pin. Figure 18 illustrates a simple model for the on-chip gate oscillator. The on-chip oscillator is designed to typically operate with crystal frequencies between 4.0 and 5.0 MHz without additional loading capacitors. If other crystal frequencies, or if ceramic resonators are used, additional loading capacitance may be necessary.

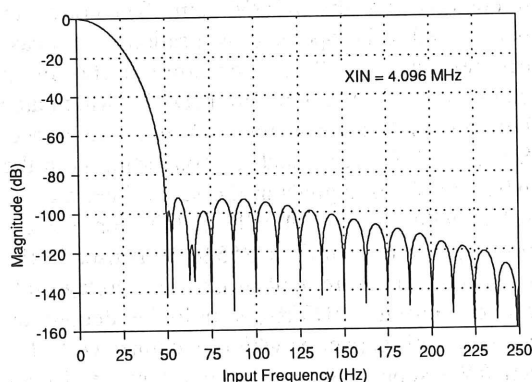


Figure 19. Filter Magnitude Response

The XOUT pin can be used to drive one CMOS gate for system clock requirements. Be sure to include the gate's input capacitance and stray capacitance as part of the loading capacitance for the resonating element.

### Digital Filter

The delta-sigma A/D converter consists of a third order modulator and a digital filter. The device is optimized to operate with clock frequencies of 4.096 MHz or 4.9152 MHz. These result in the filter having a 3dB bandwidth of 12 Hz or 15 Hz, with output word rates of 50 or 60Hz. The rejection at  $50\text{Hz} \pm 3\text{Hz}$  is 70 dB minimum with a 4.096 MHz clock. Similar rejection is obtained at 60 Hz with a 4.9152 MHz clock. The user can further decimate the output without aliasing down to the DC to 3Hz band. Rejection of line frequencies is therefore ensured over the normal frequency

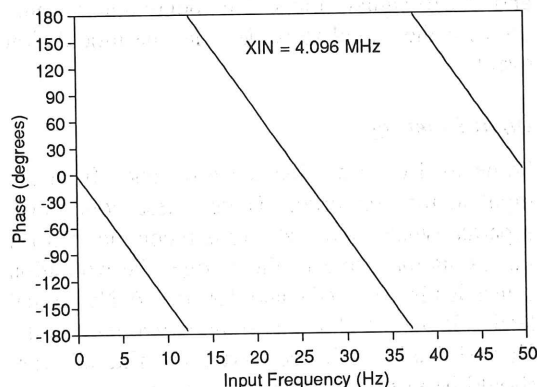


Figure 20. Filter Phase Response.

variation of the power system. Figures 19 and 20 illustrate the magnitude and phase of the filter when using a 4.096 MHz clock.

The digital filter computes a new output data word every 81,920 XIN clock cycles. If the input experiences a large change in amplitude, the PGA gain is changed, or the DAC calibration registers are changed, it may take up to six filter cycles (81,920 X 6 clock cycles) for the filter to compute an output word which is fully settled to the input signal.

### Output Coding

The CS5516/20 converters output data in binary format when operating in unipolar mode and in two's complement when operating in bipolar mode. Table 4 illustrates the output coding for the converters. Note that when reading conversion data from the converter the data word is output MSB or sign bit first. Falling edges on SCLK advance the data word to the next lower bit.

The output conversion words from both the CS5516 and the CS5520 are 24 bits long. The CS5516 has 16 data bits followed by 8 flag bits (all identical). The CS5520 has 20 data bits followed by 4 flag bits (all identical). To read the conversion data, including the error flag information will require at least 17 SCLKs for the CS5516 and at least 21 SCLKs for the CS5520.

Under large overrange conditions, approximately two times full scale, (for example: when the converter is set-up for a full scale sensitivity of 25 mV, an input of 50 mV would be an excessive overrange condition) the flag bits of the output conversion word will be set. If an excessive overrange condition exists, whether it be a positive or negative overrange, the converter may not be able to yield a proper output code. Under this condition the flag bits will be set to all 1's. Under normal operating conditions flag bits will remain 0's.

Unipolar Input Voltage	Offset Binary	Bipolar input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFF	>(VFS-1.5 LSB)	7FFF
VFS-1.5 LSB	FFFF	VFS-1.5 LSB	7FFF
	-----		-----
	FFFE		7FFE
VFS/2-0.5 LSB	8000	-0.5 LSB	0000
	-----		-----
	7FFF		FFFF
+0.5 LSB	0001	-VFS+0.5 LSB	8001
	-----		-----
	0000		8000
<(+0.5 LSB)	0000	<(-VFS+0.5 LSB)	8000

CS5516 Output Coding

Unipolar Input Voltage	Offset Binary	Bipolar input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFFF	>(VFS-1.5 LSB)	7FFFF
VFS-1.5 LSB	FFFFF	VFS-1.5 LSB	7FFFF
	-----		-----
	FFFFE		7FFFE
VFS/2-0.5 LSB	80000	-0.5 LSB	00000
	-----		-----
	7FFFF		FFFFF
+0.5 LSB	00001	-VFS+0.5 LSB	80001
	-----		-----
	00000		80000
<(+0.5 LSB)	00000	<(-VFS+0.5 LSB)	80000

CS5520 Output Coding

Note: VFS in the table equals the full scale voltage between +VREF/(G x 25) and ground for unipolar mode; and between  $\pm VREF/(G \times 25)$  for bipolar mode. The signal input to the A/D section of the converter has been amplified by the instrumentation amplifier (x25) and the PGA gain, G (1, 2, 4 or 8). See text about error flags under overrange conditions.

Table 4. CS5516/20 Output Coding



After the converter is first powered-up, a  $\overline{\text{RST}}$  is issued, or the device comes out of the SLEEP mode, the first conversion data read may erroneously have its error flag bits set to "1".

### ***Synchronizing Multiple Converters***

Multiple converters can be made to output their conversion words at the same time if they are operated from the same clock signal at XIN. To synchronize multiple converters requires that they all have their RF bit of the configuration register written to a logic 1 and then back to 0. The filters will be allowed to start convolutions after the falling edge of the 24th SCLK used to write the RF bit to the configuration register. The filter will start a new convolution on the next rising edge of the XIN clock after the 24th SCLK falls.

### ***Sleep Mode***

The CS5516/20 configuration register has an A/S bit which allows the users to put the device in a sleep condition to lower quiescent power. Upon reset the A/S bit device is set to a logic 0 which places the device in the 'awake' condition. Writing a 1 to the A/S bit will shutdown most of the chip, including the oscillator. It is desirable to use the following sequence when coming out of sleep. Write a logic 0 to the A/S bit of the configuration register. In the same configuration word write a logic 1 to the RF bit of the configuration register. Then wait until it is certain that the oscillator has started. After the oscillator has started or a clock present on the XIN pin, set the RF bit back to 0. The user should then wait at least 6 output word update periods before expecting a valid output data word.

## PIN DESCRIPTIONS

Modulator Diff. Voltage Ref +	<b>MDRV+</b>	1	24	<b>SMODE</b>	Ser Interface Mode Select
Modulator Diff. Voltage Ref -	<b>MDRV-</b>	2	23	<b>XOUT</b>	Crystal Out
Positive Analog Power	<b>VA+</b>	3	22	<b>XIN</b>	Crystal In
Negative Analog Power	<b>VA-</b>	4	21	<b>VD-</b>	Negative Digital Power
Analog Ground One	<b>AGND1</b>	5	20	<b>VD+</b>	Positive Digital Power
Analog In +	<b>AIN+</b>	6	19	<b>DGND</b>	Digital Ground
Analog In -	<b>AIN-</b>	7	18	<b>SOD</b>	Serial Output Data
Analog Ground Two	<b>AGND2</b>	8	17	<b>SID</b>	Serial Input Data
Voltage Ref In +	<b>VREF+</b>	9	16	<b>SCLK</b>	Serial Clock Input
Voltage Ref In -	<b>VREF-</b>	10	15	<b>DRDY</b>	Data Ready
Bridge Excite 2	<b>BX2</b>	11	14	<b>CS</b>	Chip Select
Bridge Excite 1	<b>BX1</b>	12	13	<b>RST</b>	Reset

3

### Power Supply Connections

#### VD+ - Positive Digital Power, PIN 20.

Positive digital supply voltage. Nominally +5 volts.

#### VD- - Negative Digital Power, PIN 21.

Negative digital supply voltage. Nominally -5 volts.

#### DGND - Digital Ground, PIN 19.

Digital ground.

#### VA+ - Positive Analog Power, PIN 3.

Positive analog supply voltage. Nominally +5 volts.

#### VA- - Negative Analog Power, PIN 4.

Negative analog supply voltage. Nominally -5 volts.

#### AGND1, AGND2 - Analog Ground, PINS 5, 8.

Analog ground.

### Clock Generator

#### XIN; XOUT - Crystal In; Crystal Out, Pins 22, 23

An internal gate is connected to these pins enabling the use of either a crystal or a ceramic resonator to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be input to the XIN pin as the master clock for the device.

### **Digital Inputs**

#### **RST - Reset, PIN 13.**

Reset pin initializes all calibration registers to a known condition and places the serial port into the command mode.

#### **CS - Chip Select, PIN 14.**

An input which can be enabled by an external device to gain control over the serial port. When this pin is high, SOD is in a high impedance state if SMODE = 0.

#### **SCLK - Serial Data Clock, PIN 16.**

A clock signal at this pin determines the output rate of the data from the SOD pin and the input data rate on the SID pin.

#### **SID - Serial Input Data, PIN 17.**

This pin is used for inputting command and configuration words or inputting calibration words. Data is input at a rate determined by SCLK. SID is in a don't care state when no data is being clocked in.

#### **SMODE - Serial Interface Mode Select, PIN 24.**

Selects the operating mode of the serial port. When low the serial port operates in the 5 or 4 wire interface mode. When high the chip will enter the 3 wire interface mode.

### **Analog Inputs**

#### **AIN+ and AIN- - Analog Inputs, PINS 6, 7.**

The analog input signals from the transducer. These are true differential inputs.

#### **VREF+ and VREF- - Voltage Reference Inputs, PINS 9,10.**

These are the differential analog reference voltage inputs.

#### **MDRV+ - Modulator Differential Voltage Reference, PIN 1.**

Positive terminal of the internal differential voltage reference which can be tied to the positive supply (VA+) or ground (AGND).

#### **MDRV- - Modulator Differential Voltage Reference, PIN 2.**

This is the -3.75V modulator differential voltage reference output and can be used to generate an analog reference. Note this is with reference to the MDRV+ line.

### Digital Outputs

#### BX1 and BX2 - AC Bridge Excitation Signals, PINS 12, 11.

These can be buffered to drive the transducer or used as synchronizing signals for a transducer drive circuit. BX1 and BX2 are 0 to +5V signals.

#### DRDY - Data Ready, PIN 15.

DRDY goes low every 81,920 cycles of XIN (when in read conversion data mode) to indicate that new data has been placed in the output port. DRDY goes high when all the serial port data is clocked out, when the serial port is being updated with new data, when a calibration is in progress, or when the device is in SLEEP.

#### SOD - Serial Output Data, PIN 18.

Data from the serial port will be output from this pin at a rate determined by SCLK. The data will either be conversion data, or, calibration values, dependent upon the command word that has been previously input on the SID pin. The SOD pin furnishes a high impedance output state when not transmitting data (SMODE = 0).

3

### Ordering Guide

Model Number	Linearity Error (Max)	Temperature Range	Package
CS5516-AP	0.003%	-40 to +85°C	24-pin 0.3" Plastic DIP
CS5516-AS	0.003%	-40 to +85°C	24-pin 0.3" SOIC
CS5516-SD	0.003%	-55 to +125°C	24-pin 0.3" Cerdip
CDB5516	CS5516 evaluation board		
CS5520-BP	0.0015%	-40 to +85°C	24-pin 0.3" Plastic DIP
CS5520-BS	0.0015%	-40 to +85°C	24-pin 0.3" SOIC
CS5520-SD	0.003%	-55 to +125°C	24-pin 0.3" Cerdip
CDB5520	CS5520 evaluation board		

## SPECIFICATION DEFINITIONS

### Linearity Error

The deviation of a code from a straight line which extends between two fixed points on the A/D converter transfer function. In unipolar mode, the straight line extends from one point located  $\frac{1}{2}$  LSB below the first code transition, one count above all zeros; to the second point located  $\frac{1}{2}$  LSB beyond the code transition to all ones. In bipolar mode, the straight line extends from one point located  $\frac{1}{2}$  LSB beyond the code transition to all ones, passing through a point  $\frac{1}{2}$  LSB below code 8000(H) (16-bit); 80000(H) (20-bit); extending to beyond negative full scale. Units are in percent of full-scale.

### Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

### Full Scale Error

The deviation of the last code transition from the ideal  $[(V_{REF+}) - (V_{REF-})] - \frac{3}{2}$  LSB]. Units are in LSBs.

### Unipolar Offset

The deviation of the first code transition from the ideal ( $\frac{1}{2}$  LSB above AGND) when in unipolar mode (BP/ $\overline{UP}$  low). Units are in LSBs.

### Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal ( $\frac{1}{2}$  LSB below AGND) when in bipolar mode (BP/ $\overline{UP}$  high). Units are in LSBs.

## CS5516 & CS5520 ADC Evaluation Board

### Features

- On board microcontroller
- RS232 Serial Communications with host PC
- On board bridge drivers
- Correct power & grounding

### General Description

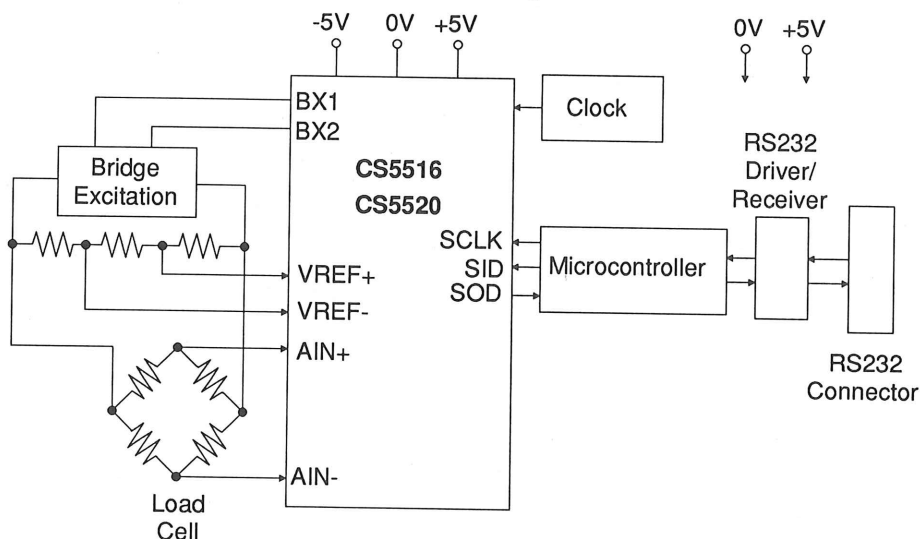
The CDB5516 and CDB5520 provide quick and easy evaluation of the CS5516 and CS5520 bridge transducer A/D converters. Direct connection of the bridge to the host board is provided.

The board also contains a microcontroller, with firmware which allows the board to be controlled via simple serial commands, using the RS232 communications port of a PC.

ORDERING INFORMATION: CDB5516

3

**Block Diagram**



•Notes•





**GENERAL INFORMATION****1****DIGITAL AUDIO:****DIGITAL AUDIO PRODUCTS****2****Digital Volume Control****Multimedia Codecs****Digital-to-Analog Converters****Analog-to-Digital Converters****AES/EBU & S/PDIF Interfaces****DATA ACQUISITION:****ANALOG-TO-DIGITAL CONVERTERS****3****General Purpose & Military****Seismic****DC Measurement****Transducer Interface****SUPPORT FUNCTIONS:****SUPPORT FUNCTION PRODUCTS****4****Power Monitor****Track & Hold Amplifiers****Voltage References****COMMUNICATIONS:****COMMUNICATIONS PRODUCTS****5****T1/CEPT Line Interfaces & Framers****Jitter Attenuators****T3 Receiver****Local Area Network I.C.s****DTMF Receivers****MISCELLANEOUS:****APPLICATION NOTES & PAPERS****6****APPENDICES****7****Radiation Information****Reliability Calculation Methods****Package Mechanical Drawings****SALES OFFICES****8**

### Power Monitor and Watchdog Timer

The CS1232 compares the system power supply to an on-chip, band-gap voltage reference and signals if the supply falls below 4.6 volts. This permits the host microprocessor to power down the system gracefully before the supply fails. Critical system parameters can be saved in non-volatile memory for reinitialization when the power supply returns to rated levels. The CS1232 also contains a watchdog timer and push-button reset circuit.

### 1 $\mu$ s, 12-bit Accurate Sample and Hold Amplifiers

The CS31412 and CS3112 sample and hold amplifiers feature on-chip calibration logic for high accuracy. The CS31412 is a four channel simultaneous sample and hold amplifier capable of processing four signal-ended or two differential inputs. With 12-bit accuracy and a fast 1  $\mu$ s acquisition time, the CS31412 is ideal for processing high-frequency signals. Droop in hold mode is

less than 0.001  $\mu$ V/ $\mu$ s. The device also features output buffer amplifiers, an output multiplexer and a flexible microprocessor interface. Crystal Semiconductor's single channel CS3112 sample and hold shares the fast, accurate performance of the CS31412.

### Voltage References

The CS3903 and CS3904 are Crystal Semiconductor's first precision references. The devices feature +3.0 V and  $\pm 1.5$  V outputs which are perfectly suited for use with Crystal's CS5412, 12-bit, 1MHz ADC.

The devices only require  $\pm 5$  V supplies and are stable to 25 ppm per 1000 hours.

The CS3902 is a precision +4.5 volt reference with an operating voltage of 11 to 22 volts. Featuring very low temperature drift and excellent long term stability, it is suitable for use with all Crystal Semiconductor successive approximation A/D converters.

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## Micromonitor

### Features

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatic restart after power failure
- Monitors pushbutton for external reset
- Monitors microprocessor power supply to be within 5% or 10% of 5 V
- No discrete components needed
- 8-pin Mini-DIP or 16-pin SOIC
- Pin compatible with DS1232

### General Description

The CS1232 is a monitor for microprocessors which checks program execution, power source quality, and external reset status.

The power status ( $V_{CC}$ ) is monitored by a comparator and a precision temperature-compensated reference. Reset is forced active by an internal signal when  $V_{CC}$  goes out-of-tolerance. Reset signals stay active for a minimum for 250 ms after  $V_{CC}$  returns to an in-tolerance condition. This allows both power supply and processor to stabilize.

The pushbutton reset control input is debounced and the active reset minimum pulse width of 250 ms is guaranteed.

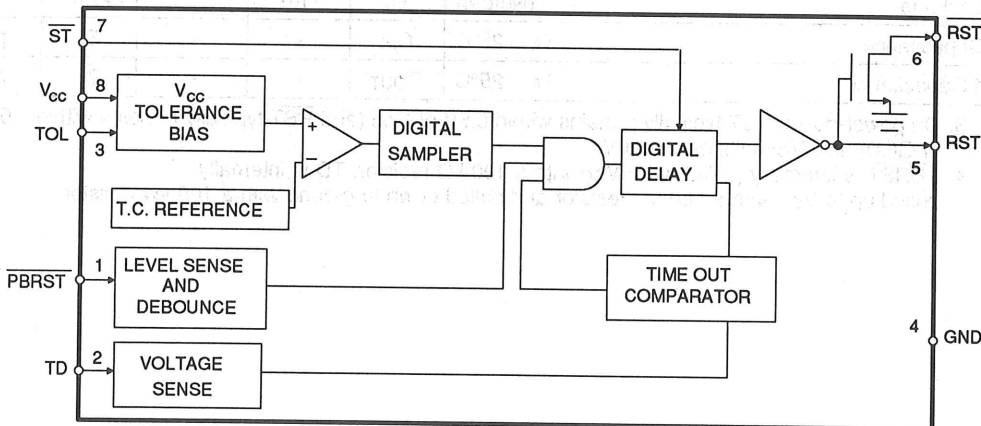
The internal watchdog timer forces the reset signals active if the strobe input is not driven low prior to time out. The CS1232 timer can be set to operate at time out settings of approximately 150ms, 600ms, and 1.2 seconds.

A surface mount 16-pin SOIC is available, as well as an 8-pin Plastic DIP.

#### ORDERING INFORMATION:

Model	Temp. Range	Package
CS1232-CP	0 °C to 70 °C	8-pin Plastic DIP
CS1232-IP	-40 °C to +85 °C	8-pin Plastic DIP
CS1232-CS	0 °C to 70 °C	16-pin SOIC
CS1232-IS	-40 °C to +85 °C	16-pin SOIC
<b>Die Only:</b>		Unpackaged Die
CS1232-YU		

4



## ANALOG CHARACTERISTICS (T<sub>MIN</sub> to T<sub>MAX</sub>, V<sub>CC</sub> = 4.5 to 5.5V)

Parameter		Symbol	Min	Typ	Max	Units
V <sub>CC</sub> Trip Point (Note 1)	TOL = GND	V <sub>CC</sub> TP	4.50	4.62	4.74	V
	TOL = V <sub>CC</sub>	V <sub>CC</sub> TP	4.25	4.37	4.49	V
Operating Current (Note 2)		I <sub>CC</sub>	-	0.4	2.0	mA

Notes: 1. All voltages referenced to ground.  
2. Measured with outputs open.

## RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
Operating Temperature	CS1232		0	-	+70	°C
	CS1232-I		-40	-	+85	°C
Supply voltage	(Note 1)	V <sub>CC</sub>	4.5	5.0	5.5	V

## DIGITAL CHARACTERISTICS (T<sub>MIN</sub> to T<sub>MAX</sub>, V<sub>CC</sub> = 4.5V to 5.5V)

Parameter		Symbol	Min	Typ	Max	Units
$\overline{ST}$ and $\overline{PBRST}$ Input High Level (Note 1)		V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level (Note 1)		V <sub>IL</sub>	-0.3	-	+0.8	V
Output High Current at 2.4 V RST only		I <sub>OH</sub>	-8.0	-10.0	-	mA
Output High Voltage at -500 $\mu$ A RST only (Note 3)		V <sub>OH</sub>	V <sub>CC</sub> -0.5	V <sub>CC</sub> -0.1	-	V
Output Low Current at 0.4 V RST, $\overline{RST}$		I <sub>OL</sub>	8.0	10.0	-	mA
Input Leakage (Note 4)		I <sub>IL</sub>	-1.0	-	+1.0	$\mu$ A
Input Capacitance T <sub>A</sub> = 25°C		C <sub>IN</sub>	-	-	5	pF
Output Capacitance T <sub>A</sub> = 25°C		C <sub>OUT</sub>	-	-	7	pF

Notes: 3. On power-down, RST typically remains within 0.5V of V<sub>CC</sub> (and  $\overline{RST}$  typically remains within 0.5V of GND) until V<sub>CC</sub> falls below 2.0V.  
4.  $\overline{PBRST}$  is internally pulled up to V<sub>CC</sub> with a 100 k $\Omega$  resistor. TD is internally pulled up to V<sub>CC</sub> with a 100 k $\Omega$  resistor and pulled down to ground with a 100 k $\Omega$  resistor.

Specifications are subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS

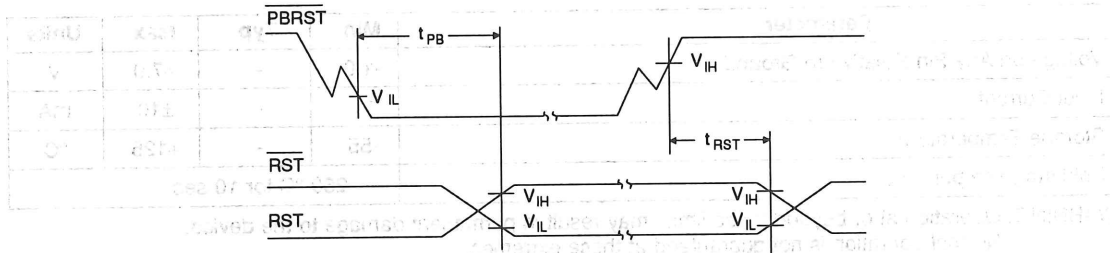
Parameter	Min	Typ	Max	Units
Voltage on Any Pin Relative to Ground	-1.0	-	+7.0	V
Input Current	-	-	±10	mA
Storage Temperature	-55	-	+125	°C
Soldering Temperature	260 °C for 10 sec			

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

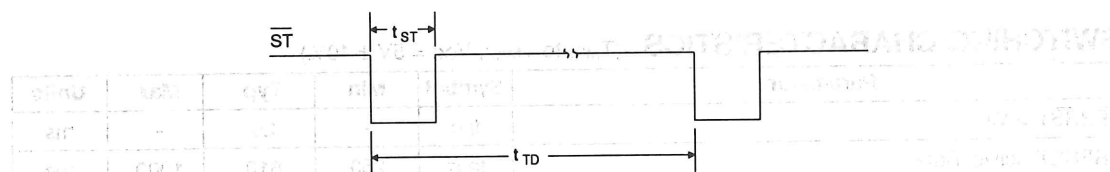
## SWITCHING CHARACTERISTICS (T<sub>MIN</sub> to T<sub>MAX</sub>, V<sub>CC</sub> = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
PBRST = V <sub>IL</sub>	t <sub>PB</sub>	-	20	-	ms
RESET Active Time	t <sub>RST</sub>	250	610	1000	ms
ST Pulse Width	t <sub>ST</sub>	20	-	-	ns
V <sub>CC</sub> Detect to RST and $\overline{\text{RST}}$	t <sub>RPD</sub>	-	-	100	ns
V <sub>CC</sub> Slew Rate from 4.75V - 4.25V	t <sub>F</sub>	300	-	-	µs
V <sub>CC</sub> Detect to RST and $\overline{\text{RST}}$ (Note 5)	t <sub>RPU</sub>	250	610	1000	ms
V <sub>CC</sub> Slew Rate from 4.25V - 4.75V	t <sub>R</sub>	0	-	-	ns
ST Pulse Period (Note 6)	TD pin at Ground	t <sub>TD</sub>	50.0	150	ms
	TD pin floating	t <sub>TD</sub>	250	600	ms
	TD pin connected to V <sub>CC</sub>	t <sub>TD</sub>	400	1200	ms

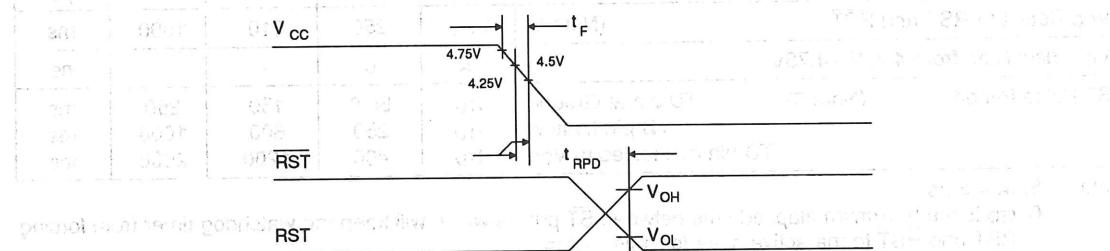
- Note: 5. t<sub>R</sub> = 5 µs  
6. t<sub>TD</sub> is the maximum elapsed time between ST pulses which will keep the watchdog timer from forcing RST and  $\overline{\text{RST}}$  to the active state for a time of t<sub>RST</sub>.  
7.  $\overline{\text{RST}}$  is an N-channel open drain output.



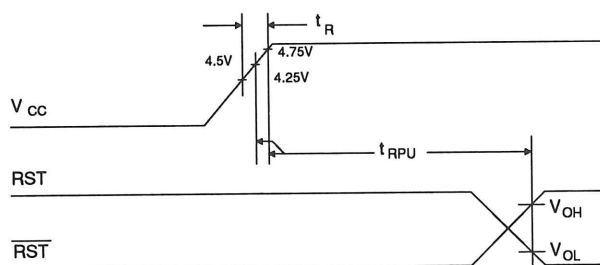
**Timing Diagram—Pushbutton Reset**



**Timing Diagram—Strobe Input**



**Timing Diagram—Power Down**



**Timing Diagram—Power Up**

### POWER SUPPLY MONITOR

The CS1232 will detect out-of-tolerance power supplies for processor-based systems as well as warn of an impending power failure. The TOL digital input pin defines the threshold level for VCC; when the VCC level drops below the TOL defined level, the CS1232 asserts the signals RST and  $\overline{\text{RST}}$ . The threshold level is set to typically 4.37 V if TOL is connected to VCC, and is set to typically 4.62 V if TOL is connected to GND. The processor is allowed to continue until the last possible moment that VCC is valid. Upon return of power, RST and  $\overline{\text{RST}}$  are active for 250 ms (minimum) to allow stabilization.

### PUSHBUTTON RESET CONTROL

$\overline{\text{PBRST}}$  is normally connected to a reset push-button (see Figure 1). This active low signal is debounced and timed to generate signals of 250 ms (minimum) for RST and  $\overline{\text{RST}}$ . The delay begins when  $\overline{\text{PBRST}}$  is released from the low state.  $\overline{\text{PBRST}}$  has an internal 100 k $\Omega$  pull-up resistor.

### WATCHDOG TIMER

When RST and  $\overline{\text{RST}}$  become inactive (normal CPU operation), the watchdog timer starts timing out, using the time set by TD. RST and  $\overline{\text{RST}}$  are forced active when  $\overline{\text{ST}}$  is not stimulated for this predetermined time. TD sets the time to be: 150 ms if TD is connected to ground, 600 ms if TD is not connected, or 1.2 seconds with TD connected to VCC. RST and  $\overline{\text{RST}}$  are driven active for 250 ms (minimum) if no high-to-low transition occurs on the  $\overline{\text{ST}}$  input pin before time out. Microprocessor address signals, data signals, control signals, and output port bits can be used for the  $\overline{\text{ST}}$  input pin. These signals cause the watchdog timer to be reset prior to time out indicating normal function of the microprocessor (see Figure 2).

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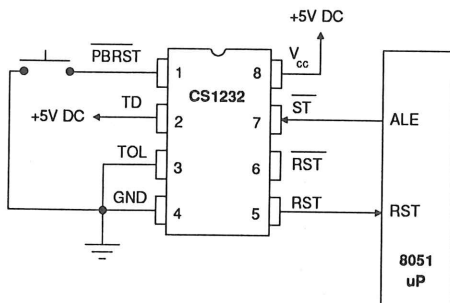


Figure 1. Pushbutton Reset

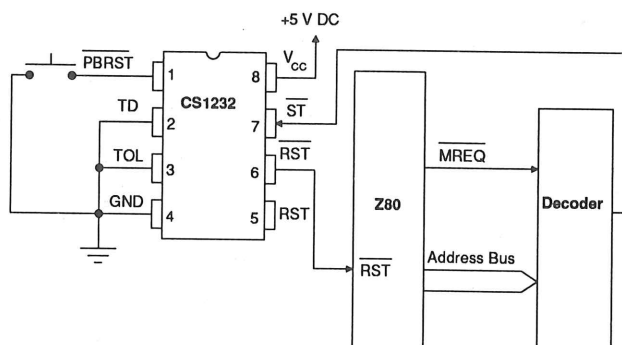


Figure 2. Watchdog Timer



PUSH BUTTON RESET INPUT	<b>PBRST</b>	1	8	Vcc	+5 VOLT POWER
TIME DELAY SET	<b>TD</b>	2	7	<b>ST</b>	STROBE INPUT
SELECTS Vcc DETECT LEVEL	<b>TOL</b>	3	6	<b>RST</b>	RESET OUTPUT (Active Low, Open Drain)
GROUND	<b>GND</b>	4	5	<b>RST</b>	RESET OUTPUT (Active High)
NO CONNECTION	<b>NC</b>	1	16	<b>NC</b>	NO CONNECT
PUSH BUTTON RESET INPUT	<b>PBRST</b>	2	15	Vcc	+5 VOLT POWER
NO CONNECT	<b>NC</b>	3	14	<b>NC</b>	NO CONNECTION
TIME DELAY SET	<b>TD</b>	4	13	<b>ST</b>	STROBE INPUT
NO CONNECT	<b>NC</b>	5	12	<b>NC</b>	NO CONNECT
SELECTS Vcc DETECT LEVEL	<b>TOL</b>	6	11	<b>RST</b>	RESET OUTPUT (Active Low, Open Drain)
NO CONNECT	<b>NC</b>	7	10	<b>NC</b>	NO CONNECT
GROUND	<b>GND</b>	8	9	<b>RST</b>	RESET OUTPUT (Active High)

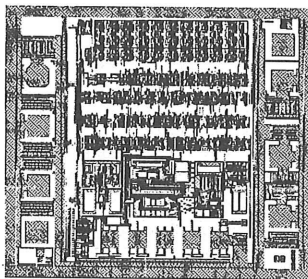


### DIE INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

#### Assembly Information

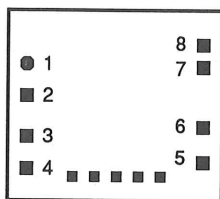
1. Die size: 0.061" by 0.069" ( $\pm 0.002$ ").
2. The die is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to  $V_{CC}$ .
3. Die thickness shall be 0.0175"  $\pm 0.0035$ ". If tighter tolerances are required, contact the factory.
4. The maximum number of die per waffle pack carrier is 100.
5. The cavity dimensions for each die within the waffle pack are 0.080" by 0.080" (Waffle Pack Type H20-080).



6. The CS1232-YU requires no particular bonding sequence.
7. Each pin of the CS1232 has ESD and latch-up protection circuitry.
8. Technical constraints limit the viability of accurate performance measurements of precision analog IC's at wafer probe. Although high yield to the limits listed in the specification tables is anticipated, no guarantee is given for unpackaged die product.

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CS1232-YU Bonding Diagram



1 - $\overline{PBRST}$	5 - $\overline{RST}$
2 - TD	6 - $\overline{RST}$
3 - TOL	7 - $\overline{ST}$
4 - GND	8 - VCC

# •Notes•



Crystal oscillator is a device that generates a precise and stable frequency signal. It is commonly used in various electronic circuits, including microcontrollers, timers, and communication systems.

The frequency of a crystal oscillator is determined by the physical properties of the crystal material, such as its size, shape, and composition. The frequency can be adjusted by changing the physical properties of the crystal.

Crystal oscillators are highly accurate and stable, making them ideal for applications that require precise timing. They are also relatively inexpensive and easy to use, which makes them a popular choice for many electronic designs.

Crystal oscillators are used in a wide range of applications, from low-frequency clocks in microcontrollers to high-frequency oscillators in communication systems. They are also used in precision timing applications, such as in scientific instruments and industrial control systems.

Crystal oscillators are available in a variety of packages, including through-hole and surface-mount. They are also available in a range of frequencies, from a few kHz to several MHz.

Crystal oscillators are a key component in many electronic systems, and their performance is critical to the overall accuracy and stability of the system. Understanding the characteristics and applications of crystal oscillators is essential for designing reliable electronic circuits.

Crystal oscillators are a simple yet powerful component that can provide a precise and stable frequency signal for a wide range of applications. They are a fundamental building block in many electronic systems.

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Crystal oscillator circuit diagram



1	Crystal	1	Crystal
2	Resistor	2	Resistor
3	Capacitor	3	Capacitor
4	Resistor	4	Resistor

## High Speed Precision Track and Hold

### Features

- Completely Self-Contained On-Chip Hold Capacitor Microprocessor Interface
- Fast Acquisition: 800ns to 0.01%
- Low Aperture Jitter: 100ps
- 12-Bit Linearity
- Total Offset, Including Hold Pedestal: 1.8 mV
- Low Droop Rate: 0.001uV/us
- Self-Calibration Insures Accuracy Over Time and Temperature
- Low Power Dissipation: 130 mW

### General Description

The CS3112 is a high speed track and hold with 12-bit linearity. It is completely self-contained, including hold capacitor, output buffer, and calibration circuitry.

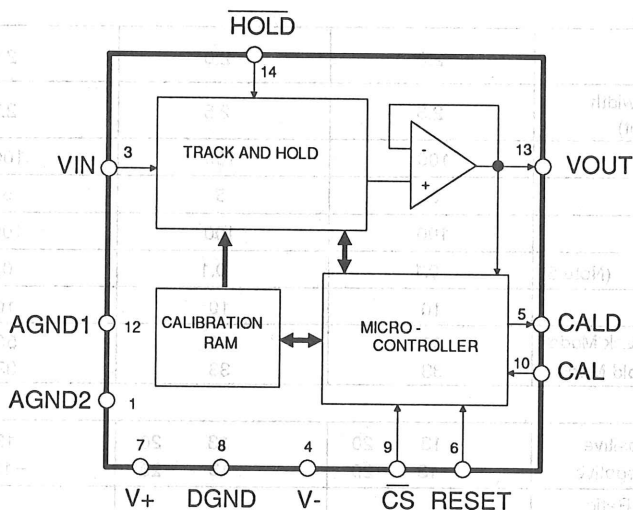
Aperture jitter of 100ps and acquisition time of 800ns to 0.01% provide excellent dynamic performance. An on-chip hold capacitor limits droop to 0.001 uV/us, and first order leakage compensation minimizes droop over the full operating temperature range.

Advanced CMOS fabrication insures low power consumption and increased reliability.

The CS3112 can be controlled and monitored through its microprocessor interface, or can operate independently.

### ORDERING INFORMATION:

Model	Acquisition Time	Temp. Range	Package
CS3112-KD2	2.0 $\mu$ s	0 to 70 °C	14-pin CerDIP
CS3112-KD1	1.0 $\mu$ s	0 to 70 °C	14-pin CerDIP
CS3112-BD1	1.0 $\mu$ s	-40 to +85 °C	14-pin CerDIP
CS3112-TD1	1.0 $\mu$ s	-55 to +125 °C	14-pin CerDIP



**ANALOG CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V_+ = +5.0\text{V}$ ,  $V_- = -5.0\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $C_L = 50\text{pF}$ , Analog Source Impedance =  $40\Omega$ , unless otherwise specified)

Parameter*	CS3112-K			CS3112-B			CS3112-T			Units
	min	typ	max	min	typ	max	min	typ	max	
Specified Temperature Range	0 to +70			-40 to +85			-55 to +125			°C
<b>Accuracy</b>										
Total Offset (Note 1) 25°C T <sub>min</sub> to T <sub>max</sub>	-1.8 ± 3.0 ± 3.5			-1.8 ± 3.0 ± 3.5			-1.8 ± 3.0 ± 3.5			mV mV
Offset Drift (Note 2) T <sub>min</sub> to T <sub>max</sub>	± 0.020			± 0.025			± 0.030			mV/°C
Tracking Offset	± 55			± 55			± 55			mV
Nonlinearity 25°C (Note 3) T <sub>min</sub> to T <sub>max</sub>	± 0.5 ± 0.7 ± 0.5			± 0.5 ± 0.7 ± 0.5			± 0.5 ± 0.7 ± 0.5			mV mV
Gain Error T <sub>min</sub> to T <sub>max</sub>	± 0.01			± 0.01			± 0.01			% FS
<b>Dynamic Characteristics</b>										
Acquisition Time (6V step to 0.01%)  (6V step to 0.1%)	-1 -2  -1 -2	0.8 1.6  0.6 1.2	1.0 2.0	0.8   0.6	1.0	0.8   0.6	1.0	0.8   0.6	1.0   us us us us	
Track to Hold Settling to 0.01%	0.5 0.8			0.5 0.8			0.5 0.8			us
Aperture Time	20			20			20			ns
Aperture Time Matching (Note 4)	2			2			2			ns
Aperture Jitter	100			100			100			ps
Droop Rate 25°C T <sub>min</sub> to T <sub>max</sub>	± 0.001 ± 0.1 ± 0.6			± 0.001 ± 0.1 ± 1.0			± 0.001 ± 0.1 ± 5.0			uV/us uV/us
<b>Analog Input/Output</b>										
Large Signal Bandwidth (6V p-p Input)	2.0			2.0			2.0			MHz
Small Signal Gain Bandwidth (60mV p-p Input)	2.5			2.5			2.5			MHz
Input Impedance (dc)	100			100			100			MΩ
Input Capacitance	5			5			5			pF
Input Bias Current	100			100			100			pA
Output Impedance at dc (Note 3)	0.1			0.1			0.1			Ω
Output Slew Rate	10			10			10			V/us
Noise (Note 5) Track Mode	50			50			50			uV <sub>rms</sub>
Hold Mode	33			33			33			uV <sub>rms</sub>
<b>Power Supplies</b>										
Supply Currents Positive	13 20			13 20			13 20			mA
Negative	-13 -20			-13 -20			-13 -20			mA
Power Supply Rejection Ratio Positive (Note 6)	75			75			75			dB
Negative (Note 7)	60			60			60			dB

\*Refer to Error Definitions at the end of this data sheet.

Specifications are subject to change without notice.

### RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 8).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive	V+	4.5	5.0	5.5	V
Negative	V-	- 4.5	-5.0	-5.5	V
Analog Input Voltage:	V <sub>IN</sub>	- 3.0	-	3.0	V

### DIGITAL CHARACTERISTICS (T<sub>A</sub> = T<sub>min</sub> to T<sub>max</sub>; V+ = 5V±10%; V- = -5V±10%)

All measurements below are performed under static conditions.

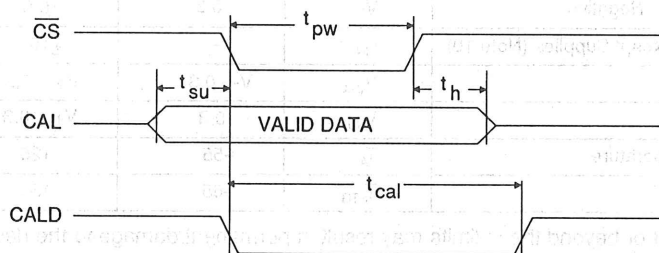
Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V <sub>IH</sub>	2.0	1.7	-	V
Low-Level Input Voltage	V <sub>IL</sub>	-	1.6	0.8	V
High-Level Output Voltage (Note 9)	V <sub>OH</sub>	(V+) - 1.0V	-	-	V
Low-Level Output Voltage, I <sub>out</sub> =1.6mA	V <sub>OL</sub>	-	-	0.4	V
Input Leakage Current	I <sub>in</sub>	-	-	10	uA

### SWITCHING CHARACTERISTICS (T<sub>A</sub> = T<sub>min</sub> to T<sub>max</sub>; V+ = 5V±10%; V- = -5V±10%)

Parameter	Symbol	Min	Typ	Max	Units
CAL to $\overline{\text{CS}}$ Setup Time	t <sub>su</sub>	20	5	-	ns
$\overline{\text{CS}}$ to CAL Hold Time	t <sub>h</sub>	20	5	-	ns
$\overline{\text{CS}}$ Pulse Width	t <sub>pw</sub>	100	50	-	ns
$\overline{\text{CS}}$ Low and CAL High to CALD High	t <sub>cal</sub>	-	500	-	ms

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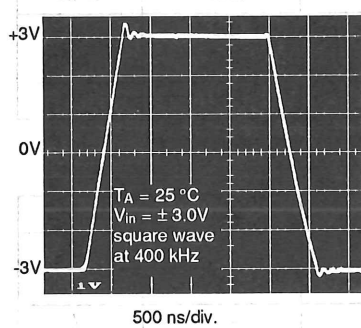
- Notes:
1. Applies after calibration at any temperature within the specified temperature range.
  2. Applies over specified temperature range without recalibration since calibration at 25°C.
  3. Applies over the input voltage range of -3.0V to +3.0V.
  4. Part to part.
  5. Total noise from dc to 1MHz.
  6. With 300 mV<sub>p-p</sub>, 1kHz ripple applied to V+.
  7. With 300 mV<sub>p-p</sub>, 1 kHz ripple applied to V-.
  8. All voltages with respect to ground.
  9. I<sub>out</sub> = -100uA. This specification guarantees TTL compatability (V<sub>OH</sub> = +2.4V @ I<sub>out</sub> = -40uA).



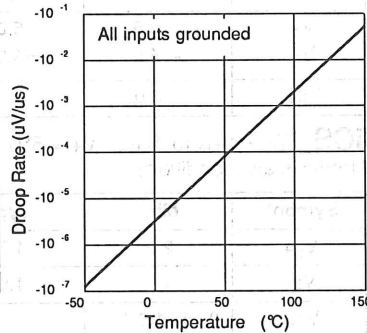
CS3112 Timing Diagram

## TYPICAL PERFORMANCE CHARACTERISTICS

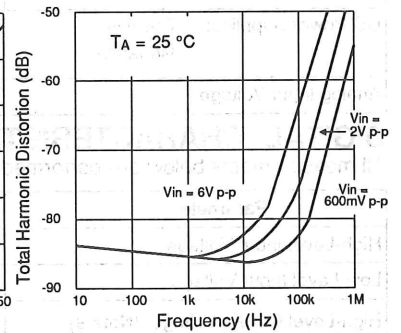
(V<sub>+</sub> = +5.0V, V<sub>-</sub> = -5.0V)



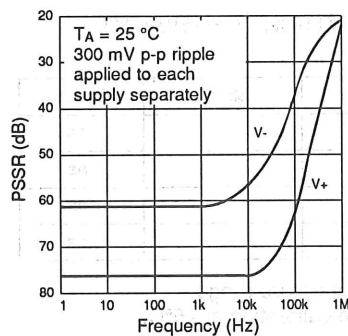
Full Scale Acquisition



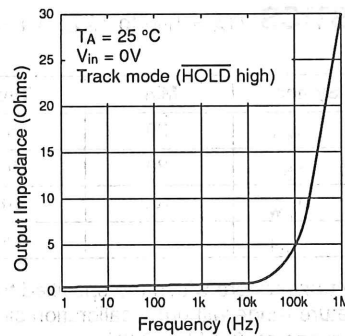
Drop Rate vs. Temperature



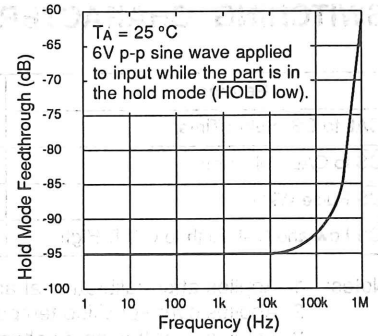
Distortion vs. Frequency



PSSR vs. Frequency



Output Impedance vs. Frequency



Hold Mode Feedthrough vs.  
Frequency

## ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground).

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive	V <sub>+</sub>	-0.3	6.0	V
DC Power Supplies: Negative	V <sub>-</sub>	0.3	-6.0	V
Input Current, Any Pin Except Supplies (Note 10)	I <sub>IN</sub>	-	±10	mA
Analog Input Voltage	V <sub>INA</sub>	V <sub>-</sub> - 0.3	V <sub>+</sub> + 0.3	V
Digital Input Voltage	V <sub>IND</sub>	-0.3	V <sub>+</sub> + 0.3	V
Ambient Operating Temperature	T <sub>A</sub>	-55	125	°C
Storage Temperature	T <sub>STG</sub>	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

Note: 10. Transient currents of up to 100mA will not cause SCR latch-up. Maximum power supply pin current is ±100 mA.



### GENERAL DESCRIPTION

The CS3112 consists of a complete track-and-hold amplifier with on-chip hold capacitor, an output buffer, and calibration circuitry. Use of an on-chip buffer isolates the track-and-hold amplifier from load conditions for optimal performance, and the calibration circuitry nulls out error sources. The CS3112 requires no external components or manual trims of any kind to achieve 12-bit performance.

The CS3112 can be controlled through its on-board microprocessor interface, or can be operated independently. Unique auto-calibration circuitry nulls any dynamic or dc error introduced between the analog input pin and the buffer's output.

### Calibration

In the calibration mode, an internal micro-controller and special nulling circuitry reduce all errors at the VOUT pin. The controller disconnects the input signal and switches a known reference voltage (AGND) to the input of the track-and-hold amplifier. This voltage is captured on the internal hold capacitor, and a DAC is adjusted to remove any error. Thus, all internal errors, including dc offset and dynamic errors due to charge injection (hold pedestal), are trimmed. During tracking, there may be up to  $\pm 55\text{mV}$  of offset.

At power-up, the user must calibrate the device. Calibration is achieved by bringing the CAL input high with  $\overline{\text{CS}}$  low. (In the stand-alone mode,  $\overline{\text{CS}}$  is grounded, so only the CAL pin needs to be pulsed.) Calibration can be similarly initiated during operation at any time, thus insuring accuracy under any conditions.

During the calibration cycle (which takes about 500ms to complete) the CALD pin remains low. During this period, any load on VOUT must remain constant; otherwise, errors could be introduced which might affect accuracy. If a new calibration is initiated before the current calibration is finished, the CS3112 will complete the current calibration before initiating the new one. CALD will go high when calibration is finished.

### Digital Interface

The CS3112 includes a digital interface designed for maximum flexibility. In a microprocessor-controlled application, the  $\overline{\text{CS}}$  control input is usually derived from a decoded address as well as write and strobe signals from the control bus (see Figure 1a). Calibration initiation thereby involves writing to the CS3112's address using a data bit to control CAL. For microprocessor-independent operation,  $\overline{\text{CS}}$  is tied low and the digital inputs are controlled by externally-latched signals (see Figure 1b).

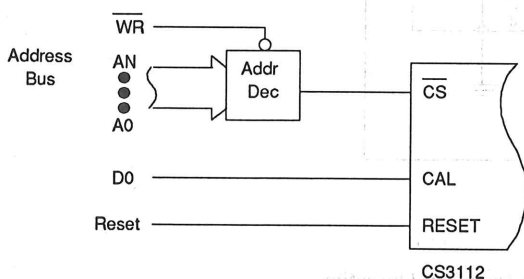


Figure 1a. CPU-Control

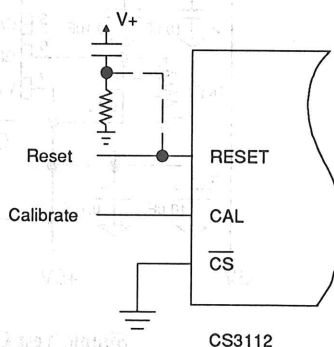


Figure 1b. Independent Control

The CS3112's CALD output can be used to generate an interrupt indicating that calibration has been completed. Alternatively, calibration status can be polled in software by connecting CALD to the data bus via a three-state buffer.

## Reset

The CS3112 must be reset after power up to ensure correct operation. The CS3112 is reset when the RESET pin is high for at least 1 $\mu$ s. An RC network attached to the RESET pin will reset the part (See Figure 1b).

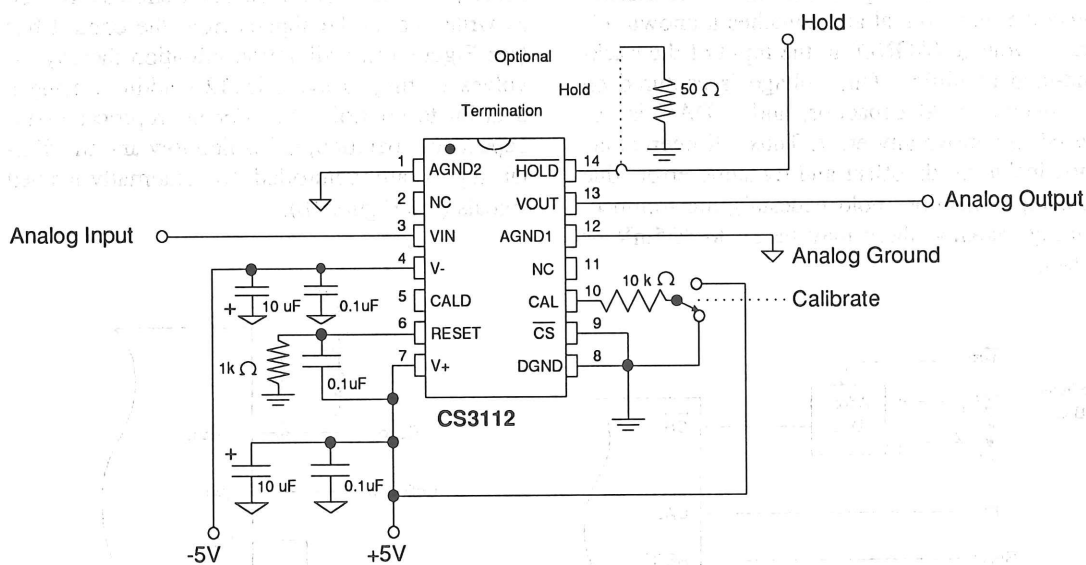
## Power Supplies and Input Connections

The CS3112 uses the analog ground voltage (AGND1) only as a reference voltage. No signal or dc power currents flow through the AGND1 connection, and it is completely independent of DGND. Both the analog input and output are referenced to the AGND1 pin internally, and

this pin needs to be at the same potential as the entire system's analog ground plane to minimize offset errors induced by noise between the AGND1 pin and the system analog ground.

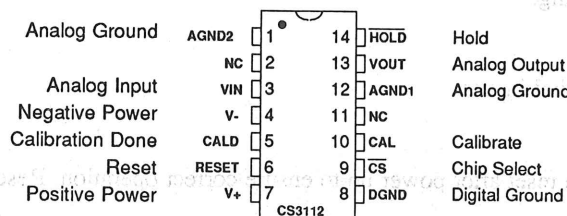
Decoupling should be performed between the V+, V- pins and AGND1 using 0.1 $\mu$ F ceramic capacitors. If significant low frequency noise is present on the supplies, 10 $\mu$ F tantalum capacitors are recommended in parallel with the 0.1 $\mu$ F capacitors. *The decoupling capacitors should be placed as close to the CS3112's power supply pins as possible.*

The signal source impedances which drive the input of the CS3112 should be minimized as much as possible. Low source impedance reduces the sensitivity of the input pin to picking up capacitively-coupled energy from logic level transitions, such as HOLD going low.



Simple Test Connections - Independent Operation

### PIN DESCRIPTION



### Analog Input and Output

#### VIN - Analog Input, PIN 3

Analog input to the track-and-hold amplifier.

#### VOUT - Analog Output, PIN 13

Buffered output from the track-and-hold.

### Power Supplies

#### V+ - Positive Power, PIN 7

Most positive supply voltage. Nominally +5 volts.

#### V- - Negative Power, PIN 4

Most negative supply voltage. Nominally -5 volts.

#### DGND - Digital Ground, PIN 8

Digital ground.

#### AGND1, AGND2 - Analog Ground, PIN 12, PIN 1

Analog ground reference.

### Digital Inputs and Outputs

#### HOLD - Hold, PIN 14

A falling transition on this pin switches the track-and-hold amplifier to the hold mode. When brought high, the track-and-hold is switched to the track mode, and acquires and then tracks the input signal.

#### CAL - Calibrate, PIN 10

When taken high with  $\overline{CS}$  low, initiates a full internal calibration.

**CALD - Calibration Done, PIN 5**

Indicates calibration status. If CALD is high the device has finished calibration. If CALD is low, the device is calibrating.

**CS - Chip Select, PIN 9**

Enables the CAL digital inputs.

**RESET - Reset, PIN 6**

The CS3112 must be reset after power up to ensure correct operation. Reset occurs when RESET is high.

**NC - No Connect, PINS 2,11**

No connection should be made to these pins.

**ERROR DEFINITIONS**

**Total Offset**

The difference between the analog input voltage and the voltage at the output pin after the hold command has been issued and all transients have settled. Applies only in the hold mode, not while tracking the analog inputs. Includes all internal offsets, including those due to charge injection (hold pedestals). Units in millivolts.

**Nonlinearity**

The deviation from a straight line on the plot of output vs input. Nonlinearity is specified as the change in *Total Offset* over the signal range of -3V to +3V. Units in millivolts.

**Gain Error**

Calculated as the difference between the errors resulting from a -3V and a +3V dc input signal, relative to a 6V input range. Units in percent of full scale.

**Acquisition Time**

The time required after the negation of the hold command ( $\overline{\text{HOLD}}$  high) for the track-and-hold amplifier to reach its final value to within a specified error band ( $\pm 0.01\%$  or  $\pm 0.1\%$ ). This determines the minimum time allowed before reassertion of the hold command. Units in microseconds.

**Track-to-Hold Settling**

The time required after the hold command is given for the output buffer amplifier to reach its final value to within a specified error band ( $\pm 0.01\%$ ). Includes switch delay (aperture) time. Units in microseconds.

**Aperture Time**

The delay after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

**Aperture Jitter**

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

**Droop Rate**

The change in the output voltage over time while in the hold mode. Units in microvolts per microsecond.

**Large Signal Bandwidth**

The frequency at which the output amplitude is 3dB below the input amplitude while tracking a full scale 6V p-p sine wave. Units in megahertz.

**Small Signal Gain Bandwidth**

The frequency at which the output amplitude is 3dB below the input amplitude while tracking a 60mV p-p sine wave. Units in megahertz.

## •Notes•

The range of variation in the speed of light is very small, and is almost negligible. The speed of light in a vacuum is about 300,000 km/s. This is the speed of light in a vacuum, and is the same in all media.

The speed of light in a medium is less than the speed of light in a vacuum. This is because the light is slowed down by the medium. The speed of light in a medium is given by the refractive index of the medium.

The refractive index of a medium is a measure of how much the speed of light is slowed down by the medium. It is defined as the ratio of the speed of light in a vacuum to the speed of light in the medium.

The refractive index of a medium is a function of the wavelength of the light. This is because the speed of light in a medium is a function of the wavelength of the light. The refractive index of a medium is given by the equation:

## 4 Channel Simultaneous Track and Hold

### Features

- Completely Self-Contained  
Four Track-and-Hold Amplifiers  
On-Chip Hold Capacitors  
Two Output Buffer Amplifiers  
Microprocessor Interface
- 800ns Acquisition Time to 0.01%
- Low Aperture Jitter: 100ps
- 12-Bit Linearity
- Total Offset Including Hold  
Pedestal: 2.8mV
- Low Droop Rate: 0.001uV/us
- Auto-Calibration Insures Accuracy Over  
Time and Temperature
- Low Power Dissipation: 250mW

### General Description

The CS31412 is a four-channel track and hold capable of processing four single-ended or two differential inputs with 12-bit linearity. It consists of four track-and-hold amplifiers, an analog multiplexer, two output buffers, and a microprocessor interface.

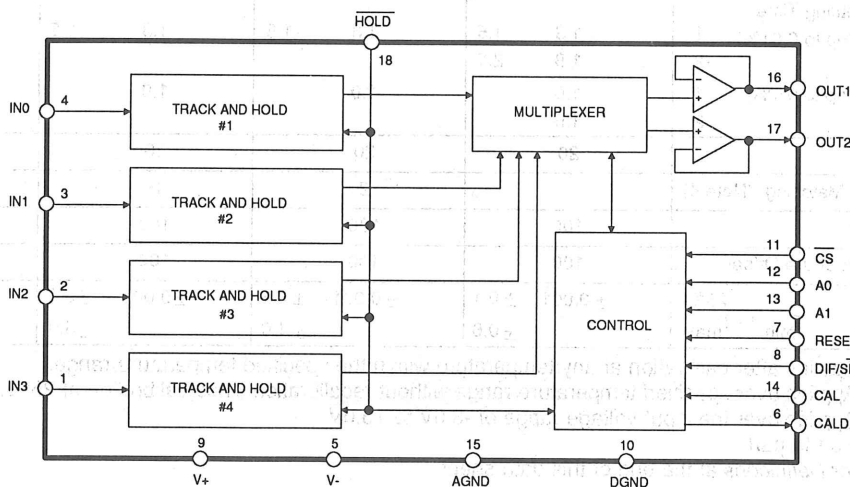
Controlled by a single **HOLD** input, the four track-and-hold amplifiers can simultaneously hold their outputs with only 100ps of aperture jitter and later acquire their inputs within 800ns to 0.01%. On-chip hold capacitors limit droop to 0.001uV/us, and first order leakage compensation minimizes droop over temperature.

The CS31412 can be configured, controlled, and monitored through its microprocessor interface, or can be operated independently of intelligent control.

### ORDERING INFORMATION:

Model	Acquisition Time	Temp. Range	Package
CS31412-KC2	2.0 $\mu$ s	0 to 70°C	18-pin Ceramic SB DI
CS31412-KC1	1.0 $\mu$ s	0 to 70°C	18-pin Ceramic SB DI
CS31412-BC1	1.0 $\mu$ s	-40 to +85°C	18-pin Ceramic SB DI
CS31412-TC1	1.0 $\mu$ s	-55 to +125°C	18-pin Ceramic SB DI

4





## ANALOG CHARACTERISTICS

(T<sub>A</sub> = 25°C, V<sub>+</sub> = +5.0V, V<sub>-</sub> = -5.0V, R<sub>L</sub> = 10kΩ, C<sub>L</sub> = 50pF, Analog Source Impedance = 40Ω, unless otherwise specified)

Parameter*	CS31412-K			CS31412-B			CS31412-T			Units
	min	typ	max	min	typ	max	min	typ	max	
Specified Temperature Range	0 to +70			-40 to +85			-55 to +125			°C
Accuracy										
Total Offset (Note 1) 25°C T <sub>min</sub> to T <sub>max</sub>	-2.8 ± 4.0 ± 4.5			-2.8 ± 4.0 ± 5.0			-2.8 ± 4.0 ± 5.0			mV mV
Total Offset Matching T <sub>min</sub> to T <sub>max</sub> Channels 0-2	0.25			0.25			0.25			mV
Channels 0-3	1.00			1.00			1.00			mV
Offset Drift (Note 2) T <sub>min</sub> to T <sub>max</sub>	± 0.020			± 0.025			± 0.030			mV/°C
Tracking Offset	± 55			± 55			± 55			mV
Nonlinearity (Note 3) 25° C T <sub>min</sub> to T <sub>max</sub>	± 1.4 ± 0.5			± 1.4 ± 0.5			± 1.4 ± 0.5			mV mV
Gain Error (Note 3) 25° C T <sub>min</sub> to T <sub>max</sub>	± 0.05 ± 0.05			± 0.05 ± 0.05			± 0.05 ± 0.05			% FS % FS
Dynamic Characteristics										
Acquisition Time (6V step to 0.01%) -1 -2 (6V step to 0.1%) -1 -2	0.8 1.0 1.6 2.0 0.6 1.2			0.8 1.0  0.6			0.8 1.0  0.6			us us us us
Track to Hold Settling to 0.01%	0.5 0.8			0.5 0.8			0.5 0.8			us
Mux Output Settling Time (6V step to 0.01%) -1 -2 (6V step to 0.1%) -1 -2	1.3 1.5 1.8 2.5 1.0 1.5			1.3 1.5  1.0			1.3 1.5  1.0			us us us us
Aperture Time	20			20			20			ns
Aperture Time Matching (Note 4)	2			2			2			ns
Aperture Jitter	100			100			100			ps
Interchannel Aperture Offset	100			100			100			ps
Droop Rate 25°C T <sub>min</sub> to T <sub>max</sub>	± 0.001 ± 0.1 ± 0.6			± 0.001 ± 0.1 ± 1.0			± 0.001 ± 0.1 ± 5.0			uV/us uV/us

- Notes:
1. Applies after calibration at any temperature within the specified temperature range.
  2. Applies over specified temperature range without recalibration since calibration at 25°C.
  3. Applies over the input voltage range of -3.0V to +3.0V.
  4. Part to part.

\* Refer to *Error Definitions* at the end of this data sheet.

**ANALOG CHARACTERISTICS** (Continued)

Parameter*	CS31412-K			CS31412-B			CS31412-T			Units
	min	typ	max	min	typ	max	min	typ	max	
Analog Input										
Large Signal Bandwidth (6V p-p Input)		2			2			2		MHz
Small Signal Gain Bandwidth (60mV p-p Input)		2.5			2.5			2.5		MHz
Output Slew Rate		10			10			10		V/us
Interchannel Isolation (Note 5)		90			90			90		dB
Input Impedance (dc)		100			100			100		MΩ
Input Capacitance		4			4			4		pF
Input Bias Current		100			100			100		pA
Analog Output										
Noise										
Track Mode (Note 6)		50			50			50		μV <sub>rms</sub>
Hold Mode (Note 7)		33			33			33		μV <sub>rms</sub>
Output Impedance at dc (Hold Mode) (Note 8)		0.1			0.1			0.1		Ω
Power Supplies										
Power Supply Currents										
Positive		25	45		25	45		25	45	mA
Negative		-25	-45		-25	-45		25	-45	mA
Power Supply Rejection Ratio										
Positive (Note 9)		75			75			75		dB
Negative (Note 10)		60			60			60		dB

- Notes:
5. With a 100kHz input signal.
  6. Total noise from dc to 1MHz.
  7. Total noise from dc to 1MHz.
  8. Applies over the input voltage range of -3V to +3V.
  9. With 300mV p-p, 1kHz ripple applied to V<sub>+</sub>.
  10. With 300mV p-p, 1kHz ripple applied to V<sub>-</sub>.

Parameter	Min	Max
V <sub>+</sub>	-0.3	0.3
V <sub>-</sub>	-0.3	0.3
V <sub>in</sub>	-0.3	0.3
V <sub>out</sub>	-0.3	0.3
V <sub>in</sub>	-0.3	0.3
V <sub>out</sub>	-0.3	0.3
V <sub>in</sub>	-0.3	0.3
V <sub>out</sub>	-0.3	0.3
V <sub>in</sub>	-0.3	0.3
V <sub>out</sub>	-0.3	0.3

Specifications are subject to change without notice.

**SWITCHING CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ;  $V_+ = 5V \pm 10\%$ ;  $V_- = -5V \pm 10\%$ )

Parameter	Symbol	Min	Typ	Max	Units
A0, A1, DIF/SE, CAL to CS Setup Time	$t_{su}$	20	5	-	ns
CS to A0, A1, DIF/SE, CAL Hold Time	$t_h$	20	5	-	ns
CS Pulse Width	$t_{pw}$	100	50	-	ns
CS Low and CAL High to CALD High	$t_{cal}$	-	500	-	ms

**DIGITAL CHARACTERISTICS** ( $T_A = T_{min}$  to  $T_{max}$ ;  $V_+ = 5V \pm 10\%$ ;  $V_- = -5V \pm 10\%$ )

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	$V_{IH}$	2.0	1.7	-	V
Low-Level Input Voltage	$V_{IL}$	-	1.6	0.8	V
High-Level Output Voltage (Note 11)	$V_{OH}$	$V_+ - 1.0V$	-	-	V
Low-Level Output Voltage $I_{out} = 1.6mA$	$V_{OL}$	-	-	0.4	V
Input Leakage Current	$I_{in}$	-	-	10	$\mu A$

Note: 11.  $I_{out} = -100\mu A$ . This specification guarantees TTL compatibility ( $V_{OH} = 2.4V$  @  $I_{out} = -40\mu A$ ).

**RECOMMENDED OPERATION CONDITIONS** ( $AGND, DGND = 0V$ , see note 12).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive	$V_+$	4.5	5.0	5.5	V
Negative	$V_-$	-4.5	-5.0	-5.5	V
Analog Input Voltage:	$V_{IN}$	-3.0	-	3.0	V

Note: 12. All voltages with respect to ground.

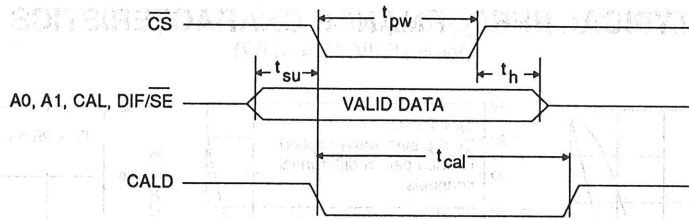
**ABSOLUTE MAXIMUM RATINGS** ( $AGND, DGND = 0V$ , All voltages with respect to ground)

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive	$V_+$	- 0.3	6.0	V
Negative	$V_-$	0.3	- 6.0	V
Input Current, Any Pin Except Supplies (Note 13)	$I_{in}$	-	$\pm 10$	mA
Analog Input Voltage	$V_{INA}$	$V_- - 0.3$	$V_+ + 0.3$	V
Digital Input Voltage	$V_{IND}$	- 0.3	$V_+ + 0.3$	V
Ambient Operating Temperature	$T_A$	- 55	125	$^{\circ}C$
Storage Temperature	$T_{stg}$	- 65	150	$^{\circ}C$

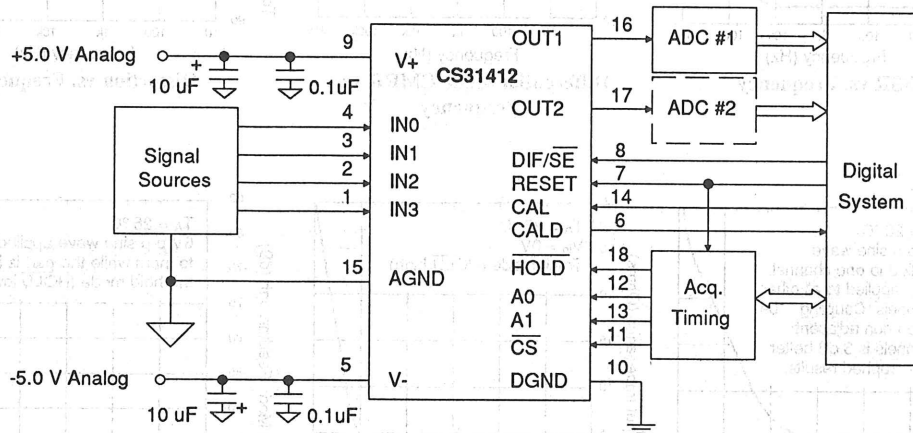
WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

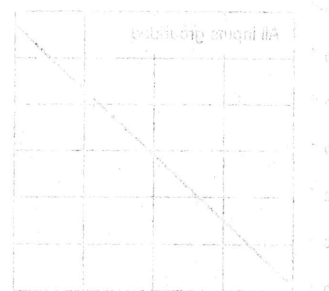
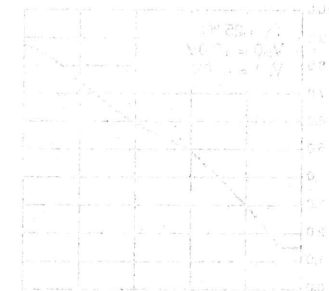
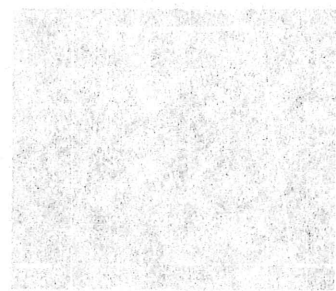
Note: 13. Transient currents of up to 100mA will not cause SCR latch-up. Maximum power supply pin current is  $\pm 100$  mA.



**Timing Diagram**

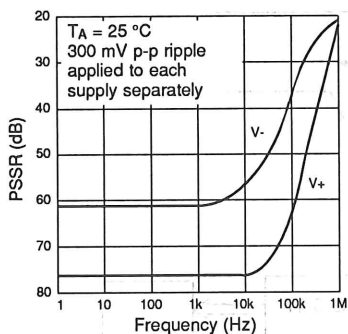


**System Connection Diagram**

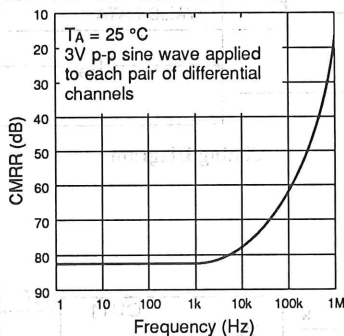


# TYPICAL PERFORMANCE CHARACTERISTICS

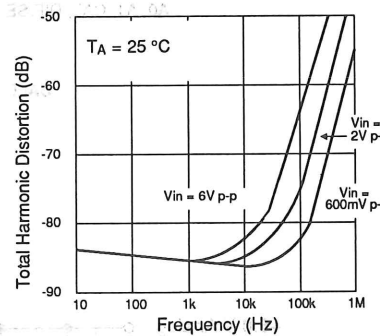
( $V_+ = +5.0V$ ,  $V_- = -5.0V$ )



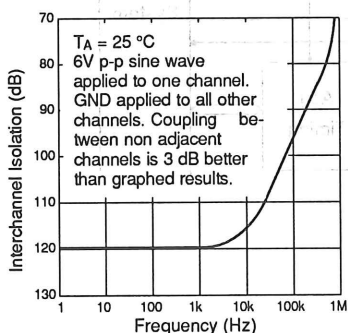
**PSSR vs. Frequency**



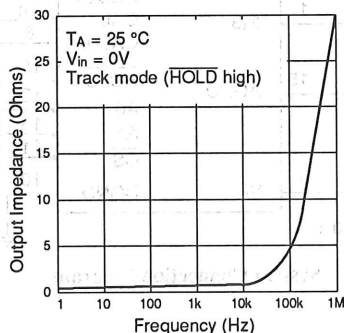
**Differential Mode CMRR vs. Frequency**



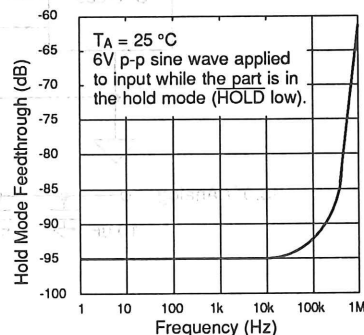
**Distortion vs. Frequency**



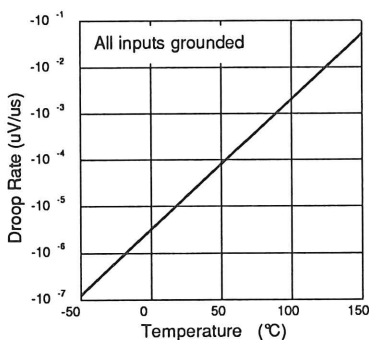
**Interchannel Isolation vs. Frequency**



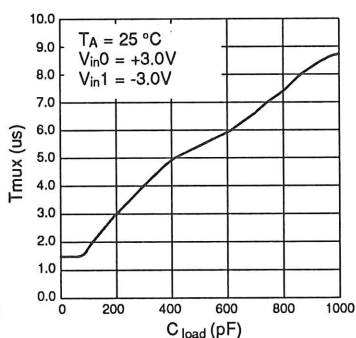
**Output Impedance vs. Frequency**



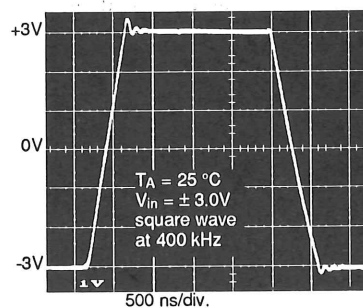
**Hold Mode Feedthrough vs. Frequency**



**Droop Rate vs. Temperature**



**Output MUX Settling Time vs. Load Capacitance**



**Full Scale Acquisition**

### GENERAL DESCRIPTION

The CS31412 consists of four track-and-hold amplifiers with on-chip hold capacitors, an analog multiplexer, and two output buffers. The CS31412 requires no external components or manual trims, and thus eliminates the task of error budgeting several components with complex (and often hidden) error sources.

The CS31412 can handle either four single-ended or two differential analog signals. The device is controlled through its on-board microprocessor interface, or it can be operated independently of intelligent control. Unique auto-calibration circuitry nulls any dynamic or dc error introduced between the analog input pin and the buffer's output for each channel.

#### Analog Multiplexer

The analog multiplexer takes the outputs of the four track-and-hold amplifiers and passes the selected outputs to the OUT1 and OUT2 pins. When  $DIF/\overline{SE}$  is low, the multiplexer is configured as a four-to-one multiplexer and each amplifier is treated as a single-ended analog input referenced to AGND. When  $DIF/\overline{SE}$  is high, the multiplexer is configured as dual two-to-one multiplexers and the track-and-hold amplifiers are treated as two groups of two amplifiers which al-

lows the CS31412 to process differential signals. This option can also be used to increase system throughput by using the CS31412 with two A/D converters (see System Throughput). Table 1 shows the multiplexer and buffer amplifier configurations as determined by the  $DIF/\overline{SE}$  pin and the address pins, A0 and A1. In the differential mode, the A0 input should be tied low to avoid floating the output buffer amplifiers. In addition, the buffer amplifier at OUT2 in the single-ended mode does not float; its output remains within 50mV of AGND and must remain unconnected.

#### Calibration

The CS31412 features on-chip digital intelligence and measurement circuitry capable of calibrating all four input channels. For each channel, the device internally deselects the input signal and switches a known reference voltage (AGND) to the input of the track-and-hold amplifier. In the calibration mode, the CS31412 uses an internal microcontroller and special nulling circuitry to reduce all errors at the OUT1 and OUT2 pins. Thus, all internal errors including dc offsets and dynamic errors due to charge injection (hold pedestal) are trimmed. The output of the CS31412 is only corrected for offset during the hold mode ( $\overline{HOLD}$  low). During tracking, each channel may have up to  $\pm 55mV$  of offset.

The user must initiate a calibration to initially calibrate the device. This is achieved by bringing the CAL input high and  $\overline{CS}$  low. Calibration can be similarly initiated during operation at any time thus insuring accuracy under any conditions. During the calibration cycle (which takes about 500 ms to complete) the CALD pin remains low. During this period, any load on OUT1 and OUT2 must remain constant; otherwise, errors could be introduced which might affect accuracy. If a new calibration is initiated before the current calibration is finished, the CS31412 will complete the current calibration before initiating the new one. CALD will go high when calibration is finished.

$DIF/\overline{SE}$	A1	A0	OUT1	OUT2
0	0	0	IN0	0V*
0	0	1	IN1	0V*
0	1	0	IN2	0V*
0	1	1	IN3	0V*
1	0	0	IN0	IN1
1	0	1	N/A**	N/A**
1	1	0	IN2	IN3
1	1	1	N/A**	N/A**

\* AGND  $\pm 50mV$

\*\* Indeterminate Output: A0 should be tied low in differential mode

Table 1. Truth Table of MUX Configurations

The DIF/SE input to the CS31412 must be in the correct state when initiating a calibration since the offsets of the analog output buffers are also calibrated. If the part is switched between the single ended and differential modes during operation, a new calibration must be initiated to guarantee that the Total Offset specification is met.

### Digital Interface

The CS31412 includes a digital interface designed for maximum flexibility. The digital inputs, A0, A1, CAL, and DIF/SE, are internally gated with CS. The input latches for the A0 and A1 inputs are level sensitive and latch on the rising edge of CS. Any state changes on these pins while CS is low appear at the output(s). In a microprocessor-controlled application, the CS control input is usually derived from a decoded address as well as write and strobe signals off of the control bus (Figure 1a). Channel selection and calibration initiation thereby involve writing to the CS31412's address using data bits to control A0, A1, CAL, and DIF/SE. For microprocessor-independent operation in single-ended mode, CS is tied low and the digital inputs are controlled by externally-latched signals (Figure 1b).

The CS31412's CALD output can be used to generate an interrupt indicating the CS31412 has completed calibration. Alternatively, calibration

status can be polled in software by connecting CALD to the data bus via a 3-state buffer.

### Reset

The CS31412 must be reset after power up to ensure correct operation. The reset function is invoked by bringing the RESET pin high for at least 1  $\mu$ s. An RC network attached to the RESET pin will reset the part (See Figure 1b).

### System Throughput

Throughput of the CS31412 varies depending on the number of input signals used. System timing diagrams which enable the throughput of the CS31412 to be calculated are shown in Figure 2. Table 2 is a listing of throughput times for the number of input channels used. These times assume that no time is required for A/D conversion. When the part is used in the differential mode, throughput time will be equal to the two channel throughput time.

Since one of the four channels must be connected to the output buffer, the Track-to-Hold settling time ( $t_{th}$ ) is included in the first channel's settling time ( $t_1$ ). The address inputs A0, and A1 must be switched before the part is put in the hold mode (HOLD low) so that the first channel's output is valid at time ( $t_1$ ). After the first output is settled,

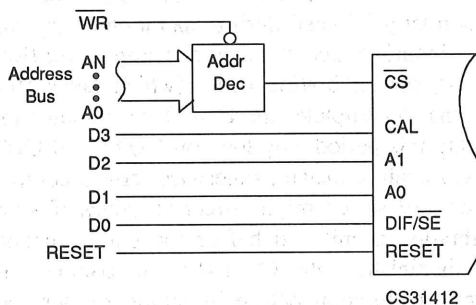


Figure 1a. CPU-Control

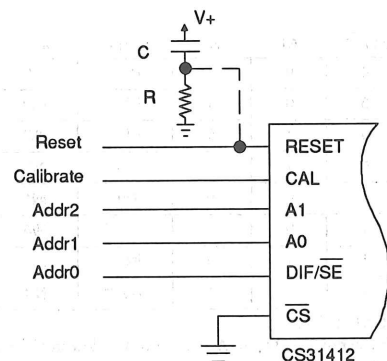


Figure 1b. CPU-Independent Control



the addresses can be used to mux each of the other three channels to the output.

Single Channel	Two Channels	Three Channels	Four Channels
2.70us	4.20us	5.71us	7.19us

**Table 2. Throughput Time**

When interfacing the CS31412 with an A/D converter which includes an integrated sample/hold, such as Crystal's CS501X series, additional reduction in throughput time can be obtained by pipelining settling times. As soon as the A/D has captured the output of the CS31412, **HOLD** can be brought high and the CS31412 can acquire the new input signals and settle the first muxed channel while the A/D is converting. Likewise, output mux settling for all other other channels can be pipelined during conversion removing all of the CS31412's timing from the throughput equation. System throughput can therefore proceed at the ADC's maximum throughput. Using the CS31412 in the differential mode with two ADCs will reduce throughput time further because two channels can be converted simultaneously.

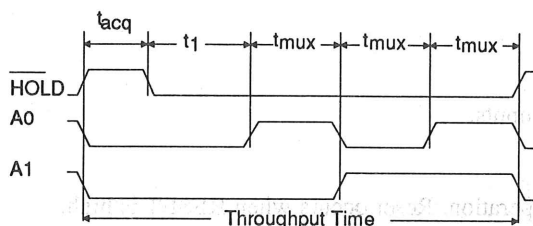
### Power Supplies and Input Connections

The CS31412 uses the analog ground voltage (AGND) only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on AGND relative to the system's analog ground plane will result in

offset errors. Therefore, the analog inputs should be referenced to the AGND pin which should be used as the entire system's analog ground. Decoupling should be performed between the V+, V- pins and AGND using 0.1uF ceramic capacitors. If significant low frequency noise is present on the supplies, 10uF tantalum capacitors are recommended in parallel with the 0.1uF capacitors. *The decoupling capacitors should be placed as close to the CS31412's power supply pins as possible.*

The signal source impedances which drive the four input channels of the CS31412 should be minimized as much as possible. Low source impedance reduces the sensitivity of the input pins to picking up capacitively-coupled energy from logic level transitions, such as **HOLD** going low.

4



$t_{acq}$ : Acquisition Time  
 $t_{tth}$ : Track to Hold Settling Time  
 $t_{mux}$ : Mux Output Settling Time  
 $t_1$ : First Channel Settling Time  
 $t_1 = \sqrt{t_{tth}^2 + t_{mux}^2}$

**Figure 2. Four Channel Timing**

### PIN DESCRIPTIONS

ANALOG INPUT 3	IN3	1	18	HOLD	HOLD
ANALOG INPUT 2	IN2	2	17	OUT2	ANALOG OUTPUT 2
ANALOG INPUT 1	IN1	3	16	OUT1	ANALOG OUTPUT 1
ANALOG INPUT 0	IN0	4	15	AGND	ANALOG GROUND
NEGATIVE POWER	V-	5	14	CAL	CALIBRATE
CALIBRATION DONE	CALD	6	13	A1	ADDRESS INPUT 1
RESET	RESET	7	12	A0	ADDRESS INPUT 0
DIFF/SINGLE-ENDED	DIF/SE	8	11	CS	CHIP SELECT
POSITIVE POWER	V+	9	10	DGND	DIGITAL GROUND

### Power Supplies

#### V+ - Positive Power, PIN 9

Most positive supply voltage. Nominally +5 volts.

#### V- - Negative Power, PIN 5

Most negative supply voltage. Nominally -5 volts.

#### DGND - Digital Ground, PIN 10

Digital ground reference.

#### AGND - Analog Ground, PIN 15

Analog ground reference.

### Analog Inputs

#### IN0; IN1; IN2; IN3 - Analog Inputs 0;1;2;3, PINS 4,3,2,1

Analog inputs to the four track and hold amplifiers.

### Digital Inputs

#### CS - Chip Select, PIN 11

Enables the DIF/SE, A0, A1, and CAL digital inputs.

#### RESET - Reset, PIN 7

The CS31412 must be reset to ensure correct operation. Reset occurs when RESET is high.

## **DIF/SE - Differential/Single-Ended Select, PIN 8**

Configures the output multiplexer in either a single-ended or differential mode. It is latched on the rising edge of CS, but usually tied high or low. If set low, the four analog inputs are routed through OUT1. If set high, IN0 and IN1 are paired as one differential signal and IN2 and IN3 are paired as a second.

## **A0; A1 - Address Input 0; Address Input 1, PINS 12; 13**

Select which amplifier or amplifier pair is output on the OUT1 and OUT2 pins. A0 should be held low when DIF/SE is high to avoid floating the outputs.

## **CAL - Calibrate, PIN 14**

When taken high with CS low, initiates a full internal calibration.

## **HOLD - Hold, PIN 18**

A falling transition on this pin signals all four amplifiers to hold their inputs simultaneously. When brought high, the amplifiers acquire, and then track the input signal.

## **Analog Outputs**

### **OUT1; OUT2 - Analog Output 1; Analog Output 2, PINS 16, 17**

The buffered outputs from the multiplexer; OUT1 is always active and OUT2 is active only in the differential mode (DIF/SE high).

4

## **Digital Outputs**

### **CALD - Calibration Done, PIN 6**

Indicates calibration status. If CALD is high the device has finished calibration. If CALD is low the device is calibrating.

## **ERROR DEFINITIONS**

**Total Offset** - The difference between the analog voltage applied to the analog input (A0, A1, A2, or A3) and the signal that appears at the appropriate output pin (OUT1 or OUT2) after the hold command has been issued and all transients have settled. Applies only in the hold mode, not while tracking the analog inputs. Includes all internal offsets, including those due to charge injection (hold pedestals). Units in millivolts.

**Nonlinearity** - The deviation from a straight line on the plot of output vs input after offset error is accounted for. Nonlinearity is specified as the change in *Total Offset* over the signal range of -3V to +3V. Units in millivolts.

**Gain Error** - Calculated as the difference between the *Total Offsets* resulting from -3V and +3V dc input signals relative to a 6V input range. Units in percent of full scale.

**Acquisition Time** - The time required after the negation of the hold command ( $\overline{\text{HOLD}}$  high) for the track-and-hold amplifiers to reach their final values to within a specified error band ( $\pm 0.01\%$  or  $\pm 0.1\%$ ). Measured internally at the inputs to the multiplexer, it determines the minimum time allowed before reassertion of the hold command. Indicates nothing about the outputs as measured at OUT1 or OUT2. Units in microseconds.

**Track-to-Hold Settling** - The time required after the hold command is given for each track and hold to reach its final value to within a specified error band ( $\pm 0.01\%$ ). Includes switch delay (aperture) time but not multiplexer and output buffer settling. Units in microseconds.

**MUX Output Settling** - The time required after reconfiguring the multiplexer for the outputs at OUT1 and OUT2 to reach their final value to within a specified error band ( $\pm 0.01\%$  or  $\pm 0.1\%$ ). Measured from the falling edge of  $\overline{\text{CS}}$  with A0 and A1 valid. Units in microseconds.

**Aperture Time** - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

**Aperture Jitter** - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

**Interchannel Aperture Offset** - The range of variation in aperture time between the four track-and-hold amplifiers for a given hold command. A measure of simultaneity. Units in picoseconds.

**Droop Rate** - The change in the output voltage over time while in the hold mode. Units in microvolts per microsecond.

**Large Signal Bandwidth** - The frequency at which the output amplitude while tracking a full scale 6Vp-p sine wave is 3dB below the input amplitude. Units in megahertz.

**Small Signal Gain Bandwidth** - The frequency at which the output amplitude while tracking a 60 mVp-p sine wave is 3dB below the input amplitude. Units in megahertz.

**Interchannel Isolation** - A measure of crosstalk between input channels while in the track mode. Units in decibels.

## CS31412 Evaluation Board

### Features

- Industry Standard Header Connector
- BNC Connectors for Analog I/O's
- DIP-Switch Selectable  
Differential & Single-Ended Modes  
Analog Mux Configuration
- Push Button Reset and Calibration
- User Configurable Ground Planes

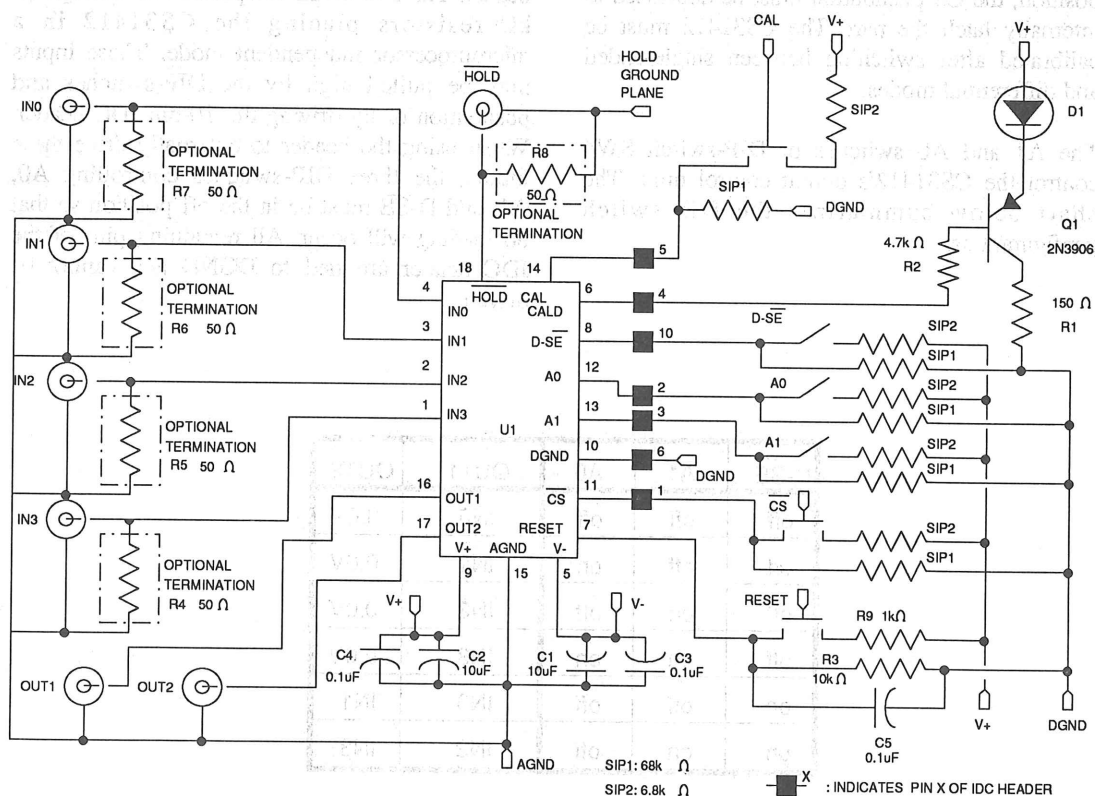
### General Description

The CDB31412 Evaluation Board is designed to allow the user to quickly evaluate the performance of the CS31412 Simultaneous Track-and-Hold.

All analog inputs and outputs can be interfaced to the board with coaxial BNC connectors. Optional termination resistors can also be added.

A 10 pin IDC header is provided for microprocessor control.

**ORDERING INFORMATION:** CDB31412



## Analog Input and Output Connections

The four analog inputs to the CS31412 are connected to the CDB31412 via the BNC coaxial connectors labeled IN0, IN1, IN2, IN3. These inputs have locations reserved for termination resistors if they are needed. The analog outputs from the CS31412 are available at the BNC coaxial connectors labeled OUT1, and OUT2.

## DIP-Switch Configuration

The input mode is controlled by the D- $\overline{\text{SE}}$  switch of DIP-switch SW4. If it is off, the part is in single-ended mode (4-to-1 mux). If it is on, the part is in the differential mode (dual 2-to-1 mux). After changing the differential mode switch position, the  $\overline{\text{CS}}$  pushbutton must be depressed to internally latch the part. The CS31412 must be calibrated after switching between single-ended and differential modes.

The A1 and A0 switches of DIP-switch SW4 control the CS31412's output control mux. The chart below summarizes the DIP-switch configurations.

## Reset and Calibration

The CS31412 will usually reset itself upon power-up. Since this function is not guaranteed, the chip must be reset upon power-up in system operation. The part can be reset on the CDB31412 board by momentarily depressing pushbutton SW3. To initiate a calibration, depress pushbutton SW1. The LED will turn on for approximately 500 ms, indicating that the part is being calibrated. Once the LED goes off, the CS31412 is ready for operation.

## Microprocessor Interface

The CAL,  $\overline{\text{CS}}$ , A0, A1, and D- $\overline{\text{SE}}$  inputs and the CALD output are available at the 10 pin IDC header. The five inputs are pulled low through 68 k $\Omega$  resistors placing the CS31412 in a microprocessor independent mode. These inputs may be pulled high by the DIP-switches and pushbutton or by driving the 10-pin IDC header. When using the header to externally drive these inputs, the three DIP-switches controlling A0, A1, and D- $\overline{\text{SE}}$  must be in the off position so that no loading will occur. All remaining pins of the IDC header are tied to DGND and cannot be driven.

D- $\overline{\text{SE}}$	A1	A0	OUT1	OUT2
off	off	off	IN0	0.0V
off	off	on	IN1	0.0V
off	on	off	IN2	0.0V
off	on	on	IN3	0.0V
on	off	off	IN0	IN1
on	on	off	IN2	IN3

Figure 1. Dip-Switch Configuration

### Decoupling

The CDB31412's decoupling scheme was designed to insure accurate evaluation of the CS31412's performance independent of the quality of the power supplies. Each supply is decoupled at the part with a 10  $\mu$ F electrolytic capacitor to filter low-frequency noise and a 0.1  $\mu$ F ceramic capacitor to handle higher frequencies. Depending on the quality of the system's power supplies, the decoupling scheme could be relaxed in actual use.

### Ground Planes

The CDB31412 has three separate ground planes which may be interconnected by the user to simulate actual system conditions. When shipped from the factory, the analog ground plane, the digital ground plane, and the hold ground plane are separate. Jumpers J1, J2, J3, and J4 are used to interconnect these ground planes. Separate ground planes are the suggested configuration for best performance of the part. For more information on grounding, Application Note: "Suggested Grounding and Supply Arrangements for the CS31412" is recommended.

### COMPONENT LIST

150 $\Omega$ resistor	R1
4.7 k $\Omega$ resistor	R2
10 k $\Omega$ resistor	R3
1 k $\Omega$ resistor	R9
68.0 k $\Omega$ sip resistor	SIP1
6.8 k $\Omega$ sip resistor	SIP2
0.1 $\mu$ F capacitor	C3, C4, C5
10 $\mu$ F capacitor	C1, C2
CS31412 Track/Hold	U1
2N3906 transistor	Q1
LED	D1
3 pos. SPST DIP switch	SW4
SPST pushbutton	SW1, SW2, SW3
10 pin header	P12
PC-mount BNC	P5, P6, P7, P8, P9, P10, P11
red banana jack	P1
black banana jack	P3, P4
green banana jack	P2
1" 4-40 spacer	POST1, POST2, POST3, POST4
3/8" 4-40 screw	SC1, SC2, SC3, SC4





# **+ 4.5V Precision Voltage Reference**

## Features

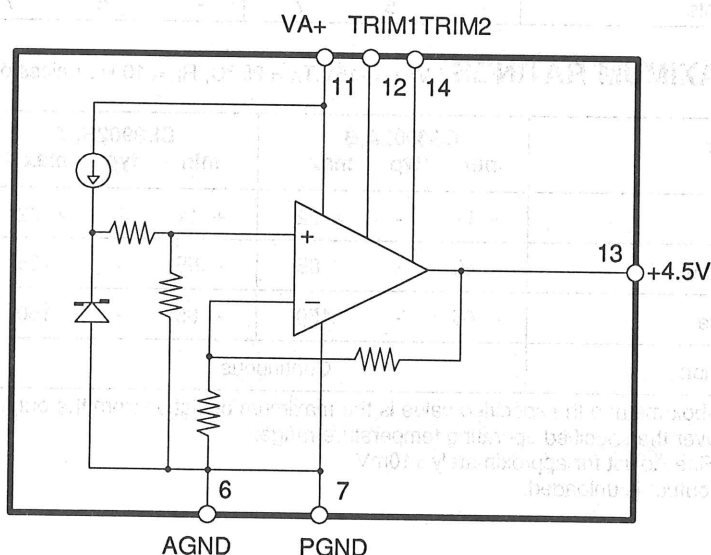
- Very High Accuracy:  $+4.500V \pm 0.4 \text{ mV}$
- Very Low Temperature Drift:  
 $\pm 0.6 \text{ ppm} / ^\circ\text{C} \text{ } -55^\circ\text{C to } +125^\circ\text{C}$
- Excellent Long-Term Stability:  
25 ppm/1000 hours
- Excellent Line Regulation: 6 ppm/V Typ.
- Designed for use with CS5012,  
CS5014, CS5016, CS5101, and  
CS5102 A/D Converters
- 14 Pin Bottom-brazed DIP Package

## General Description

The CS3902 is a precision voltage reference providing +4.500V from an input voltage of 11V to 22V. It offers very high accuracy without trimming and exhibits very low temperature drift: 1/50 LSB /  $^\circ\text{C}$  at 16 bits. Long term stability of the CS3902 is excellent. The device is suitable for all Crystal Semiconductor Successive Approximation A/D Converters.

## ORDERING INFORMATION:

Model	Initial Error	Thermal Drift	Temperature
CS3902-AC	800 $\mu\text{V}$	400 $\mu\text{V}$	$-40^\circ\text{C to } +85^\circ\text{C}$
CS3902-BC	400 $\mu\text{V}$	200 $\mu\text{V}$	$-40^\circ\text{C to } +85^\circ\text{C}$
CS3902-SC	800 $\mu\text{V}$	600 $\mu\text{V}$	$-55^\circ\text{C to } +125^\circ\text{C}$
CS3902-TC	400 $\mu\text{V}$	300 $\mu\text{V}$	$-55^\circ\text{C to } +125^\circ\text{C}$



**ANALOG CHARACTERISTICS** ( $V_{A+} = +15V$ ,  $T_A = 25^\circ C$ ,  $R_L = 10\text{ k}\Omega$  unless otherwise specified)

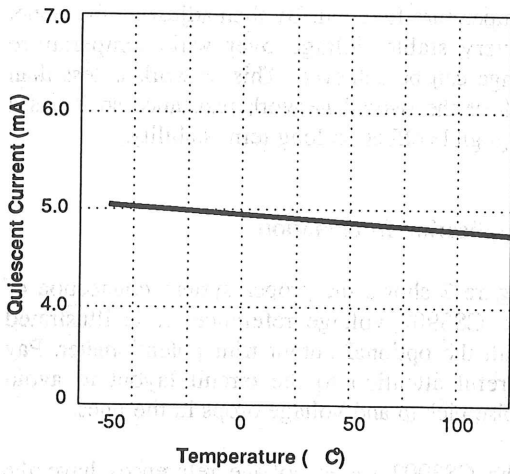
Parameter	CS3902A,B			CS3902S,T			Units
	min	typ	max	min	typ	max	
Specified Temperature Range	-40		85	-55		125	$^\circ C$
Output Voltage	-	+ 4.5	-	-	+ 4.5	-	V
Output Voltage Errors							
Initial Error -A,S	-	-	800	-	-	800	$\mu V$
-B,T	-	-	400	-	-	400	$\mu V$
Warmup Drift	-	25	-	-	25	-	$\mu V$
$T_{MIN}$ to $T_{MAX}$ (Note 1) -A,S	-	-	400	-	-	600	$\mu V$
-B,T	-	-	200	-	-	300	$\mu V$
Long-Term Stability	-	25	-	-	25	-	ppm/1000 hrs
Noise (.1 - 10 Hz)	-	5	-	-	5	-	$\mu V_{p-p}$
Output Drive	10	-	-	10	-	-	mA
Regulation							
Line	-	30	100	-	30	100	$\mu V/V$
Load	-	30	-	-	30	-	$\mu V/mA$
Output Adjustment							
Range (Note 2)	-	10	-	-	10	-	mV
Temperature coefficient	-	4	-	-	4	-	$\mu V/^\circ C/mV$
Power Supply Currents	-	5	7	-	5	7	mA

**ABSOLUTE MAXIMUM RATINGS** ( $V_{A+} = +15V$ ,  $T_A = 25^\circ C$ ,  $R_L = 10\text{ k}\Omega$  unless otherwise specified)

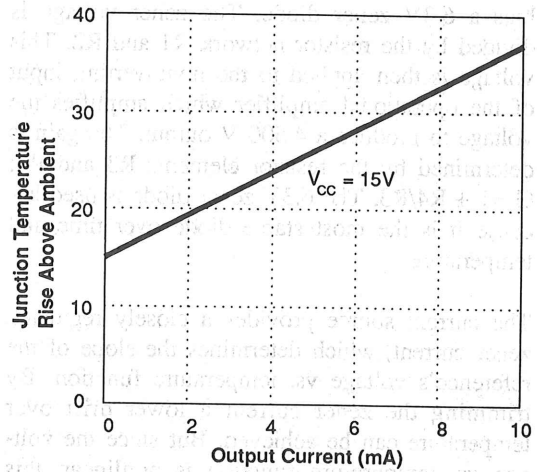
Parameter	CS3902A,B			CS3902S, T			Units
	min	typ	max	min	typ	max	
$V_{A+}$	+ 11	-	+ 22	+ 11	-	+ 22	V
Operating Temperature	- 40	-	85	- 55	-	125	$^\circ C$
Storage Temperature	- 65	-	150	- 65	-	150	$^\circ C$
Short Circuit Protection	Continuous						-

- Notes: 1. Using the box method the specified value is the maximum deviation from the output voltage at  $25^\circ C$  over the specified operating temperature range.  
2. Optional Fine Adjust for approximately  $\pm 10mV$   
3. The 4.5V output is unloaded.

Specifications are subject to change without notice.

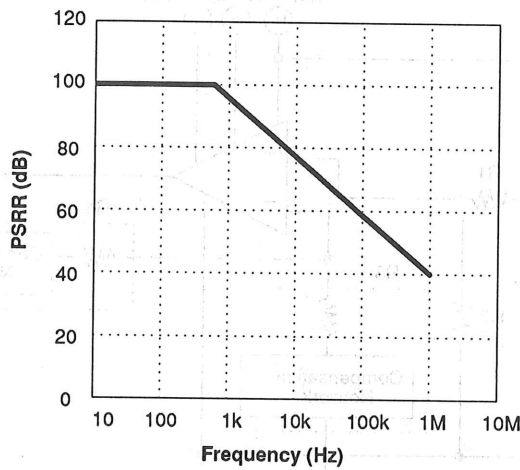


**Quiescent Current vs. Temperature**



**Junction Temperature Rise vs. Output Current**

**4**



**PSRR vs. Frequency**

## Theory Of Operation

Figure 1 illustrates the internal configuration of the CS3902. An FET current source is used to bias a 6.3V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 4.500 V output. The gain is determined by the resistor elements R3 and R4:  $G = 1 + R4/R3$ . The 6.3V zener diode is used because it is the most stable diode over time and temperature.

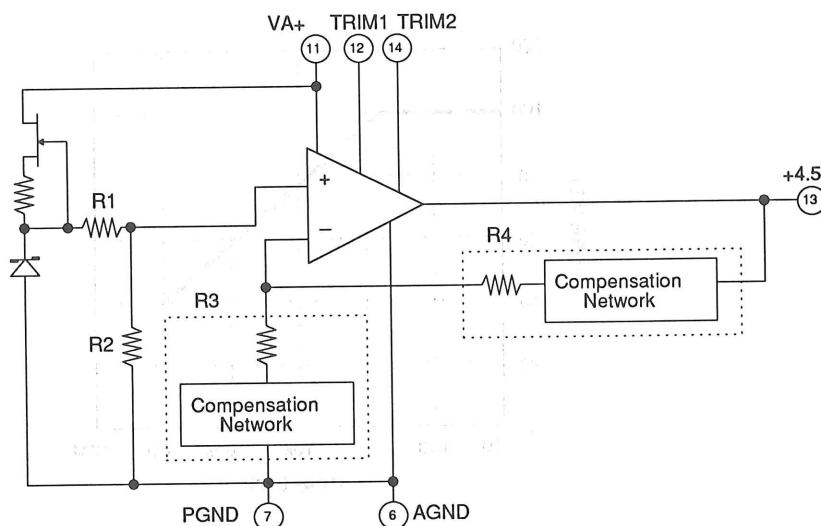
The current source provides a closely regulated zener current, which determines the slope of the reference's voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear, this method leaves a residual error over wide temperature ranges.

To remove this residual error, a nonlinear compensation network of thermistors and resistors was developed. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, a very stable voltage over wide temperature range can be achieved. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

## Application Information

Figure 2 shows the proper system connection of the CS3902 voltage reference. It is illustrated with the optional output trim potentiometer. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

The CS3902 series voltage references have the ground terminal brought out on two pins (pin 6 and pin 7) which are connected together internally. This allows the user to achieve greater



**Figure 1. CS3902 Internal Configuration**

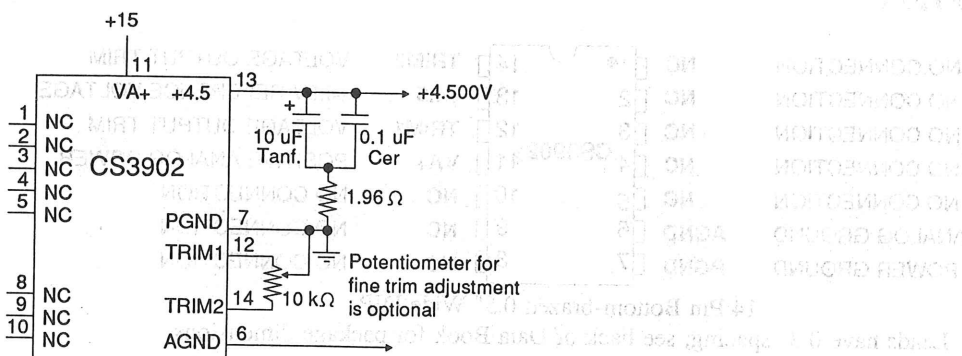


Figure 2. System Connection Diagram

accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature this voltage drop could be trimmed out. When the reference is plugged into a socket this source of error can be as high as 20 ppm. By connecting pin 7 to the power supply ground and pin 6 to a high impedance ground point in the measurement circuit the error due to the contact resistance can be eliminated. If the unit is soldered into place the contact resistance is sufficiently small that it doesn't affect performance.

See the application note "Voltage References for the CS501X/CS5101/CS5102/CS5126 Series of A/D converters" for discussion of the filtering components on the output of the CS3902.

### PIN DESCRIPTION

NO CONNECTION	NC	1	14	TRIM2	VOLTAGE OUTPUT TRIM
NO CONNECTION	NC	2	13	+4.5	+4.5V REFERENCE VOLTAGE
NO CONNECTION	NC	3	12	TRIM1	VOLTAGE OUTPUT TRIM
NO CONNECTION	NC	4	11	VA+	POSITIVE ANALOG POWER
NO CONNECTION	NC	5	10	NC	NO CONNECTION
ANALOG GROUND	AGND	6	9	NC	NO CONNECTION
POWER GROUND	PGND	7	8	NC	NO CONNECTION

14 Pin Bottom-brazed 0.5" Wide DIP

Leads have 0.3" spacing; see back of Data Book for package dimensions.



## $\pm 1.5 \text{ V}$ and $3.0 \text{ V}$ Voltage References

### Features

- High Accuracy  
CS3903: +3.0V Output @  $\pm 700 \mu\text{V}$   
CS3904:  $\pm 1.5\text{V}$  Output @  $\pm 500 \mu\text{V}$
- Low Drift
- Excellent Stability
- Operates from  $\pm 5\text{V}$
- 14-Pin Bottom-brazed DIP

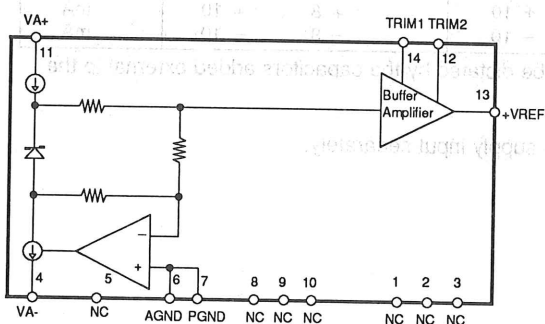
### General Description

The CS3903 and CS3904 are precision hybrid voltage references for the CS5412 A/D Converter. The devices provide either +3.0V (CS3903) or  $\pm 1.5\text{V}$  (CS3904) outputs from  $\pm 5\text{V}$  inputs. The voltage outputs do not require trimming, but trim pins are available if fine adjustments are desired. The outputs of the CS3903 and CS3904 provide low impedance, low noise and excellent temperature stability to insure optimum performance from the A/D converter.

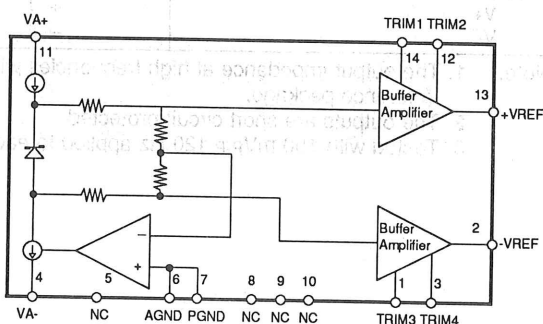
### ORDERING INFORMATION:

CS3903-KC	0 °C to 70 °C	Unipolar	+3V
CS3903-TC	- 55 °C to +125 °C	Unipolar	+3V
CS3904-KC	0 °C to 70 °C	Bipolar	$\pm 1.5\text{V}$
CS3904-TC	- 55 °C to +125 °C	Bipolar	$\pm 1.5\text{V}$

3903



3904



**ANALOG CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V_{A+} = 5\text{V}$ ,  $V_{A-} = -5\text{V}$ , VREF outputs unloaded)

Parameter	CS3903/4-K			CS3903/4-T			Units
	min	typ	max	min	typ	max	
Specified Temperature Range	0	—	70	— 55	—	125	$^\circ\text{C}$
Supply Voltage							V
$V_{A+}$	+ 4.85	+ 5.0	+ 5.5	+ 4.85	+ 5.0	+ 5.5	V
$V_{A-}$	— 5.5	— 5.0	— 4.85	— 5.5	— 5.0	— 4.85	V
+VREF Voltage (CS3903 Only)		+ 3.0			+ 3.0		V
Deviation from +3.0V:							$\mu\text{V}$
at $T_A = 25^\circ\text{C}$	— 350		+ 350	— 350		+ 350	$\mu\text{V}$
at $T_A = T_{\min}$ to $T_{\max}$	— 700		+ 700	— 700		+ 700	$\mu\text{V}$
+VREF Voltage (CS3904 Only)		+ 1.5			+ 1.5		V
Deviation from +1.5V:							$\mu\text{V}$
at $T_A = 25^\circ\text{C}$	— 175		+ 175	— 175		+ 175	$\mu\text{V}$
at $T_A = T_{\min}$ to $T_{\max}$	— 500		+ 500	— 500		+ 500	$\mu\text{V}$
-VREF Voltage (CS3904 Only)		— 1.5			— 1.5		V
Deviation from -1.5V:							$\mu\text{V}$
at $T_A = 25^\circ\text{C}$	— 175		+ 175	— 175		+ 175	$\mu\text{V}$
at $T_A = T_{\min}$ to $T_{\max}$	— 500		+ 500	— 500		+ 500	$\mu\text{V}$
Output Trim Range		$\pm 5$			$\pm 5$		mV
Output Impedance (Note 1) dc to 1000 Hz			10			10	milliohms
Output Noise dc to 1 MHz			100			100	$\mu\text{V}$ (p-p)
Output Drive (Note 2)	5			5			mA
PSRR $V_{A+}$ or $V_{A-}$ (Note 3)	70			70			dB
Long-Term Stability		25			25		ppm/1000 hr
Supply Current							mA
$V_+$		+ 8	+ 10		+ 8	+ 10	mA
$V_-$		— 8	— 10		— 8	— 10	mA

- Note:
1. The output impedance at high frequencies will be dictated by the capacitors added external to the reference package.
  2. The outputs are short circuit protected.
  3. Tested with 100 mVp-p 120 Hz applied to each supply input separately.

Specifications are subject to change without notice.

## THEORY OF OPERATION

### General Description

The CS3903 and CS3904 are hybrid voltage reference circuits which use a very low drift zener diode as a reference. The CS3903 is capable of delivering a +3.0V unipolar output voltage and the CS3904 delivers a  $\pm 1.5V$  bipolar output voltage. Each device contains an amplifier to buffer the resistor network voltage. The buffer amplifier is capable of driving up to 5 mA minimum and being loaded with up to 15  $\mu F$  of capacitance without stability problems.

The buffer output voltages do not require trimming, but are trimmable if a 10 k $\Omega$  potentiometer is appropriately connected to the trim pins. The wiper of the potentiometer should be connected to the -5V supply. TRIM1 and TRIM2 are for trimming the positive output voltage of the CS3903 and CS3904. Moving the wiper of the pot toward TRIM2 will cause the positive output to increase in magnitude. TRIM3 and TRIM4 (CS3904 only) are for trimming the negative output voltage. Moving the wiper of the potentiometer toward TRIM3 will cause the negative output to increase in magnitude.

### Power Supply Connection

The CS3903/4 are designed to operate from  $\pm 5V$  supplies. These inputs should be decoupled with 0.1  $\mu F$  ceramic capacitors located near to the part. The PGND (power ground) pin is to be used for the power supply ground return. This pin is internally connected to the AGND (analog ground) pin.

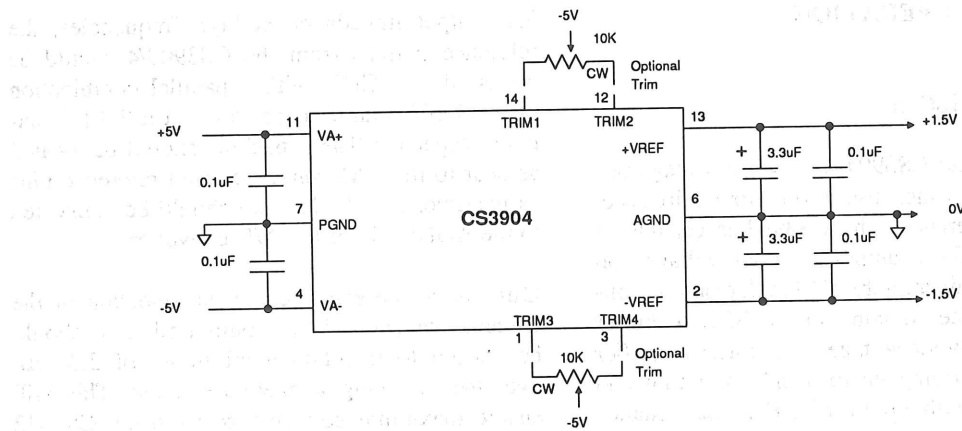
### CS3903/CS3904 System Combination

The CS3903 and CS3904 are designed to be used with the CS5412 A/D converter. The CS5412 A/D converter draws a high frequency dynamic current from the CS3903/4 outputs. To maintain

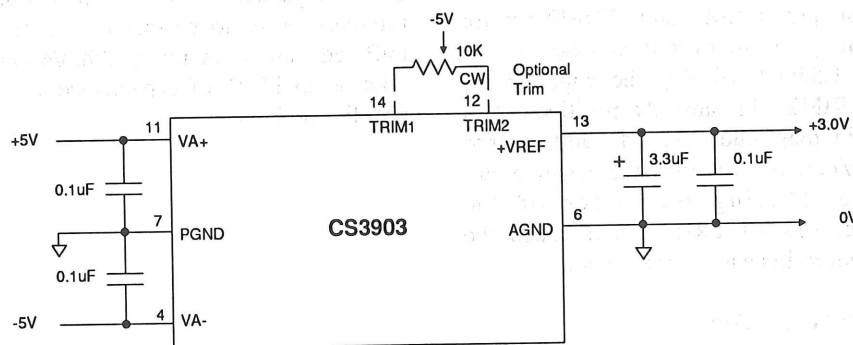
low output impedance at high frequencies, the reference outputs from the CS3903/4 should be bypassed to AGND with a parallel combination of a 0.1  $\mu F$  ceramic capacitor and a 3.3  $\mu F$  tantalum capacitor. The capacitors should be located as near to the A/D converter input reference pins as possible. The AGND pin should be connected to the AGND pin of the A/D converter.

Care should be exercised in the selection of the tantalum capacitor in the output filter. It should be chosen to maintain a minimum of 3.3  $\mu F$  over the operating temperature range. This will ensure maximum performance from the CS5412 A/D converter.

A single CS3903 or CS3904 is capable of being used to supply reference voltages to several CS5412 A/D converters. If this is done the value of the capacitance on the VREF outputs of the reference needs to be increased accordingly. The buffered outputs of the CS3903/4 can be loaded with up to 15  $\mu F$  of capacitance without causing stability problems.



**Figure 1. Bipolar Output Configuration**



**Figure 2. Unipolar Output Configuration**

### PIN DESCRIPTIONS

VOLTAGE OUTPUT TRIM	TRIM3	1	14	TRIM1	VOLTAGE OUTPUT TRIM
NEGATIVE VOLTAGE REFERENCE	-VREF	2	13	+VREF	POSITIVE VOLTAGE REFERENCE
VOLTAGE OUTPUT TRIM	TRIM4	3	12	TRIM2	VOLTAGE OUTPUT TRIM
NEGATIVE ANALOG POWER	VA-	4	11	VA+	POSITIVE ANALOG POWER
NO CONNECTION	NC	5	10	NC	NO CONNECTION
ANALOG GROUND	AGND	6	9	NC	NO CONNECTION
POWER GROUND	PGND	7	8	NC	NO CONNECTION

14-Pin Bottom-brazed 0.5" wide DIP

Leads have 0.3" spacing; see back of Data Book for package dimensions.

### Power Supply Connections

#### VA+ - Positive Analog Power, PIN 11

Positive analog power supply, nominally +5 V.

#### VA- - Negative Analog Power, PIN 4

Negative analog power supply, nominally -5 V.

#### PGND - Power Ground, PIN 7

The ground pin for the VA+ and VA- inputs. It is internally connected to AGND.

### Reference Output Pins

#### +VREF - Positive Voltage Reference output, PIN 13

Provides a positive output reference voltage with respect to the AGND pin. The magnitude can be either +1.5 V in the CS3904 or +3.0 V in the CS3903.

#### -VREF - Negative Voltage Reference output, PIN 2 (CS3904 Only)

Provides a negative output reference voltage with respect to the AGND pin. The magnitude is -1.5 V in the bipolar reference mode.

#### AGND - Analog Ground, PIN 6

Analog ground node for the voltage reference outputs. Connection should be made between this pin and the analog ground of the A/D converter.

**Reference Trim Pins****TRIM1 - Voltage Output Trim, PIN 14**

TRIM1 works in conjunction with TRIM2 to allow adjustment of the +VREF output voltage.

**TRIM2 - Voltage Output Trim, PIN 12**

See definition for TRIM1.

**TRIM3 - Voltage Output Trim, PIN 1 (CS3904 Only)**

TRIM3 works in conjunction with TRIM4 to allow adjustment of the -VREF output voltage.

**TRIM4 - Voltage Output Trim, PIN 3 (CS3904 Only)**

See definition for TRIM3.

**Miscellaneous****NC - No Connection, PINS 5, 8, 9, 10**

Should be left unconnected.

**GENERAL INFORMATION****1****DIGITAL AUDIO:****DIGITAL AUDIO PRODUCTS****2**

Digital Volume Control

Multimedia Codecs

Digital-to-Analog Converters

Analog-to-Digital Converters

AES/EBU &amp; S/PDIF Interfaces

**DATA ACQUISITION:****ANALOG-TO-DIGITAL CONVERTERS****3**

General Purpose &amp; Military

Seismic

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Transducer Interface

**SUPPORT FUNCTIONS:****SUPPORT FUNCTION PRODUCTS****4**

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Track &amp; Hold Amplifiers

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**COMMUNICATIONS:****COMMUNICATIONS PRODUCTS****5**

T1/CEPT Line Interfaces &amp; Framers

Jitter Attenuators

T3 Receiver

Local Area Network I.C.s

DTMF Receivers

**MISCELLANEOUS:****APPLICATION NOTES & PAPERS****6****APPENDICES****7**

Radiation Information

Reliability Calculation Methods

Package Mechanical Drawings

**SALES OFFICES****8**



### Low Power T1, PCM-30 and ISDN Primary Rate Line Interface Circuits

Crystal Semiconductor offers a broad family of low power CMOS PCM line interface circuits, with each device optimized for a unique system application. The CS6152, CS61535A, CS61574A and CS61575 are recommended for use in new designs. Since introducing the industry's first T1 and PCM-30 line interface circuits (the CS61534 and CS61544), we have shipped more CMOS PCM line interface ICs than any other vendor worldwide. Crystal Semiconductor's leadership continues with the best in pulse shapes, jitter attenuation, jitter tolerance and low power consumption.

Product	CS6152	CS61535A	CS61574A	CS61575
Rate	T1	T1/PCM-30	T1/PCM-30	T1/PCM-30
Receiver Functions	Data Slicer	Clock/Data Recovery	Clock/Data Recovery & Jitter Atten.	Clock/ Data Recovery & Jitter Atten.
Transmitter Functions	Driver	Jitter Atten. & Driver	Driver	Driver
Serial Control Port	-	✓	✓	✓
DIP Package	24-pin, .3"	28-pin, .6"	28-pin, .6"	28-pin, .6"
Surface Mount	28-pin PLCC	28-pin PLCC	28-pin PLCC	28-pin PLCC
AMI/B8ZS/HDB3 Coder	-	✓	✓	✓
Jitter Tolerance of Receiver	> 300 UI	> 300 UI	28 UI	138 UI

Line Interface Comparison Table

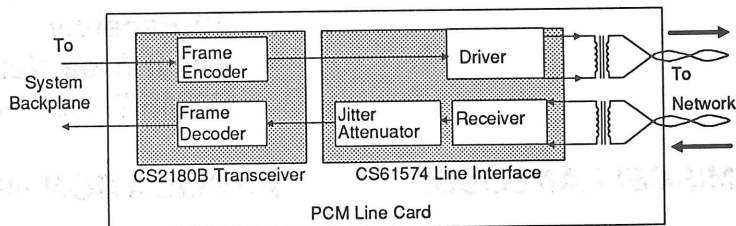
**CS6152:** Basic DSX-1 driver and receive buffer. For low power cards using digital-ASIC clock recovery. Ideal for trunk card bays where T1 density is limited by heat dissipation.

**CS61535:** Enhanced transmit-side jitter attenuator supports SONET VT1.5 and VT2, and other high speed transmission systems such as digital microwave radio and M13 multiplexers.

**CS61574A and CS61575:** Receive-side jitter attenuation supports loop-timing in customer-premises equipment and in channel banks. In the presence of large amplitudes of received jitter, the CS61575 provides more jitter attenuation than any device in the industry, and is ideal for AT&T 62411 applications.

### T1 Transceiver

Our CS2180B T1 Transceiver is a perfect companion to our T1 line interface ICs. This device handles encoding and decoding of all T1 frame formats (D4, SLC-96 and T1DM and ESF). Serial interface and control registers make it simple to configure from a microprocessor, including per channel control options. Packages available include 40-pin DIP or 44-lead PLCC.



The CS2180B is ideal for use with Crystal's family of line interface IC's

### Quartz Crystals

To complement our family of T1 Line Interface circuits, Crystal Semiconductor supplies pullable quartz crystals. The CXT6176 (for

T1 applications at 1.544 Mbps) and CXT8192 (for PCM-30 applications at 2.048 Mbps) are designed for 100% compatibility with our PCM line interface and jitter attenuator circuits.

### DTMF Receivers

Crystal has improved on industry standard DTMF receiver ICs while maintaining 100% pin compatibility. Our device features on-chip filters which offer the best possible signal-to-noise ratio allowing highly accurate decoding of telephone tones. Our CS20X family requires half the power of industry alternatives while providing 22 dB more dial tone rejection and better latch-up immunity.

### Jitter Attenuation Circuits

Our jitter attenuation technology is available stand-alone for a wide variety of applications. The CS61600 is ideal for T1 and PCM-30 applications while the CS80600 attenuates jitter in T2, 2nd-level CEPT lines and Token Ring LANs. Both attenuators can be used with external divide circuits to handle low frequencies.

### T3/E3/SONET Analog Receivers

Crystal's CS6300 and CS6301 are high-performance analog receivers for T3(44 MHz), E3 (34 MHz) and SONET STS-1/OC-1 (51 MHz) applications. The devices provide line equalization, plus clock and data recovery. For optical applications, the line equalizer can be bypassed, allowing the output of an optical receiver to be input to the clock recovery section. The Phase Lock Loop used for clock recovery has continuous frequency calibration and matches the frequency of an external reference clock upon loss of signal.

### Ethernet

Crystal offers a complete Ethernet/Cheapernet hardware solution. The CS8005 is a sophisticated Advanced Ethernet Data Link Controller, which connects to the CS8023A Manchester Code Converter. Connection to the co-ax cable is achieved by the CS83C92C transceiver.

The CS8005 is a high-performance 16-bit Ethernet controller. The CS8005 uses a large dedicated local buffer memory, which off-loads the host CPU and CPU backplane. This local memory, along with a comprehensive command set, allows Ethernet capability to be added with minimal host CPU impact.

The CS8023A Manchester Code Converter is implemented in low-power CMOS, and requires only a single 5 V supply. The CS8023A is implemented in a high-voltage process allowing it to tolerate the required 16 V fault conditions.

Crystal is the first company to bring the benefits of low-power CMOS technology to Ethernet/Cheapernet transceivers. The CS83C92C uses up to 40% less power than the DP8392A and DP8392B. This translates into increased reliability and compatibility with surface mount technology. The CS83C92C is the first Ethernet transceiver which is fully compliant with ISO/IEEE 802.3.

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CS61535A T1 (1.544 MHz) & PCM-30 (2.048 MHz ) Line Interface	5-9
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CS80600 4.5 MHz to 8.5 MHz Jitter Attenuator	5-16
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CS8870 DTMF Receiver	5-18

See the Crystal Telecommunications Data Book  
for the complete data sheets on the above products

## DTMF Receiver

### Features

- Full Receiver Implementation
- Central Office Quality
- Detects 12 or 16 DTMF Tone Pairs
- Uses Inexpensive 3.579 MHz Colorburst Crystal
- Hex or Binary 2-of-8 Output
- Synchronous or Handshake Controlled Output
- Built-in Filter for Dial Tone Rejection
- 18 Pin Package
- Single 5 Volt  $\pm 10\%$  Power Supply
- Early Detect Output
- Pin Compatible with SSI 202/SSI 203

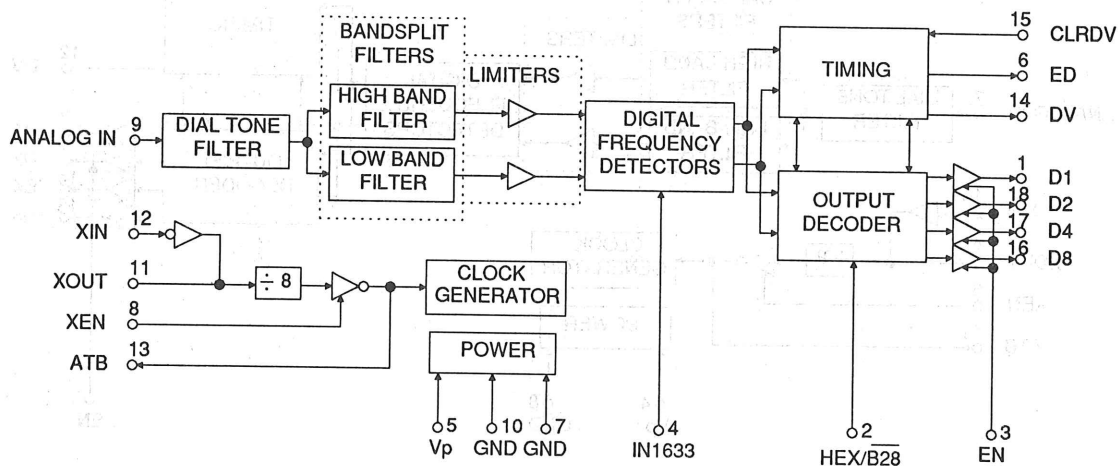
### General Description

The CS202 and CS203 are fully integrated DTMF (Dual Tone Multifrequency) receivers that decode the tone pairs used in standard dialing schemes. All of the functions needed for decoding the tone pairs are implemented using Crystal's double-poly CMOS process for low power and high performance.

### ORDERING INFORMATION

CS202-P - 18 Pin Plastic DIP  
CS203-P - 18 Pin Plastic DIP  
All standard 300 mil DIPs

### Block Diagram



## DTMF Receiver

### Features

- Full Receiver Implementation
- Central Office Quality
- Detects All 16 DTMF Tone Pairs
- Uses Inexpensive 3.579 MHz Colorburst Crystal
- Hex Output
- Built-in Filter for Dial Tone Rejection
- 14 Pin Package
- Single 5 Volt  $\pm 10\%$  Power Supply
- Low Power CMOS Technology
- Pin Compatible with SSI 204

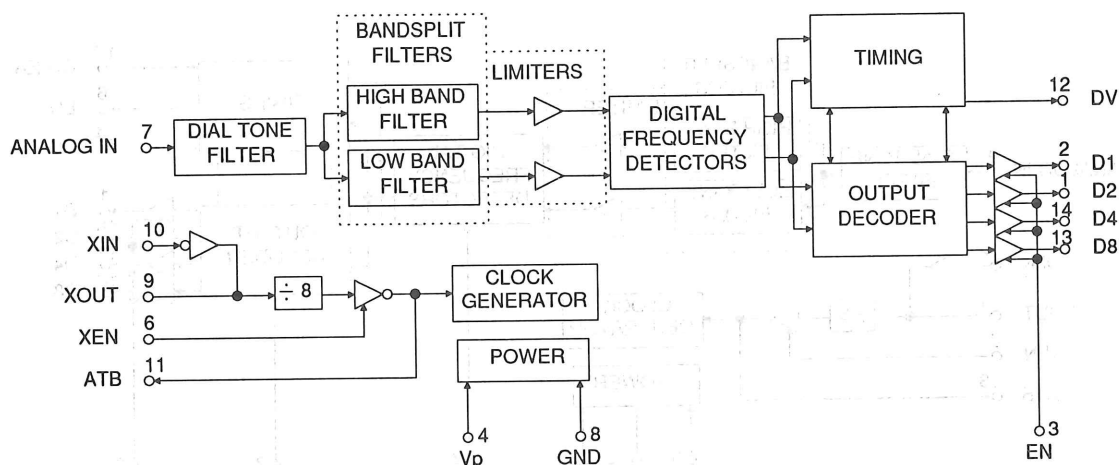
### General Description

The CS204 is a fully integrated DTMF (Dual Tone Multifrequency) receiver that decodes the tone pairs used in standard tone dialing schemes. All of the functions needed for decoding the tone pairs are implemented using Crystal's double-poly CMOS process for low power and high performance.

### ORDERING INFORMATION

CS204-P - 14 Pin Plastic DIP  
Standard 300 mil DIPs

### Block Diagram



## T1 Transceivers

### Features

- Monolithic T1 Framing Device
- Both Transceivers support D4 and ESF framing formats
- CS2180B also supports SLC-96 and T1DM framing formats
- CS2180B has updated AIS and Carrier Loss detection criteria
- CS2180B is Plug Compatible with CS2180A, DS2180A and DS2180

### General Description

The CS2180A and CS2180B are monolithic CMOS devices which encode and decode T1 framing formats. The devices support bit-seven and B8ZS zero suppression, and bit-robbled signaling. Clear channel mode can be selected on a per channel basis.

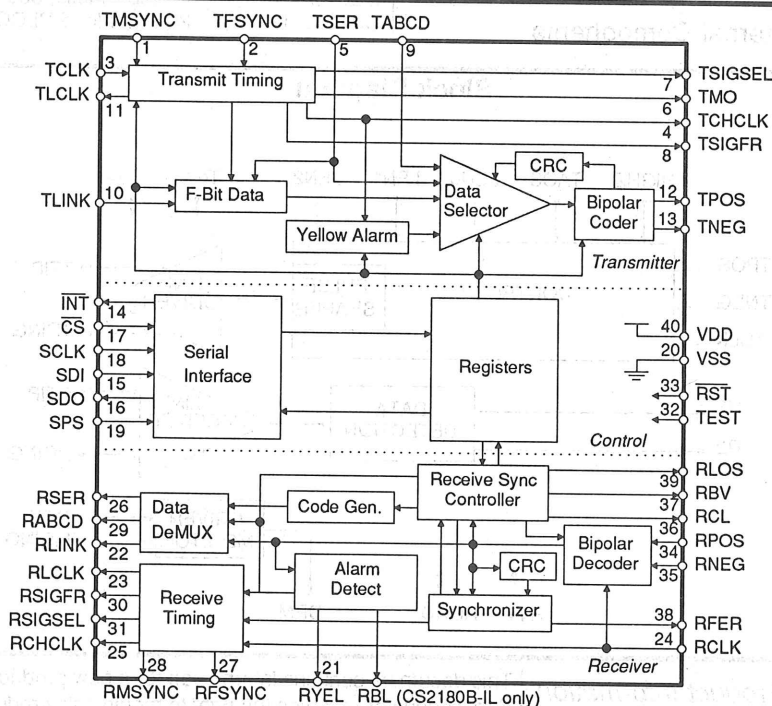
The serial interface has been enhanced to allow the CS2180A and CS2180B to share a chip select signal and register address space with the CS61534/35/74 PCM Line Interface device.

### Applications

- T1 Line Cards
- ISDN Primary Rate Line Cards

### Ordering Information:

CS2180B-IP	40 Pin Plastic DIP	-40 to 85 °C
CS2180B-IL	44 Pin PLCC	-40 to 85 °C
CS2180A-IP	40 Pin Plastic DIP	-40 to 85 °C
CS2180A-IL	44 Pin PLCC	-40 to 85 °C



## Low Power T1 Analog Interface

### Features

- Provides Analog T1 Line Interface
- Low Power Consumption  
(normally 180 mW)
- EXPERT *Pulse*™ Programmable  
Pulse-Shaping Line Driver
- Provides Receiver AMI-to-TTL Buffer  
Which Compliments Digital Gate Array  
Clock-Recovery Circuits
- Driver Performance Monitor
- Minimal External Components

### General Description

The CS6152 combines the analog transmit and receive line interface functions for T1 system interface in one device. The T1 analog interface operates from a 5 Volt supply, and is transparent to the T1 framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet. The device provides the ideal front-end to digital gate array based clock recovery circuits.

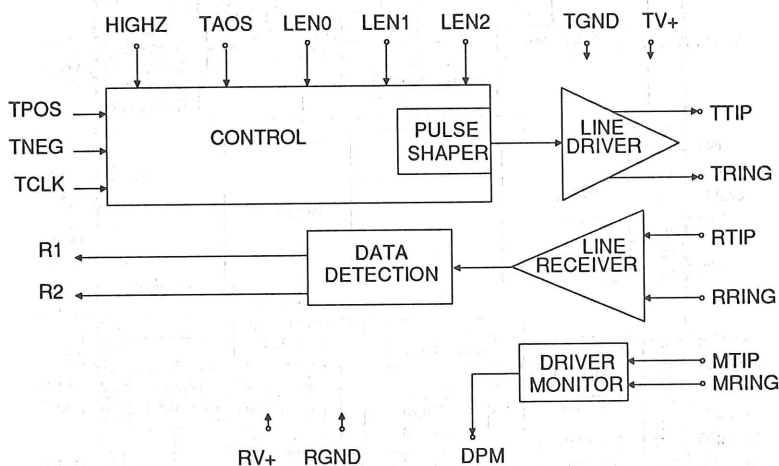
### Applications

- Interfacing Network Equipment such as Multiplexors, Channel Banks and Switching Systems to a DSX-1 Cross Connect.
- Interfacing Customer Premises Equipment such as PABX's, T1 Multiplexors, Data PBX's and LAN Gateways to a Channel Service Unit or T1 modem.

### ORDERING INFORMATION

CS6152A-IP - 24 Pin Plastic, 300 mil DIP  
CS6152-IL - 28 Pin J-lead PLCC

### Block Diagram



### Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.



## PCM Line Interface

### Features

- Provides Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Transmit Side Jitter Attenuation Starting at 6 Hz, with > 300 UI of Jitter Tolerance
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoders/Decoders
- 14 dB of Transmitter Return Loss
- Compatible with SONET, M13, CCITT G.742, and Other Asynchronous Muxes

### General Description

The CS61535 and CS61535A combine the analog transmit and receive line interface functions for a T1/PCM-30 interface in a single 28-pin device. The line interface unit (LIU) operates from a single 5 Volt supply and is transparent to the framing format. Crystal's EX-PERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for CCITT G.703, or for connecting to DSX-1 cross-connects for line lengths ranging from 0 to 655 feet. The transmitter uses a 32-bit elastic store to remove jitter from the transmit data.

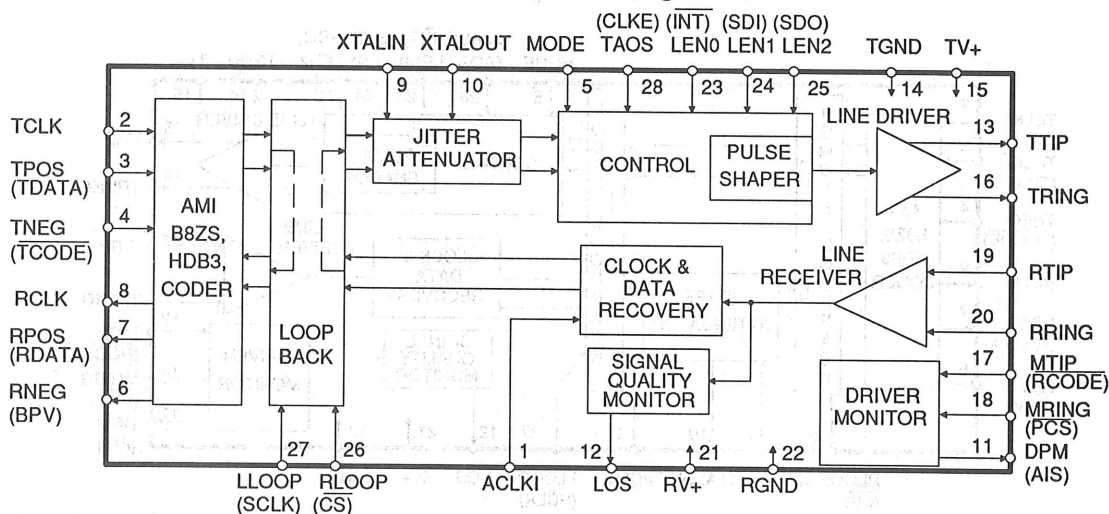
### Applications

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-1 cross connect.
- Interfacing customer premises equipment to a CSU.
- Interfacing to PCM-30 links.

### Ordering Information

CS61535A-IP1	28 Pin Plastic DIP	T1 & PCM-30
CS61535A-IL1	28 Pin PLCC (j-leads)	T1 & PCM-30
CS61535-IP1	28 Pin Plastic DIP	T1 & PCM-30
CS61535-IL1	28 Pin PLCC (j-leads)	T1 & PCM-30

### CS61535A Block Diagram



### Preliminary Product Information

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JUN '90  
DS40PP2.1  
5-9

## PCM Line Interface

### Features

- Provides Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, Jitter Attenuation & Clock Recovery Functions
- Fully Compliant with AT&T 62411 (1990 Version) Jitter/Synchronizer (Stratum 4, Type II) Requirements
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoders/Decoders
- 14 dB of Transmitter Return Loss

### General Description

The CS61575, CS61574A and CS61574 combine the analog transmit and receive line interface functions for a T1/PCM-30 interface in a single 28-pin device.

The line interface unit (LIU) operates from a single 5 Volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for CCITT G.703, or for connecting to DSX-1 cross-connects for line lengths ranging from 0 to 655 feet. The CS61575 receiver uses a 128-bit elastic store to remove jitter from the incoming data. The CS61574A and CS61574 employ a 32-bit elastic store.

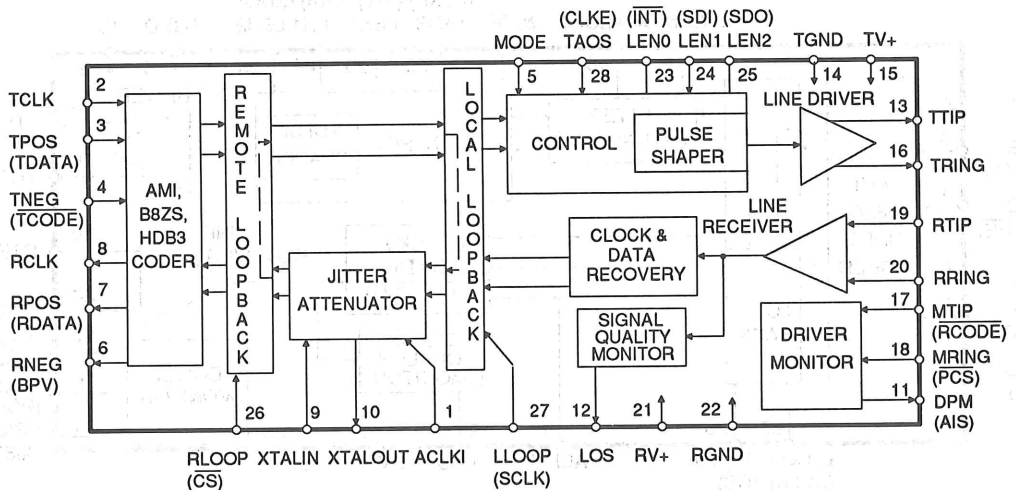
### Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

### ORDERING INFORMATION

Contact Crystal Semiconductor

### Block Diagram



### Preliminary Product Information

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JUN'90  
DS20PP5  
5-10

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## PCM Jitter Attenuator

### Features

- Unique Clock-Tracking Circuitry Filters 50 Hz or Higher Frequency Jitter for T1 and PCM-30 Applications
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

### General Description

The CS61600 from Crystal Semiconductor accepts T1 (1.544 Mb/s) or CCITT standard (2.048 Mb/s) data and clock inputs, and tolerates at least 7 (and up to 14) unit intervals, peak-to-peak, of jitter. Before outputting data and clock, jitter is attenuated using an internal clock-tracking variable oscillator and a 16 bit FIFO elastic store.

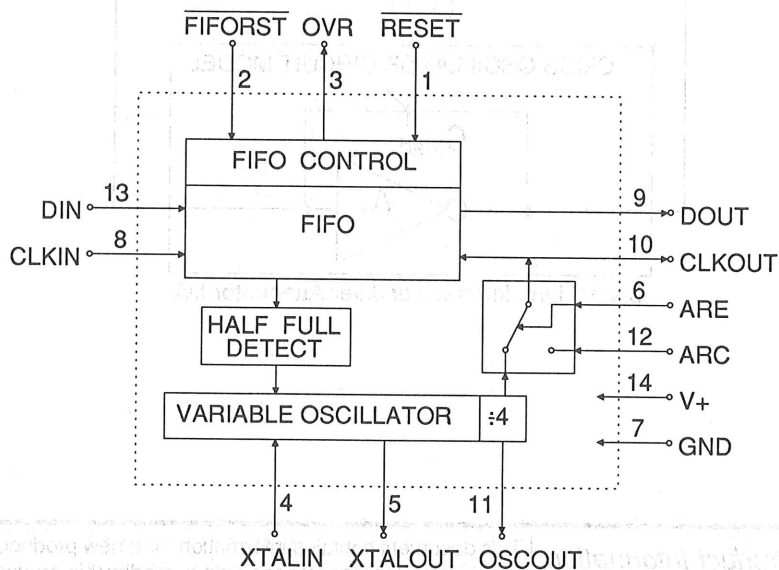
The jitter attenuation function can be determined by appropriate specification of the external crystal.

The CS61600 is transparent to data format, and is intended for application in carrier systems, switching systems, Local Area Network gateways and multiplexers.

### ORDERING INFORMATION

CS61600-ID1 - 14 Pin Cerdip; T1 and 2.048 MHz  
CS61600-IP1 - 14 Pin Plastic DIP; T1 and 2.048 MHz

### Block Diagram



## Pullable Quartz Crystals

### Features

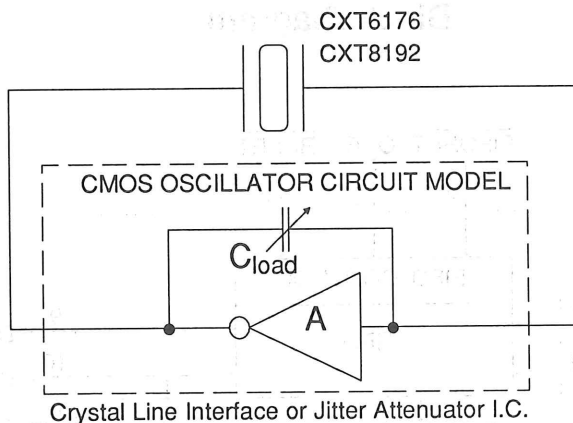
- Complements CS61534, CS61535, CS61535A, CS61544, CS61574, CS61574A, and CS61575 PCM Line Interface integrated circuits and CS61600 PCM Jitter Attenuator.

### Description

Crystal Semiconductor's line interface and jitter attenuator IC's require unique performance specifications for the crystals. The CXT6176 and CXT8192 are built to meet Crystal's specifications for T1 and PCM-30 applications respectively.

### Ordering Information

CXT6176	Crystal for T1 Applications
CXT8192	Crystal for PCM-30 Applications



### Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

## E3/T3/STS-1 Analog Line Receiver

### Features

- CS6300 Provides Complete Analog Line Receiver for T3 and STS-1 Applications
- CS6301 Provides Complete Analog Line Receiver for E3 G.703/G.823 Applications
- Provides Line Equalization, and Clock and Data Recovery Functions
- Line equalizer can be bypassed for OC-1 optical applications
- Includes local loopback multiplexor

### General Description

The CS6300 provides the analog receive line interface functions for a 44.736 MHz T3 or 51.84 MHz STS-1 interface, and an OC-1 optical interface. The CS6301 supports 34.386 MHz E3 operation. The devices operate from a single +5 Volt supply and are transparent to the framing format. The CS6300 is pin-compatible with the T7295.

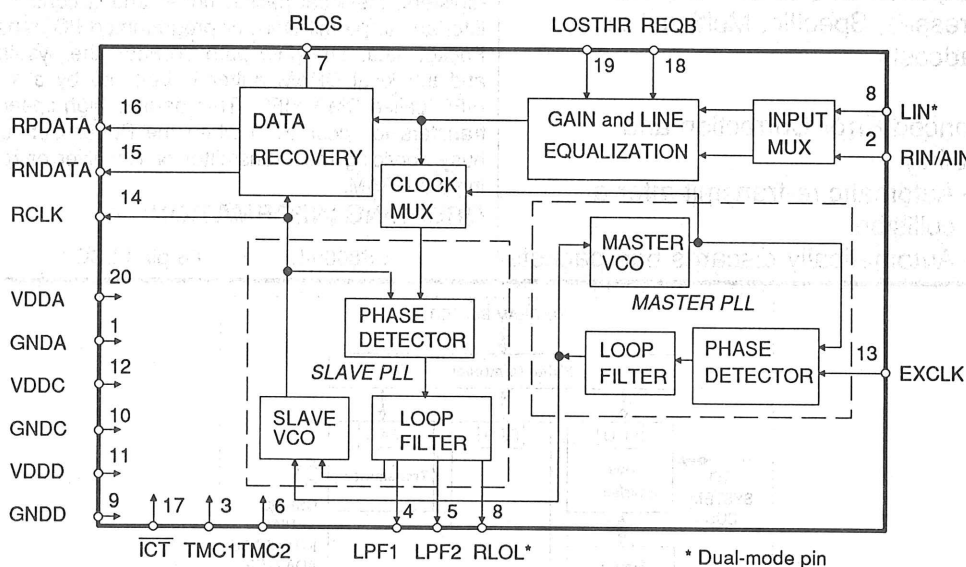
### Applications

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-3 cross connect.
- Interfacing customer premises equipment to a line.

### Ordering Information

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### Block Diagram



5

### Preliminary Product Information

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APR '92  
DS56PP3  
5-13

## Advanced Ethernet Data Link Controller

### Features

- High Throughput
  - Supports Full 10M BPS Data Rate
  - Back-to-Back Packets
- 64 K-Byte Local Packet Buffer
  - Provides refresh for DRAMs
  - Off-loads host bus
- Conforms to ISO/IEEE 802.3 Standard
- Flexible Bus Interface
  - Intel and Motorola bus modes
  - I/O, string move, DMA access
  - Memory or I/O mapped
  - 8 or 16 bit bus width
- Recognizes One to Six Receive Addresses, Specific, Multicast or Broadcast
- Advanced Error Correction and Handling
  - Automatic re-transmit after a collision
  - Automatically discards bad packets

### General Description

The CS8005 has five major blocks: the Transmitter, Receiver, Buffer Controller, Bus Interface and Status and Command Register.

The CS8005 supports the link layer (layer 2) of the IEEE 802.3 standard. It performs serialization/deserialization, preamble generation/stripping, CRC generation/stripping, transmission deferral, collision handling and address recognition of up to 6 station addresses including multicast/broadcast addresses.

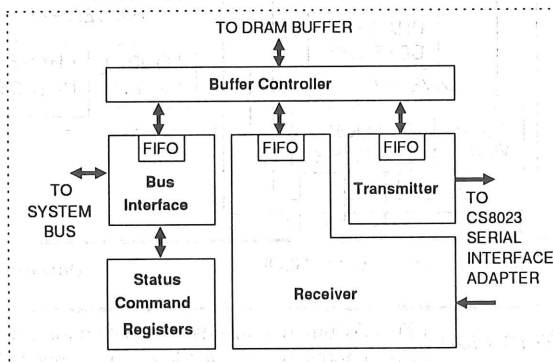
The Buffer Controller manages a 64K byte local packet buffer. This block provides arbitration and control for four memory ports: the transmitter, the receiver, the bus interface and an internal DRAM refresh generator. Received packets are temporarily stored until the system either reads or disposes of them, and packets placed there by the system are held for transmission over the link.

The Bus Interface interfaces to the system bus and provides access to internal configuration and status registers, the local packet buffer and a control signal interface to permit DMA or programmed I/O transfer of Packet data. The data path between the system bus and the local DRAM buffer is buffered by a 16 byte FIFO called DMA FIFO. This permits high speed data transfers to occur even when the Buffer Controller is busy servicing the Transmitter or Receiver or refreshing the DRAM.

### ORDERING INFORMATION:

CS8005-L

68-pin PLCC



## Manchester Code Converter

### Features

- Compliant with ISO/IEEE 802.3 and Ethernet Rev. 1
- Works with the CS8005 and Intel 82586 LAN Controllers.
- Manchester Data Encoding/Decoding and Receiver Clock Recovery
- Loopback Capability for Diagnostics and Isolation
- Fail-Safe Watchdog Timer Circuit to Prevent Continuous Transmission.
- Transceiver Interface High Voltage (16V) Short Circuit Protection
- Low Power CMOS Technology with Single 5V Supply.

### General Description

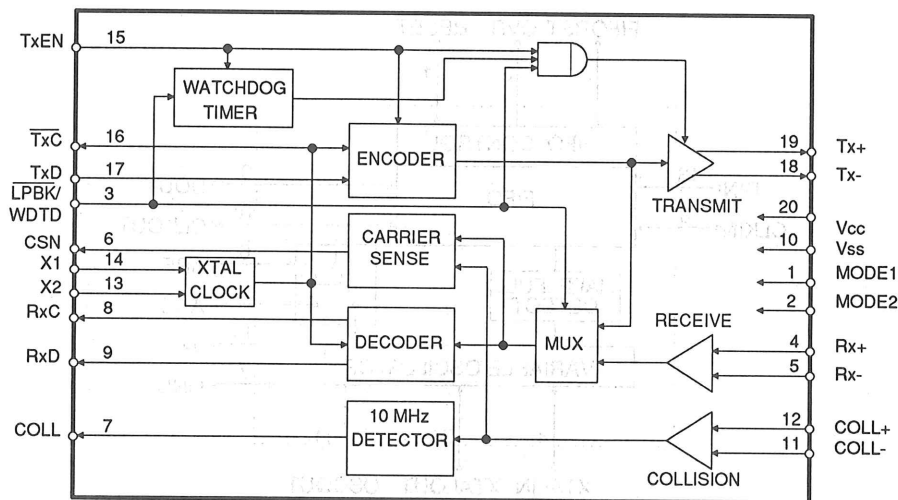
The CS8023A Manchester Code Converter provides the Manchester data encoding and decoding functions of the Ethernet Local Area Network physical layer. It interfaces to the CS8005 CSMA/CD Data Link Controller or to the Intel 82586 LAN Controller and any standard Ethernet transceiver as defined by IEEE 802.3 and Ethernet Revision 1.

The CS8023A is a functionally complete Encoder/Decoder including ECL level balanced driver and receivers, on board oscillator, analog phase locked loop for clock recovery and collision detection circuitry. In addition, the CS8023A includes a 25 millisecond watchdog timer, a 4.5 microsecond window generator, and a loopback mode for diagnostic operation.

Together with the CS8005 and CS83C92C, the CS8023A provides a high performance minimum cost interface for any system to Ethernet.

### ORDERING INFORMATION:

CS8023A-P	Plastic DIP
CS8023A-L	20-Pin PLCC



### Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation  
P.O. Box 17847, Austin, TX 78760  
(512) 445 7222 Fax: (512) 445 7581

MAY '90  
DS65PP1  
5-15



## High Speed Jitter Attenuator

### Features

- Accepts Input Clock with Frequency of 4.5 MHz to 8.5 MHz
- Unique Clock-Tracking Circuitry
- Tolerates and Attenuates At Least 3 Unit Intervals of Jitter
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

### General Description

The CS80600 from Crystal Semiconductor accepts 4.5 to 8.5 MHz clock and data inputs and removes up to  $\pm 3$  data bits of jitter before outputting the data and clock. Jitter is removed using an internal clock tracking circuit and an 8-bit FIFO elastic store.

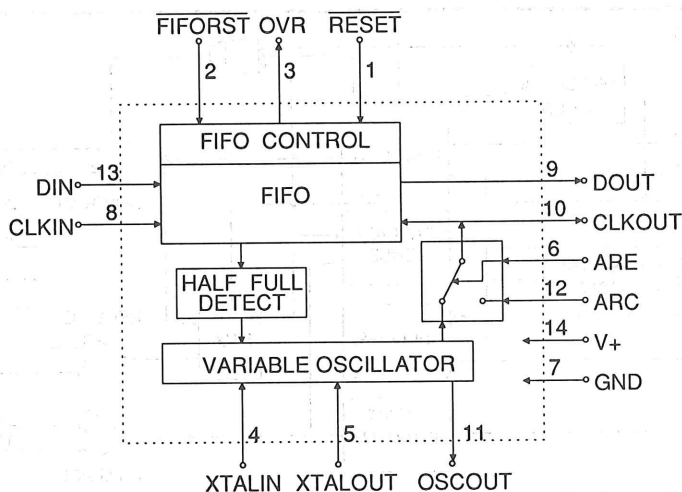
### Applications

- **Token Ring:** The CS80600 can be used to eliminate the accumulation of data-pattern dependent jitter which is the primary factor limiting the size of token rings. The CS80600 is intended for application in station adaptor cards, in active wiring concentrators, and in repeaters.
- **PCM:** TIC, T2, and CEPT2 and second order multiplexors.

### ORDERING INFORMATION

CS80600-P - 14 Pin Plastic DIP

### Block Diagram



## Coaxial Transceiver Interface (Rev D)

### Features

- Implemented in High Voltage, Low Power CMOS
- Compatible with National's DP8392A
- CS83C92C is Compliant With ISO/IEEE 802.3 10Base5 (Ethernet) and 10Base2 (Cheapernet)
- All Transceiver Functions Integrated Except Signal and Power Isolation
- Squelch Circuitry Rejects Noise
- CD Heartbeat Externally Selectable Allowing Operation with IEEE 802.3 Compatible Repeaters
- Receive & Transmit Mode Collision Detection
- Standard 16-pin DIP Package & 28 pin PLCC

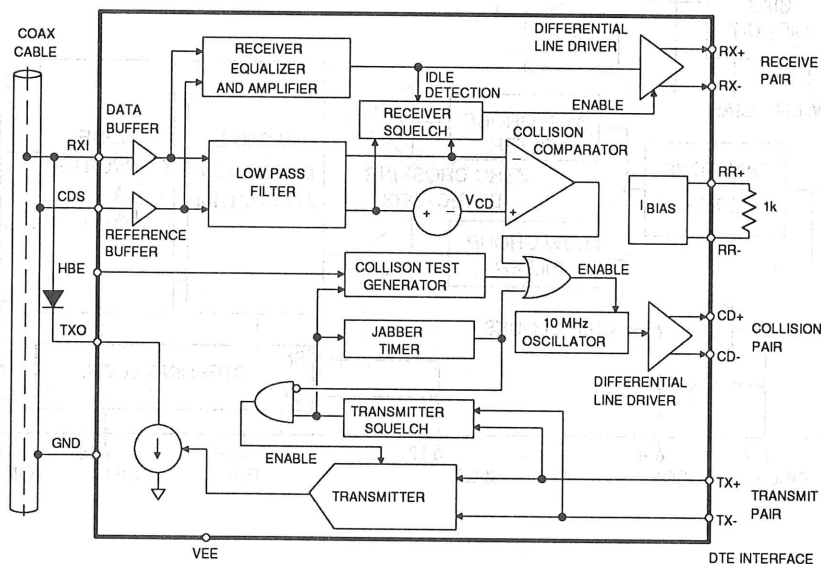
### General Description

The CS83C92 Ethernet Transceiver interfaces an Ethernet or Cheapernet Local Area Network (LAN) to a LAN Adapter board, and may be located up to 50 meters from the station equipment. The Transceiver operates with the Crystal LAN components CS8005 Ethernet Data Link Controller and the CS8023A Manchester Code Converter. The CS83C92A is fully compatible with the DP8392A but the CS83C92A is built in CMOS technology (hence the 83"C"92). The CS83C92C is a higher performance grade which is compliant with IEEE 802.3 specifications.

For Ethernet applications, the CS83C92 is mounted on the COAX cable, and connects to the station equipment via an AUI cable. In a Cheapernet network, the CS83C92 is usually mounted on the LAN adapter card in the station equipment where it connects to the thin COAX through a BNC connector.

### ORDERING INFORMATION:

CS83C92A-CP/D PDIP	CS83C92C-CP/D PDIP
CS83C92A-CL/D PLCC	CS83C92C-CL/D PLCC



## DTMF Receiver

### Features

- Full Receiver Implementation
- Central Office Quality
- Adjustable Receive Sensitivity
- Adjustable Detection and Release Time
- Single Supply Operation
- Low Power Consumption
- 18 Pin Package
- Pin Compatible with MT8870B

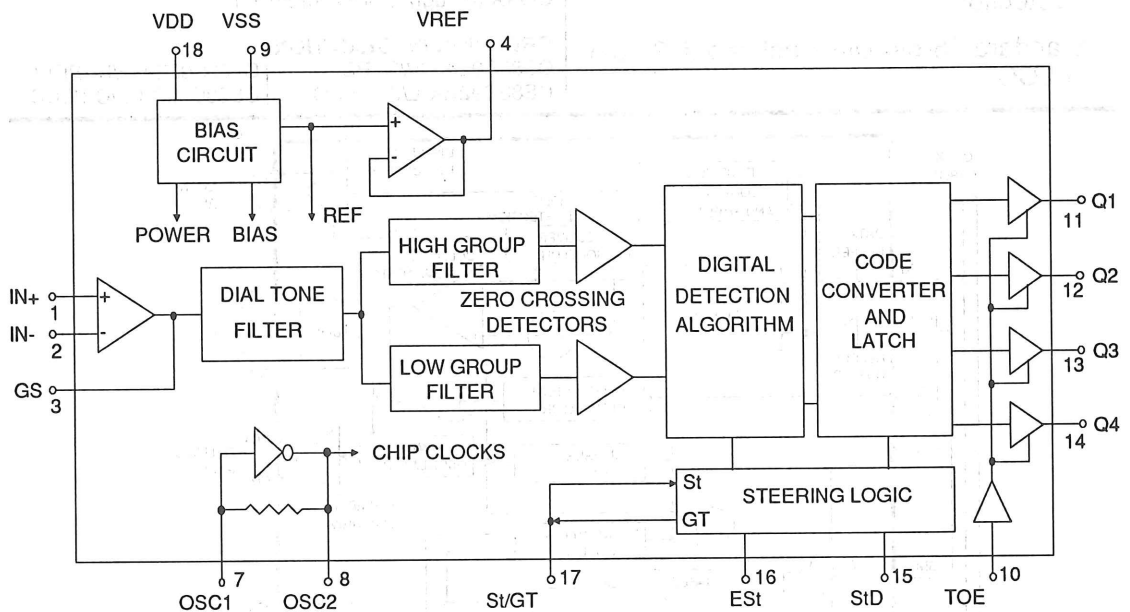
### General Description

The CS8870 is a fully integrated DTMF (Dual Tone Multifrequency) receiver for decoding tone pairs generated by a tone dialing telephone. The decoded signal is output as a four bit binary code. All of the functions needed to decode the 16 DTMF tone pairs are integrated in the CS8870 using Crystal's CMOS double-poly process, taking advantage of the low power and high performance offered by this technology.

### ORDERING INFORMATION

CS8870-IP - 18 Pin Plastic DIP

### Block Diagram



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Multimedia Codecs  
Digital-to-Analog Converters  
Analog-to-Digital Converters  
AES/EBU & S/PDIF Interfaces

**DATA ACQUISITION:****ANALOG-TO-DIGITAL CONVERTERS****3**

General Purpose & Military  
Seismic  
DC Measurement  
Transducer Interface

**SUPPORT FUNCTIONS:****SUPPORT FUNCTION PRODUCTS****4**

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Track & Hold Amplifiers  
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Local Area Network I.C.s  
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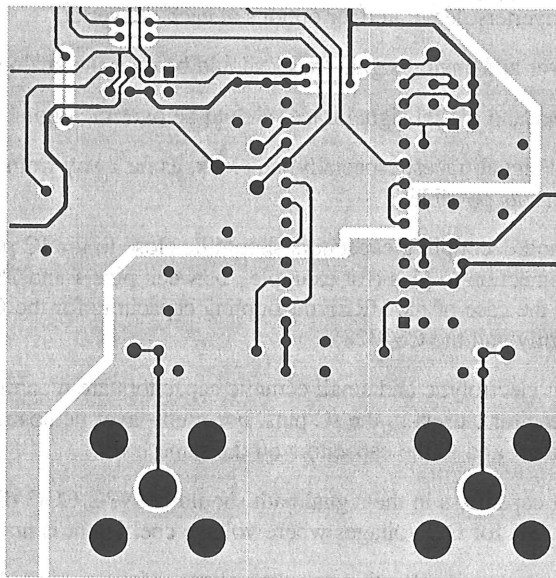
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## **Application Note**

### **Layout and Design Rules for Data Converters**

by  
**Ron Knapp & Steven Harris**



Here is a list of guidelines for optimum printed circuit board layout for Crystal ADC's and DAC's. Use these pages as a checklist during and after layout by checking the boxes when each line item is OK. Remember, Crystal offers a free schematic and layout review service. Try hard to use this service before building your first prototype board. Comments or additional items are very welcome.

- ☐ 1) Partition the board with all analog components grouped together in one area and all digital components in the other. Common power supply related components should be centrally located.
- ☐ 2) Have separate analog and digital ground planes on the same layer, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes should be  $>1/8"$ .
- ☐ 3) Mixed signal components, including the data converters, should bridge the partition in the ground plane with only analog pins in the analog area, and only digital pins in the digital area. Rotating the data converter can often make this task easier.
- ☐ 4) Analog and digital ground planes should only be connected at one point (in most cases). Have vias available in the board to allow alternative connection points.
- ☐ 5) The analog to digital ground plane connection should be near to the power supply, or near to the power supply connections to the board, or near to the data converter. In the case of multiple converters, leave jumper options at each converter.
- ☐ 6) Analog power and analog signal traces should be over the analog ground plane.
- ☐ 7) Digital power and digital signal traces should be over the digital ground plane.
- ☐ 8) Keep digital signal traces, especially the clock, as far away from analog input and voltage reference pins as possible.
- ☐ 9) Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connection to pins (for example, between pins 1 and 28 at the top end of the IC package in the case of the VREF decoupling capacitors for the CS5326 family, the CS5336 family and the CS4328).
- ☐ 10) If both large electrolytic and small ceramic capacitors are recommended, make the small ceramic capacitor closest to the IC pins. For multi-layer pc boards, make the connections to the converter and to the capacitors on the same layer.
- ☐ 11) All filtering capacitors in the signal path should be NPO/COG dielectric. BX/X7R dielectric is OK for DC voltages where voltage coefficient is not a factor.
- ☐ 12) All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors are OK for DC voltages and the power supply path where voltage coefficient, temperature coefficient or noise are not a factor. Avoid wire wound resistors and potentiometers.



- ☐ 13) Avoid multiple crystal oscillators or asynchronous clocks. Best results are obtained when all circuits are synchronous to the A/D or D/A sampling clock.
- ☐ 14) When using converters with DSP IC's, operate everything from one crystal using ☐ dividers if necessary.
- ☐ 15) In systems requiring multiple crystals for selectable sampling frequencies, enable only one at a time. Shut off all other oscillators by removing power. Make sure other oscillators are off either with an active crowbar on Vcc or very high impedance switch. Often the leakage from a transistor or FET which is not completely off is sufficient for the oscillator to produce a low level output frequency.
- ☐ 16) When using DC-DC switching regulators, synchronize the switching frequency to the A/D if possible. This applies to CMOS chopper amplifiers as well.
- ☐ 17) Avoid connecting the clock source oscillator to the converter sampling clock input through analog multiplexers, PAL's, gate arrays, opto-couplers or circuits which can cause jitter.
- ☐ 18) Locate the crystal or oscillator close to the converter. Avoid overshoot and undershoot on the master clock for the converter. This is particularly important for the CS5326 family, where the master clock (CLKIN) goes directly into the analog modulator die.
- ☐ 19) Use buffers for digital signals directly to or from the converter to connectors which go off the board.
- ☐ 20) In the case of piggy-back boards, or boards which plug into a slot adjacent to other boards, consider the circuits which will be above or below the converter as sources of interference. A mu-metal screen may be required.
- ☐ 21) For delta sigma converters, make sure that potential interfering clocks are not in sensitive frequency regions. Sensitive regions are defined as  $\pm$  passband either side of multiples of the input sample rate. Two examples are : a) for a CS5336 operating at 48 kHz word rate, the frequencies to avoid are  $(N \times 3.072\text{MHz}) \pm 24 \text{ kHz}$ . b) for a CS5501 with a 4 MHz crystal, the frequencies to avoid are  $(N \times 16 \text{ kHz}) \pm 10 \text{ Hz}$ . Frequencies which are synchronous to the input sample rate will not cause problems, since they will be converted to dc, and calibrated out.
- ☐ 22) For boards with more than 2 layers, do not overlap analog related and digital related planes. Do not have a plane which crosses the split between the analog ground plane region and the digital ground plane region.
- ☐ 23) For CS5326, CS5336 & CS5349 families, supply VD+ to the device via a separate trace connected to where the +5V digital supply enters the board. Connect no other logic to this trace. Alternatively, provide a 10  $\mu\text{H}$  inductor in series with VD+, near to the ADC.
- ☐ 24) For boards with both A/D converters and D/A converters, provide a means for testing each function separately. Possible methods include providing a header to allow access to the digital data paths, and allowing for easy attachment of a CS8402 and CS8412 AES/EBU transmitter and receiver parts.

- ☐ 25) Terminate unused op-amps in dual and quad packs by grounding the + input and connecting the - input to the output.
- ☐ 26) Digital control lines which must cross into the analog region should be as short as possible and should be mostly static. For example, digital gain and analog mux control lines.
- ☐ 27) Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. This has been shown to reduce digital to analog coupling by up to 30 dB.
- ☐ 28) The pins of DIP or SOIC packages should not have ground plane in between adjacent pins.
- ☐ 29) In systems using a delta-sigma converter, then avoid the use of clocks (particularly the serial bit clock) at half the frequency of the input sample rate. If this frequency interferes with the voltage reference, then tones can occur.

## Application Note

### ADC Input Buffer and Protection Techniques

by  
Steven Green

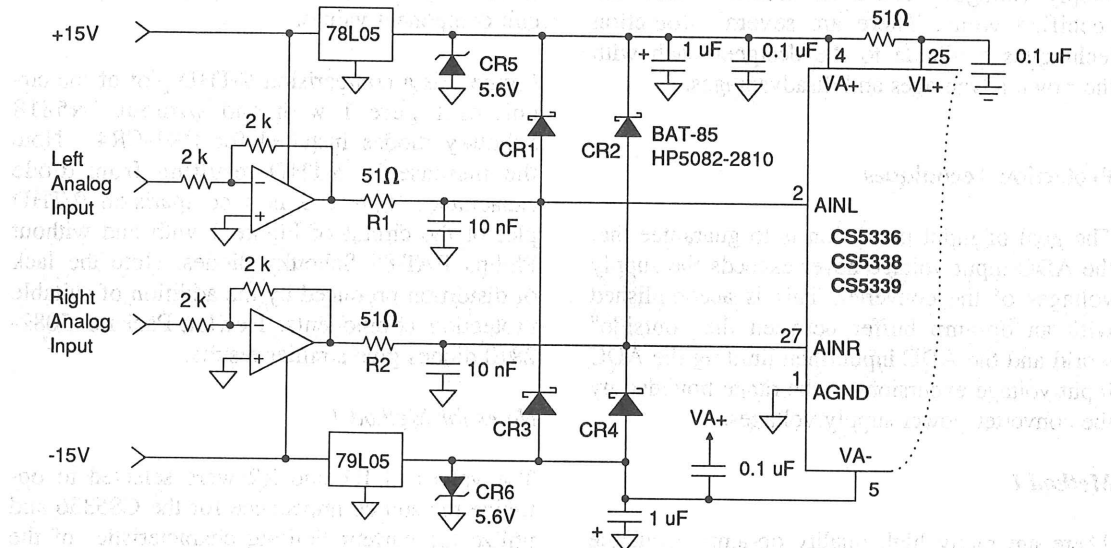


Figure 1. ADC Input Protection  $\pm 15V$  Op-Amp

#### Introduction

The design of input buffer and protection circuits for analog-to-digital-converters (ADC) is critical to an optimized and reliable data acquisition system. The Crystal Semiconductor application note "ADC Input Buffers" covered this area well and the system designer should review this information. Since the publication of "ADC Input Buffers" there have been many requests for additional information and circuits relating to ADC input protection. This application note describes suitable buffer/protection circuits for the CS5336 family of converters. The techniques described are equally applicable to the other families of Crystal analog-to-digital converters.

#### SCR Latch-up

SCR latch-up has been defined as "the creation of a low impedance path between the power supply rails by the triggering of parasitic, four-layer bipolar structures (SCR's) inherent in CMOS input and output circuitry." This is a self-sustaining condition and once latched, a CMOS device will remain so regardless of the I/O pin voltages until the power supply voltages are removed. The excessive power dissipation during latch-up may also damage the device. Latch-up is most often caused by forcing current into the inputs or outputs of a CMOS device by applying voltages greater than the power supply rails. When powered, Crystal

Semiconductor ADC's are extremely immune to latch-up because of the amount of current required to initiate a latch. Problems can arise when input voltages greater than the instantaneous power supply voltages are applied during power-up. A less common but equally damaging SCR condition can occur when power-supply voltages exceed the absolute maximum specified value. There are several protection techniques available to the designer each with their own advantages and disadvantages.

### Protection Techniques

The goal of input protection is to guarantee that the ADC input voltage never exceeds the supply voltages of the converter. This is accomplished with an op-amp buffer between the "outside" world and the ADC input, then limiting the ADC input voltage excursions to the range bounded by the converter power supply voltages.

#### Method I

There are many high quality op-amps available to the design engineer for use as input buffers and the majority of these have been designed to operate from power supplies greater than  $\pm 5V$ . The use of the required multiple supplies presents potential problems: It is possible for the ADC analog input to experience voltages greater than the ADC supplies either during signal amplitude excursions, transient power-on conditions or op-amp failure. Several methods are available to clamp the ADC input voltage and are discussed in detail in references 1-7. Figure 1 shows a diode-clamped input buffer circuit utilizing multiple supplies. The type of diode selected for CR1-CR4 is crucial and must be evaluated using the following criteria:

- 1) Forward-biased voltage characteristics. Schottky diodes are preferred due to their low forward-biased voltage characteristics.
- 2) Reverse-bias leakage current. The effects of

voltage dependent leakage currents are proportional to circuit impedances and can cause distortion. Leakage currents will also vary with temperature and must be evaluated over the intended temperature operating range.

- 3) Reverse-bias capacitance. Voltage dependent junction capacitance can cause distortion and must be insignificant in comparison to the circuit component values.

Figure 2 is a comparison %THD plot of the circuit of Figure 1 with and without 1N5818 Schottky diodes installed for CR1-CR4. Note the increase in %THD resulting from diode capacitance. Figure 3 is a comparison %THD plot of the circuit of Figure 1 with and without Philips BAT-85 Schottky diodes. Note the lack of distortion produced by the addition of suitable protection components. Hewlett-Packard 5082-2810 diodes give similar results.

#### Notes for Method I

The values of R1 and R2 were selected to optimize the source impedance for the CS5336 and utilize the current limiting characteristics of the op-amp.

Clamping circuits with diodes in the feedback loop of the op-amp work well for signal clamping but are not effective for power-on transient or op-amp failure conditions. These circuits are not recommended for protection.

#### ADC Power Supply Overvoltage

Standard 3-terminal regulators are designed to either source (78L05) or sink (79L05) current but not both. It is possible to raise the ADC supply voltage above the regulation voltage through the Schottky diodes during error conditions. The 5.6V zener diodes CR5 and CR6 are included to prevent the supply voltages from exceeding the maximum specified value and damaging the converter.

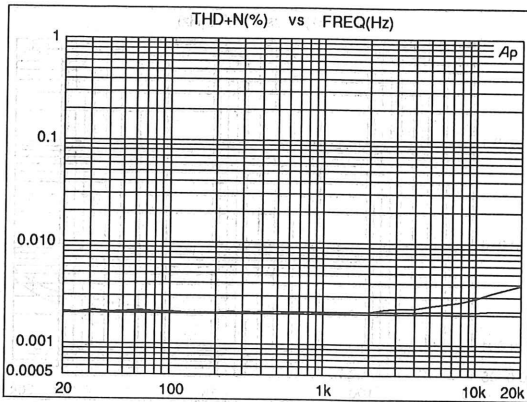


Figure 2. %THD Effects of 1N5818 Schottky Diodes with NE5532 Op-amp

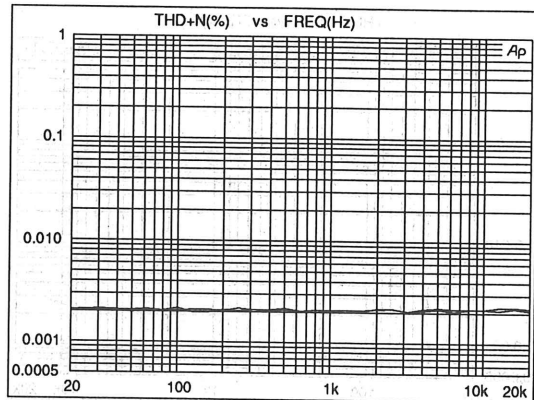


Figure 3. %THD Effects of BAT-85 Schottky Diodes with NE5532 Op-amp

### Method II

The goals of input protection can also be achieved by powering the input buffer from the same supplies as the converter as shown in Figure 4. This circuit requires fewer components than the circuit of Figure 1 and the use of com-

mon power supplies guarantees that the op-amp output will not exceed the ADC supply voltages. However, the required analog voltage to achieve full scale digital output for the CS5336 is typically  $\pm 3.68$  V and the majority of op-amps do not have this output capability with  $\pm 5$  V supplies.

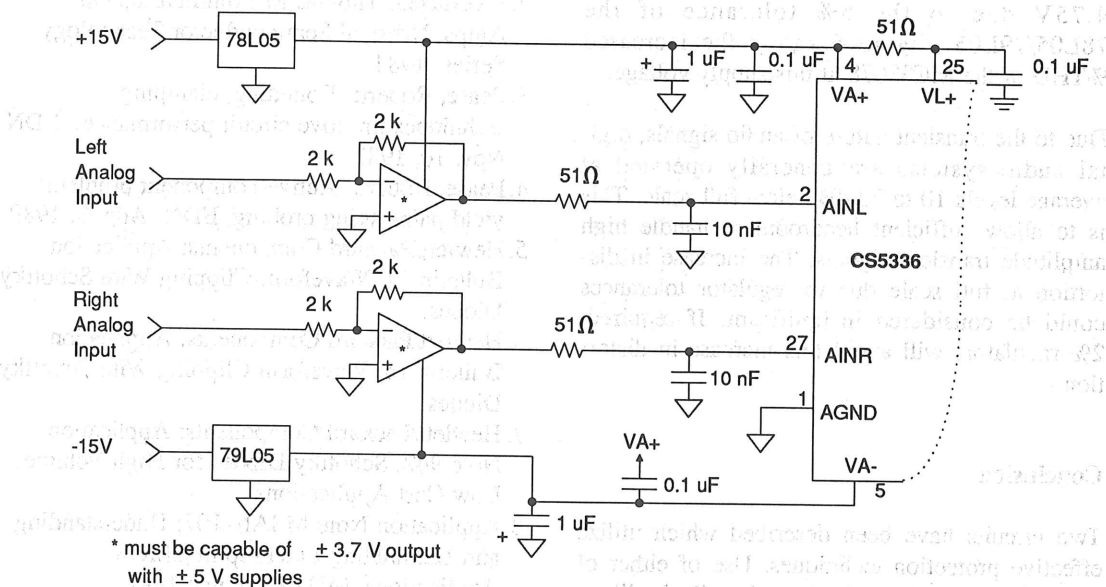
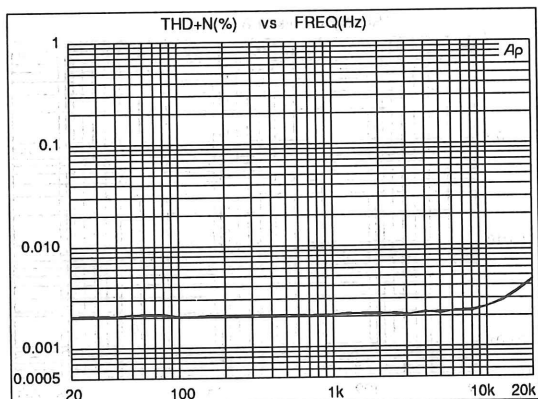


Figure 4. ADC Input Protection  $\pm 5$  V Op-Amp



**Figure 5. %THD Effects of Power Supply Variation for MC33078 at  $\pm 15V$  and  $\pm 5V$**

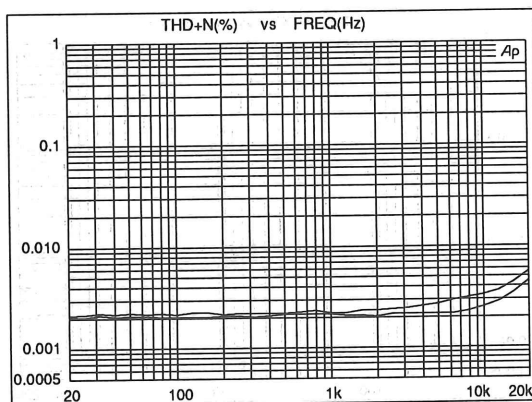
The Motorola MC33078/9 is a viable contender for this application. Figure 5 shows the %THD vs Frequency of the MC33078 with  $\pm 15V$  and  $\pm 5V$  supplies operating at 3.68 Vp. Note the lack of performance degradation resulting from the reduced supplies.

The power supply voltages could be as low as 4.75V due to the 5% tolerance of the 78L05/79L05. Figure 6 shows the increased %THD of the MC33078 at this supply voltage.

Due to the transient nature of audio signals, digital audio systems are generally operated at average levels 10 to 20 dB below full scale. This is to allow sufficient headroom to handle high amplitude transient signals. The increase in distortion at full scale due to regulator tolerances could be considered insignificant. If required, 2% regulators will avoid this increase in distortion.

## Conclusion

Two circuits have been described which utilize effective protection techniques. Use of either of these circuits or the techniques described will insure that the performance and reliability of a



**Figure 6. %THD Effects of Power Supply Variation for MC33078 at  $\pm 15V$  and  $\pm 4.75V$**

data acquisition system will not be limited by the input buffer and protection circuits.

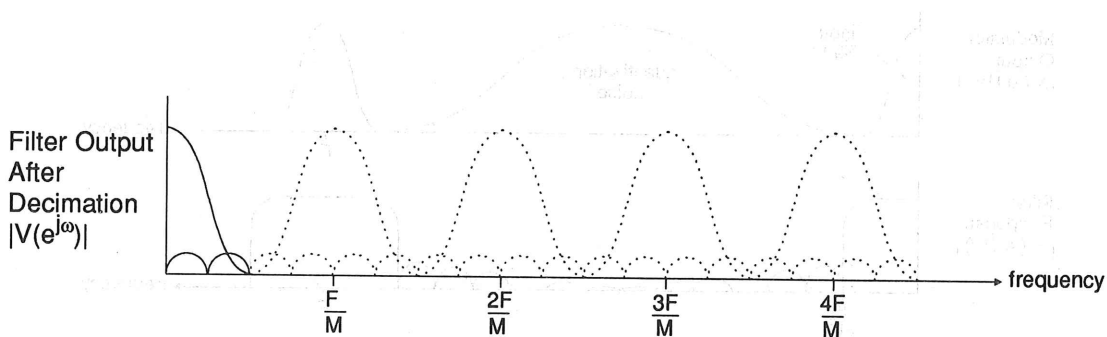
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6. Hewlett/Packard Components: Application Bulletin 15, Waveform Clipping With Schottky Diodes.
7. Hewlett/Packard Components: Application Note 942, Schottky Diodes for High Volume, Low Cost Applications
8. Application Note MSAN-107: Understanding and Eliminating Latch-up in CMOS Applications, MITEL August 1982

## Application Note

### Antialiasing Considerations for the CS5317

by  
Nav Sooch



# APPLICATION NOTE

## ANTIALIASING CONSIDERATIONS FOR THE CS5317

### Introduction:

Delta-Sigma A/D converters perform a rough A/D conversion at a high rate and digitally filter the output to obtain an accurate low frequency conversion. Since the input is initially sampled at a high rate and followed by a digital filter, the majority of antialias filtering is performed by the digital filter. However, aliasing problems due to

decimation still remain. These aliasing issues can be addressed by analog and/or digital filters. In general, the antialias filtering requirements of the CS5317 are simpler than those of conventional A/D converters. This application note describes the aliasing properties of the CS5317 and provides examples of filtering options.

Note: Antialiasing requirements are a function of the desired signal bandwidth and out-of-band energy. For simplicity, a clock rate of 4.096 MHz has been chosen for this note. If the actual clock rate is different, all the frequency values in this

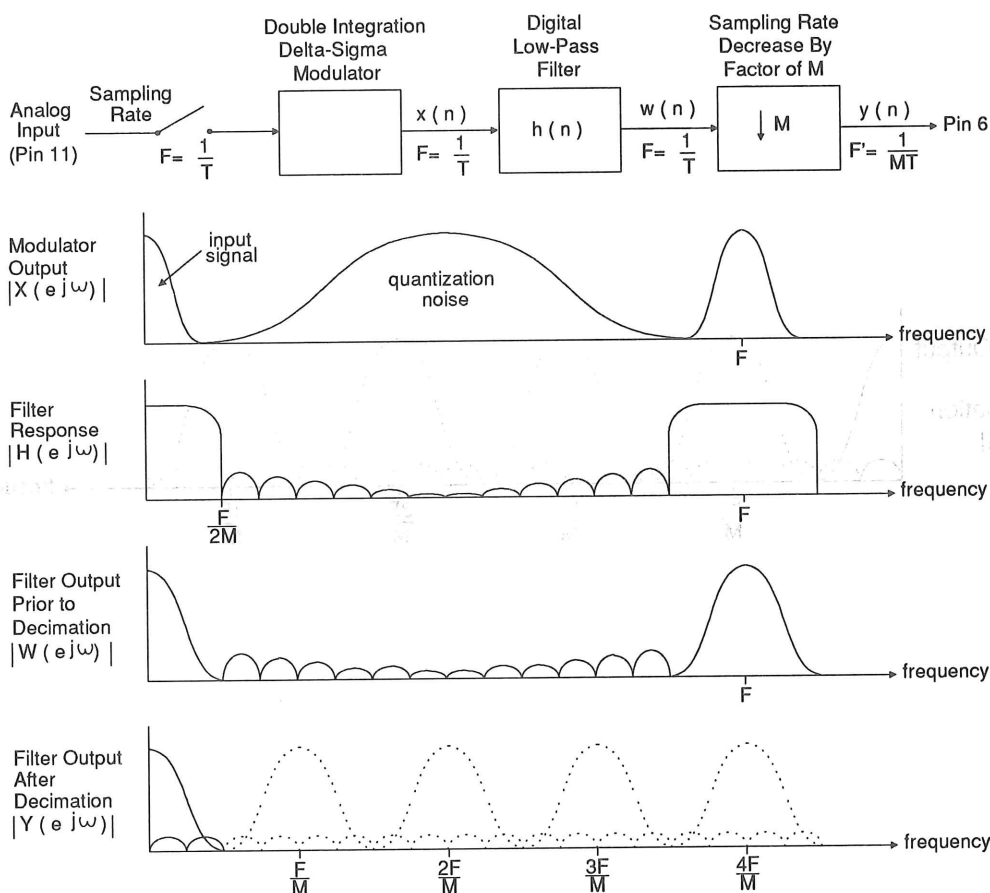


Figure 1. Block Diagram and Typical Spectra for Sampling Rate Reduction by a Factor of  $M$



note should be scaled by (actual clock rate)/(4.096 MHz).

### Initial Sampling:

The initial sampling of the analog input is done at 2.048 MHz. There is no internal filtering of frequencies at  $(2.048)n \text{ MHz} + 8 \text{ kHz}$  (where  $n = 1, 2, 3, \dots$ ). If signals in this band exist, an analog filter must attenuate them. Typically, a single-pole RC filter will suffice (see CS5317 data sheet).

### Decimation:

The process of digitally converting the sampling rate of a signal from a given rate  $F$  to a lower rate  $F'$  is called decimation. The decimation process is shown graphically in the frequency domain in Figure 1. The delta-sigma modulator output,  $x(n)$ , sampled at frequency  $F$  is fed into a low-pass filter with response  $h(n)$ . The output of this filter is decimated by a factor  $M$  to a new sampling rate of  $F' = F/M$ .

The analog modulator on the CS5317 is followed by a digital filter that has the following frequency response:

$$\text{Mag} | H(e^{j\omega}) | = \left| \frac{\sin(N\pi f/f_s)}{N \sin(\pi f/f_s)} \right|^3 \quad (1)$$

$$\text{where } N = 128 \text{ and } f_s = \frac{\text{CLKIN}}{2}$$

The digital filter's frequency response is plotted in Figure 2. The output rate of this digital filter is internally decimated to 16 kHz. Decimating to 16kHz implies that the output of the filter is effectively resampled at 16 kHz. Therefore, signals at multiples of 16 kHz will alias into the baseband after being attenuated according to the filter response defined in Equation 1. For example, an input tone at 28 kHz will be attenuated by 53.4 dB and will appear at 4 kHz in the output spectrum ( $2(16 \text{ kHz}) - 28 \text{ kHz} = 4 \text{ kHz}$ ).

Table 1 shows the antialiasing rejection at a few key frequencies.

Mag  $| H(e^{j\omega}) |$  (dB)

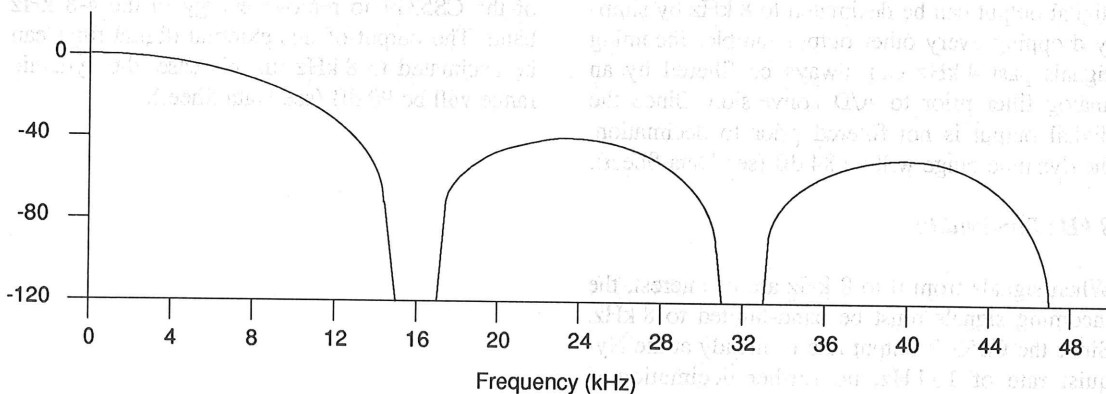


Figure 2. Low-Pass Filter Response

Input Frequency (kHz)	Output Frequency (kHz)	Attenuation (dB)
10	6	19.6
12	4	31.4
14	2	51.4
18	2	57.9
20	4	44.7
24	8	40.4
28	4	53.4
34	2	74.5

**Table 1. Antialiasing Rejection at Key Frequencies**

Note that the worst case rejection into the 0-4 kHz band is 31.4 dB for input signals at 12 kHz. Also note that very little rejection is provided for signals that alias into the 4-8 kHz band.

### ANTIALIASING STRATEGIES

One of the following three cases and associated antialiasing strategies should apply to any CS5317 application:

#### Case 1 -No Out of Band Energy

##### 4 kHz Bandwidth:

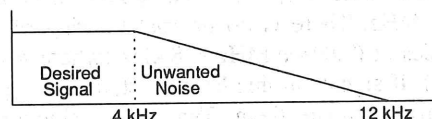
If there is no incoming energy past 4 kHz, the digital output can be decimated to 8 kHz by simply dropping every other output sample. Incoming signals past 4 kHz can always be filtered by an analog filter prior to A/D conversion. Since the digital output is not filtered prior to decimation, the dynamic range will be 84 dB (see Data Sheet).

##### 8 kHz Bandwidth:

When signals from 0 to 8 kHz are of interest, the incoming signals must be band-limited to 8 kHz. Since the CS5317 output rate is already at the Nyquist rate of 16 kHz, no further decimation is necessary. The dynamic range will be 84 dB.

#### Case 2 -Limited Out of Band Energy

Assume that the input signal has the following spectrum:



**Figure 3. Limited Out of Band Energy**

Two filtering methods are possible to prevent aliasing:

##### Analog Filter on Input

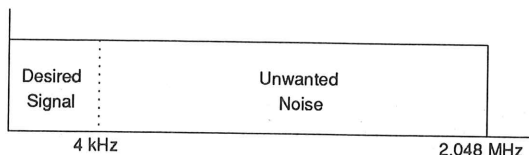
An analog filter can be used to remove the energy in the 4-12 kHz band prior to A/D conversion. The digital output of the CS5317 can be decimated to 8 kHz. If decimation is done without digital filtering, the dynamic range will be 84 dB (see Data Sheet).

##### Digital Filter on Output

Unwanted noise from 8 to 12 kHz will alias into the 4-8 kHz band after internal decimation in the CS5317. A digital filter can be used at the output of the CS5317 to remove energy in the 4-8 kHz band. The output of this external digital filter can be decimated to 8 kHz. In this case, the dynamic range will be 90 dB (see Data Sheet).

### Case 3 -Lots of Out of Band Energy

Assume that the input signal has the following spectrum:



**Figure 4. Lots of Out of Band Energy**

The following filtering possibilities exist:

#### *Analog Filter*

An analog filter can be used to remove energy past 4 kHz. The digital output of the CS5317 can be decimated (drop every other sample) to 8 kHz. If decimation is done without a post digital filter, then the dynamic range will be 84 dB (see Data Sheet).

#### *Analog and Digital filters*

A combination of analog and digital filters can be used. The digital filter can remove signals that alias into the 4-8 kHz band. As seen from Table 1, the frequencies that alias into the 4-8 kHz band are 8-12 kHz, 20-28 kHz, 36-44 kHz, and so on. The internal decimation filter on the CS5317 provides a minimum rejection of 31.4 dB for components in the 12-20 kHz and 28-36 kHz bands. Note that the requirements on this analog filter are significantly relaxed compared to the filter in the analog alone option (i.e. the transition band for this analog filter is much wider). Since a digital filter is used to remove energy in the 4-8 kHz band, the dynamic range will be 90 dB (see Data Sheet).

## •Notes•

The CS5317 is a high performance, low power, single-chip antialiasing filter. It is designed to be used in conjunction with a digital-to-analog converter (DAC) to filter the output of the DAC. The CS5317 is a fully differential, low-pass filter with a bandwidth of 10 MHz. It has a gain of 1 and a phase shift of 0 degrees. The CS5317 is available in a 16-pin DIP package.

The CS5317 is a high performance, low power, single-chip antialiasing filter. It is designed to be used in conjunction with a digital-to-analog converter (DAC) to filter the output of the DAC.



Figure 1. CS5317 Block Diagram

The CS5317 is a high performance, low power, single-chip antialiasing filter. It is designed to be used in conjunction with a digital-to-analog converter (DAC) to filter the output of the DAC.

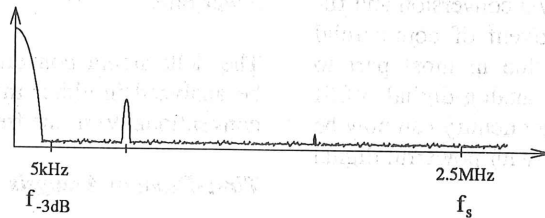
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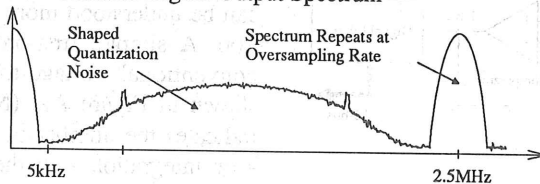
## Application Note

### Delta Sigma A/D Conversion Technique Overview

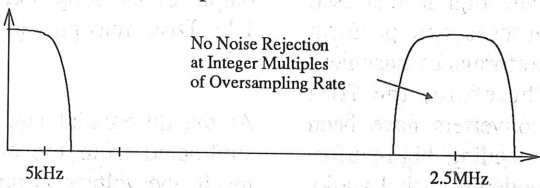
a. Analog Input Spectrum



b. Modulator Digital Output Spectrum

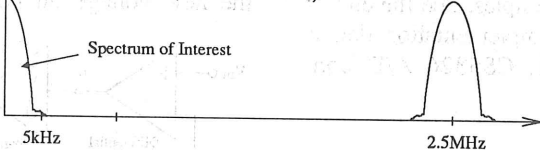


c. Digital Filter Response



d. Digital Filter Output Spectrum

(Before Decimation)



### SECTION A

#### OVERVIEW: DELTA-SIGMA MODULATION

Although developed over two decades ago, delta-sigma modulation has only recently achieved commercial implementation. The technique utilizes oversampling and digital filtering to achieve high performance in both A/D conversion and filtering at low cost. The advent of commercial delta-sigma converters is due in most part to recent advances in mixed analog-digital VLSI technology. Precision analog circuitry can now be integrated on the same chip with powerful digital filters.

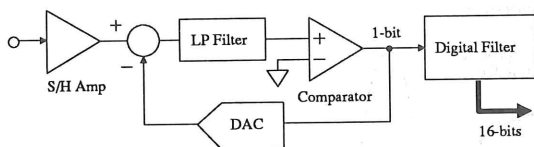


Figure A1. Delta-Sigma ADC

In a delta-sigma ADC, the same digital filter used in the A/D conversion process can perform system-level filtering with performance unachievable in analog form. Therefore, the first commercial delta-sigma converters have been targeted at applications demanding high-performance filtering (high-end modems, digital audio, geophysical exploration, etc).

This application note uses the CS5317 voice band A/D converter for examples. See the end of this application note for implementation details for the CS5317, CS5501, CS5326 A/D converters.

#### Fundamentals

A delta-sigma ADC consists of two basic blocks: an analog modulator and a digital filter (see Figure A1). The fundamental principle behind the modulator is that of a single-bit A/D converter

embedded in an analog negative feedback loop with high open loop gain. The modulator loop oversamples and processes the analog input at a rate much higher than the bandwidth of interest. The modulator's output provides small packages of information (that is, 1-bit) at a very high rate and in a format that the digital filter can process to extract higher resolution (such as 16-bits) at a lower rate.

The delta-sigma converter's basic operation can be analyzed in either the time domain, or (more conventionally) in the frequency domain.

#### Time-Domain Analysis

The basic operation of a delta-sigma modulator can be understood more intuitively by demonstration. A simple, first-order modulator (that is, a conventional voltage-to-frequency converter) is shown in Figure A2. (Note: a modulator's order indicates the number of orders of analog filtering - or integration - in the loop). Full-scale inputs are  $\pm 1V$  and three nodes are labeled  $V_1$ ,  $V_2$ , and  $V_3$ . The output of the comparator, node  $V_3$ , is the output of the loop and is also converted by the 1-bit DAC into plus or minus full-scale ( $+1V$  or  $-1V$ ).

At the differential amplifier, the  $+1V$  or  $-1V$  is subtracted from the analog input voltage. The result, the voltage at node  $V_1$ , is input to the integrator. The integrator acts as an analog accumulator; ie. the input voltage at node  $V_1$  is added to the voltage on node  $V_2$  which becomes the new voltage on node  $V_2$ . Node  $V_2$  is then

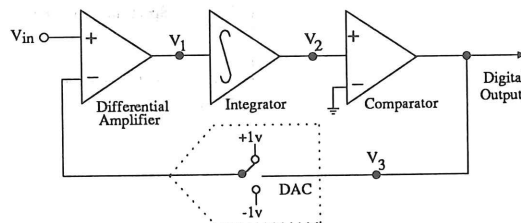


Figure A2. 1<sup>st</sup>-order Delta-Sigma Modulator

compared to ground. If it is greater than ground, node V<sub>3</sub> becomes +1V; if it is less than ground, V<sub>3</sub> becomes -1V. Each operation occurs once during each clock cycle.

In the example shown in Table A1, all nodes are initially set to zero, and the analog input voltage is assumed to be 0.6V. Since all nodes are identical in clock cycles two and seven, the period defined by cycles two to six will repeat if the analog input remains unchanged. The average value of modulator outputs (at node V<sub>3</sub>) during that period, 0.6, yields a numerical representation of the analog input.

Clock Period	V <sub>1</sub>	V <sub>2</sub>	V <sub>3</sub>	Period Avg
0	0	0	0	
1	0.6	0.6	1	
2	-0.4	0.2	1	0.6
3	-0.4	-0.2	-1	
4	1.6	1.4	1	
5	-0.4	1.0	1	
6	-0.4	0.6	1	
7	-0.4	0.2	1	
8	-0.4	-0.2	-1	

Table A1. Modulator Walk-Through

With conventional voltage-to-frequency converters a digital counter is used to extract the information in the VFC's 1-bit output. Pulses are counted over a specified period, effectively creating a digital averaging (or integrating) filter. The final count represents the average analog input value during the integrating period.

Advanced delta-sigma converters use higher-order modulators and more powerful digital filters. For example, the CS5317 uses a second-order modulator. The pattern of transitions in its 1-bit output provides more useful information regarding higher resolution at higher frequencies.

However, a more sophisticated digital filter than a counter is needed to interpret that information. A digital FIR filter is basically a rolling, weighted average of consecutive samples (see Appendix B). An averaging filter weights all samples equally. By applying a more sophisticated weighting function to the 1-bit signal, a digital FIR filter can assemble an N-bit output (with  $2^N$  possible values) without having to wait for  $2^N$  samples.

### The Charge-Balance Name

Delta-sigma ADC's are also known by other names - sigma delta and charge-balance are two examples. The *Charge-Balance* name derives from the fact that the modulator tries to *balance* the analog input with the DAC's output in the negative feedback loop. The charge injected onto the integrator's capacitor from sampling the analog input (see Figure A2) is therefore balanced by the charge injected by the DAC's output. Modulators have been implemented in both switched-capacitor and continuous-time form.

### Frequency-Domain Analysis

Since filtering plays a key role in a delta-sigma ADC, it is easier to understand the converter's operation by analyzing it in the frequency domain.

### Overview

An A/D converter's resolution determines its dynamic range (or signal-to-noise ratio). Conversely, one can improve a converter's signal-to-noise ratio and thereby increase its effective resolution. The fundamental concept behind delta-sigma converters is to perform a simple, low-resolution A/D conversion and reduce the resulting "quantization noise" (without affecting the frequency band of interest) using analog and digital filtering.

### Quantization Noise

The comparator in the delta-sigma modulator loop plays the role of a 1-bit A/D converter. Any A/D converter can represent a continuous analog input by one of only a *finite* number of codes, giving rise to an uncertainty, or quantization error, of up to  $\pm 1/2$  LSB. For a consecutive sequence of samples in a waveform, these quantization effects can be modeled as a random noise source under conditions commonly encountered in signal processing applications. (These conditions hold true for delta-sigma modulators). The rms value of the noise source relative to a full-scale input can be shown to equal  $-(6.02 N + 1.76)$  dB, for an N-bit resolution converter. Since this error "signal" is totally random (or uncorrelated with the input) it can be assumed to be white, with its energy spread uniformly over the band from dc to one-half the sampling rate.

As a 1-bit ADC, the comparator in a delta-sigma modulator offers (an almost comical) 7.78 dB signal-to-noise ratio. However, the input signal is grossly oversampled (2.5 MHz in the CS5317), thus spreading the quantization noise over a wide bandwidth (1.25 MHz). The noise density in the bandwidth of interest (5 kHz) is therefore reduced.

### Noise Shaping

Analog filtering is used in the modulator loop to further reduce noise density in the frequency band of interest by shaping the quantization noise spectrum. The spectrum of the input signal, meanwhile, remains unaltered. Figure A3 shows a modulator loop with analog and digital circuit differences ignored. The comparator is simply shown as a (quantization) noise source, and the analog filtering, which is simply an integrator, assumes the filter response  $H(f)$ . If the analog input equals zero, then

$$D_{out} = Q(n) - H(f) D_{out}$$

$$D_{out} = \frac{Q(n)}{1 + H(f)}$$

The quantization noise at the output is reduced by the open-loop gain of the integrator. At low frequency, the integrator is designed for high open-loop gain, so that quantization noise is reduced. As shown in Figure A4b, the integrator effectively pushes the quantization noise out of the bandwidth of interest and into higher frequencies. Digital lowpass filtering then removes the quantization noise at the higher frequencies without affecting the low-frequency spectrum of interest.

The spectral characteristics of the analog loop filtering dictates the delta-sigma converter's resolution/bandwidth ratio. Higher-order integrators improve noise shaping and allow for higher resolutions at wider bandwidths. The CS5317 uses a second-order modulator for superior noise shaping.

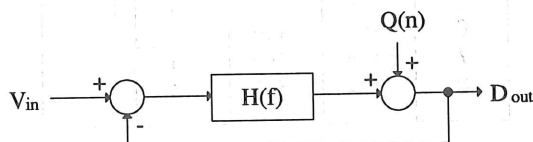


Figure A3. Analog Modulator Model

### Digital Filtering

The spectral characteristics of the back-end digital filtering also affects the delta-sigma converter's resolution/bandwidth ratio. Faster roll-off and greater stopband rejection reduces residual quantization noise. Section B offers a detailed explanation of the theory behind digital filtering.

### Anti-Alias Requirements

As shown in Figure A4, the input and digital filtering spectrum of any ADC repeats around integer multiples of its sampling rate. A delta-



sigma ADC thus does not provide noise rejection in the region around integer multiples of the sampling rate ( $\pm 5$  kHz around 2.5 MHz, 5 MHz, 7.5 MHz...). If noise exists in the system in these narrow bands, analog filtering is needed to remove it at the converter's input otherwise it will alias and pass unfiltered to the converter's output.

Since delta-sigma ADC's are grossly over-sampled, anti-alias filtering requirements are often trivial. For instance, the CS5317 provides a factor of 500 of oversampling (2.5 MHz/5 kHz). A single-pole, passive RC filter at the CS5317's input is therefore sufficient in most applications.

### Decimation

Even though the delta-sigma ADC oversamples and processes analog samples at a frequency well above the bandwidth of interest, it will generally offer its high-resolution output at a much-lower system sampling rate. Any reduction in sampling rate is termed *decimation*. The output can be further decimated at the system level by selectively reading a fraction of the available samples (for instance, every tenth sample). Independent of the decimation ratio, the converter's noise performance (and effective resolution) remains unchanged.

### Conversion Accuracy/Performance

Like integrating ADC's and V/F converters, a delta-sigma ADC does not contain any source of nonmonotonicity and thereby offers "theoretically perfect" DNL with no missing codes. The ADC in the modulator is simply a comparator, and the DAC is the positive and negative voltage references. No precision ratio matching is needed as in other medium- or high-speed A/D conversion techniques such as successive-approximation. Useful resolution is limited only by residual quantization noise which, in turn, is determined by coarse analog and high-performance digital filtering.

Linearity error is limited only by imperfections in the input sample/hold. The CS5317 achieves typical nonlinearity of just  $\pm 0.003$  % through the use of high-quality on-chip silicon dioxide capacitors with low capacitor voltage coefficient.

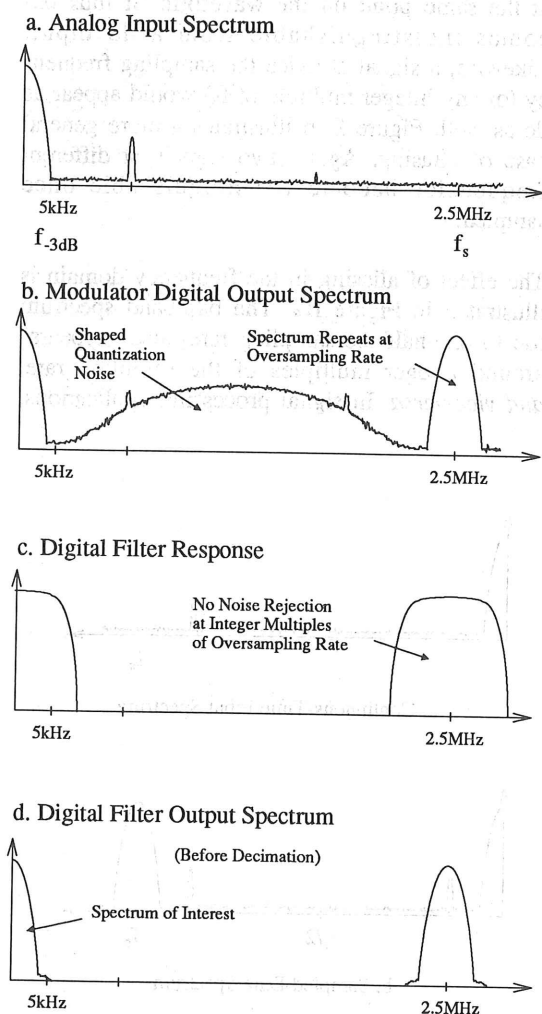


Figure A4. Delta-Sigma Spectral Analysis  
(Using frequencies taken from the CS5317 A/D Converter)

### SECTION B

#### OVERVIEW: DIGITAL FILTERING

A conventional analog filter implements a mathematical equation using reactive components (capacitors and inductors). A digital filter can implement the same filter equation using two fundamental arithmetic operations: multiplication and addition (or accumulation). A digital filter considers a consecutive sequence of digitized samples a "waveform." It analyzes the relationship between samples, processes the data, and outputs an adjusted waveform.

Digital filters offer ideal stability, repeatability, and potentially perfect performance (linear phase, etc.). Digital filters also remain impervious to environmental conditions, thus providing superior reliability over time and temperature. The major difference compared to analog filters, though, is that digital filters operate on a signal in sampled form.

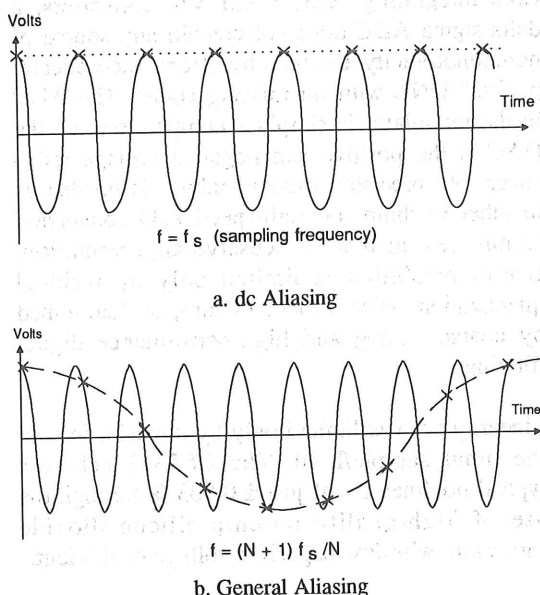


Figure B1. Aliasing in Sampled-Data Systems

#### Sampled-Data Theory

A fundamental phenomenon in sampled-data systems is an effect called "aliasing." Basically, *once an analog signal is sampled, its frequency components are no longer uniquely distinguishable.* Figure B1a shows a special case called "dc aliasing." If a signal is sampled precisely at its fundamental frequency, it will always be sampled at the same point on the waveform. It thus becomes indistinguishable from a dc input. Likewise, a signal at twice the sampling frequency (or any integer multiple of  $f_s$ ) would appear as dc as well. Figure B1b illustrates a more general case of aliasing. Again, two signals at different frequencies become indistinguishable once sampled.

The effect of aliasing in the frequency domain is illustrated in Figure B2. The baseband spectrum (dc to one-half the sampling rate) also "appears" around integer multiples of the sampling rate, and vice-versa. In signal processing applications,

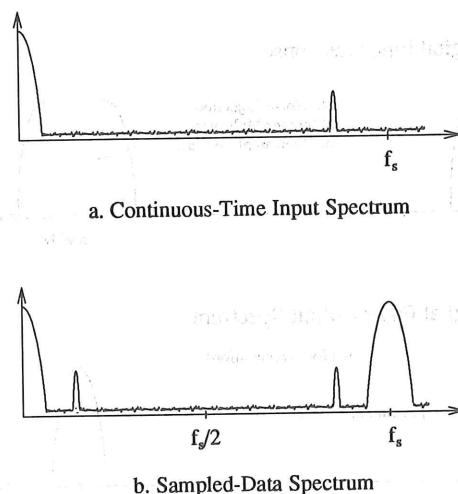


Figure B2. Sampled-Data Spectrum

anti-alias filtering is used to bandlimit the analog signal before it is sampled. This removes out-of-band components which could be mistaken for important information in the band of interest.

Aliasing is critical in digital filtering. A digital filter is incapable of distinguishing signals in its passband from signals aliasing from around its sampling frequency. Its passband spectrum therefore repeats around integer multiples of the sampling frequency. Take for instance the case of dc aliasing shown in Figure B1a. A digital low-pass filter would treat the signal at  $f_s$  as a dc input and pass it with no attenuation. Similarly, if the filter would attenuate the lower-frequency signal in Figure B1b by 10 dB, the higher-frequency signal would receive the same 10 dB of attenuation. The higher-frequency signals in both cases could be selectively filtered only by analog anti-alias filtering *before the signal is sampled*.

Sampling rates are usually set high enough that analog anti-alias requirements become trivial (or perhaps eliminated). Higher oversampling ratios offer greater bandwidth to roll off between the passband and sampling frequency. Noise in the digital domain can be analyzed just as it is in the analog domain. Limiting a system's bandwidth will reduce noise and improve dynamic range.

### Digital Filtering

The most popular digital filtering technique is averaging. A sequence of digital samples are simply collected and averaged to produce an output. This reduces noise by limiting the effective noise bandwidth. Averaging yields a  $(\sin x)/x$  (or sinc) filter response as shown in Figure B3. The zeroes of infinite rejection (at  $f_s/N$ ,  $2f_s/N$ ,  $3f_s/N$ , etc.) can be strategically placed by selecting  $f_s$  and the number of samples averaged,  $N$ , to average over an integral number of periods of critical frequencies (50 Hz, 60 Hz, etc.). Of course, this same principle lies at the heart of integrating ADC's, but the averaging is done in analog form. In both cases greater dynamic range

(or resolution) can be achieved by increasing integration time. The trade-off is bandwidth.

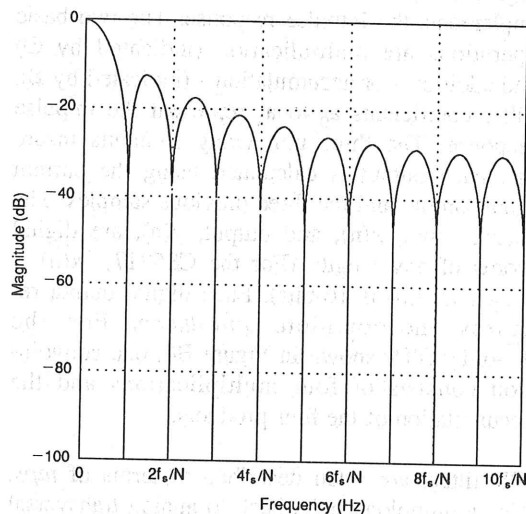


Figure B3. Averaging Filter Response

### FIR Filters

Averaging is an elementary example of FIR, or *Finite Impulse Response*, digital filtering. Finite Impulse Response indicates that the filter considers only a *finite* number of inputs to calculate each output. The number of samples determines the *impulse response duration*. For example, a filter which averages ten samples has an impulse response duration of ten. Longer durations indicate more information is considered for each calculation, resulting in a more powerful filter response.

A digital filter's *impulse response* is what determines its filter function. It is basically a weighting function applied to the sequence of samples being considered. The averaging filter is an elementary example of an FIR filter because it uses equal weighting (weight =  $1/N$  where  $N$  = # samples). More sophisticated impulse responses extract the information contained in the *relation-*

ship between samples. Averaging filters ignore this information.

Figure B4 illustrates how an FIR filter actually implements the impulse response. The two basic operations are multiplication (indicated by  $\otimes$ ) and addition - or accumulation - (indicated by  $\Sigma$ ). Filter coefficients  $a_0$  to  $a_3$  represent the impulse response. The three unit delay elements insure that each output is calculated using the current input sample and the three previous samples. The filter's input,  $x(n)$ , and output,  $y(n)$ , are digital words of any length. (For the CS5317,  $x(n)$  is 1-bit and  $y(n)$  is 16-bits). Each digital output requires one complete convolution. For the 4<sup>th</sup>-order filter shown in Figure B4, one convolution consists of four multiplications and the accumulation of the four products.

FIR filters are often described in terms of *taps*. This terminology hails back to analog transversal filters, which were basically analog implementations of the filter in Figure B4. The analog delay elements were termed taps. The number of taps indicated the filter's impulse duration. The longer the duration, the more powerful the filter.

### Decimation

Digital filters often operate with input sampling rates well above the bandwidth of interest. This serves to minimize analog anti-alias filtering requirements. The filter's output rate, however, is

generally dropped to a more manageable system sampling rate. Any reduction in sampling rate is termed *decimation*.

To illustrate the decimation process lets return to averaging. A filter which collects ten samples and then averages them to produce one output *decimates by ten*. That is, for an input rate of  $f_s$ , the output rate is  $f_s/10$ . Alternatively, one could use a "rolling average." For each input sample received, an output would be calculated using that sample and the nine previous samples. The sampling rate would therefore remain at  $f_s$  with no decimation.

The 4<sup>th</sup>-order FIR filter in Figure B5 exhibits the same filter response as that in Figure B4, but decimates by a factor of four. In this case, only one multiplication is performed per input cycle. Without any delay elements, the accumulator needs four input cycles to complete one convolution. Output samples are therefore produced at  $f_s/4$ . Decimation clearly relaxes computational complexity.

Decimation does not affect overall signal-to-noise or dynamic range. For this reason, one can decimate the CS5317's 20 kHz output (by selectively reading a fraction of the available samples) without affecting the converter's noise. However, a digital signal is normally not decimated if additional filtering is to be used to increase dynamic range (and resolution). All noise energy in a

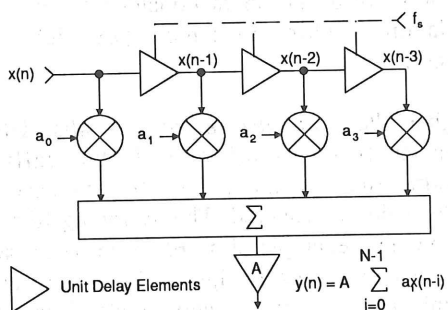


Figure B4. 4<sup>th</sup>-order FIR Filter

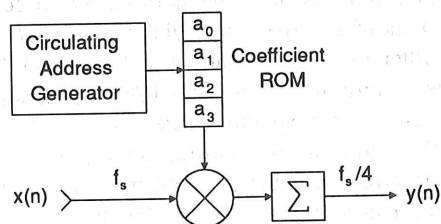


Figure B5. 4<sup>th</sup>-order FIR Filter with 4X Decimation

sampled signal lies between dc and one-half the sampling rate. Lower sampling rates therefore exhibit larger noise *densities* in the bandwidth of interest for a given amount of noise energy due to aliasing.

### FIR Characteristics

The only source of inaccuracy in digital filters is rounding errors due to finite word lengths in the computations. If properly designed, a digital filter will not induce linearity, offset, or gain errors.

Aside from their simplicity, FIR filters' most popular characteristic is their ability to implement perfectly linear phase filters. The effect of every input sample on the output is always seen a *fixed* number of cycles later. This processing delay from input to output is termed the filter's *group delay*, and can be shown to equal one-half the impulse response duration.

Unfortunately, FIR filters can only implement zeroes, no poles. Roll-off is therefore limited. Of course, this limitation can be overcome by cascading FIR filters to produce an extraordinarily long impulse duration. (Fortunately stability is not an issue with FIR filters). The trade-off, though, is an extraordinarily long group delay.

### IIR Filters

*Infinite Impulse Response* filters, on the other hand, can implement zeroes and poles to achieve high roll-off. Unlike FIR filters, which use previous inputs to calculate an output, IIR filters also utilize *historical output information* to calculate each new output. In this manner, IIR filters can implement mathematical filter equations with variables in the denominator (that is, poles).

The only drawback to IIR filters is their computational complexity. Since their computations use historical information on their past outputs, *each output must be calculated*. That is, unlike FIR filters an IIR filter cannot decimate to reduce

computational complexity. Therefore, IIR filters generally operate with lower sampling rates.

### The CS5317 Voice-band A/D Converter Implementation

The CS5317 uses oversampling, decimation, and FIR filtering to implement its digital filter. The CS5317 samples its analog input at 2.5 MHz (for a full-rated 5 MHz master clock). This high oversampling ratio of 500:1 (2.5 MHz sampling/5 kHz bandwidth) reduces external analog anti-alias requirements.

The FIR filter decimates the sampling rate from 2.5 MHz to 20 kHz to reduce computational complexity. The filter features an impulse response duration of  $384 \times 2.5$  MHz and a decimation ratio of 128 (2.5 MHz:20 kHz). Since the filter does not decimate by 384 as shown in Figure B5, multiple convolutions must be in process concurrently. To achieve this, the CS5317 uses three accumulators working from a single 384-word coefficient memory. The three convolutions are spaced to begin and end 128 samples apart. Thus, a new 16-bit output sample becomes available every 128 input samples (for a decimation ratio of 128) whereas each 16-bit output is calculated using 384 input samples (for an impulse response duration of 384).

### The CS5501 dc Measurement A/D Converter Implementation

The CS5501 uses oversampling, decimation, and both FIR and IIR filtering to implement its 6-pole Gaussian filter. The CS5501 samples its analog input at 16kHz (for a full-rated 4.096MHz master clock). This high oversampling ratio of 1600:1 (16kHz sampling/10Hz bandwidth) reduces and most often eliminates external analog anti-alias requirements.

The FIR filter is used to decimate the sampling rate from 16kHz to 4kHz to reduce computational complexity in the subsequent IIR filter. The

FIR filter response is not especially critical. Its only goal is to reject energy within  $\pm 10\text{Hz}$  bands around integer multiples of  $4\text{kHz}$ , the IIR filter's sampling rate.

The IIR filter is needed to implement the poles in the 6<sup>th</sup>-order Gaussian filter and achieve high roll-off of  $120\text{dB/decade}$ . Its baseband filter characteristics are shown on page 4. Note that the filter's entire frequency response can be scaled by adjusting the master clock. The converter's sampling rate simply scales accordingly. With its cut-off frequency set at  $10\text{Hz}$  ( $4.096\text{MHz}$  master clock) for maximized settling, the CS5501 offers  $55\text{dB}$  rejection at  $60\text{Hz}$ . With a  $5\text{Hz}$  cut-off, though,  $60\text{Hz}$  rejection increases to greater than  $90\text{dB}$ . Master clocks as low as  $40.96\text{kHz}$  are acceptable, yielding cut-off frequencies as low as  $0.1\text{Hz}$ .

### The CS5326 Digital Audio A/D Converter Implementation

Linear-phase finite-impulse-response (FIR) filters are used for decimation. The 1-bit,  $3.072\text{MHz}$  outputs of the modulators are decimated in steps of 8, 4, and 2 to yield 16-bit,  $48\text{kHz}$  results.

The decimation strategy includes two stages, FIR1 and FIR2, whose primary responsibility is attenuation of quantization noise prior to decimation and aliasing. Modulator out-of-band quantization noise spectral density is very high. FIR1 and FIR2 use 17 and 18-bit coefficients to attenuate this noise, and out-of-band input signals, into the converter noise floor. Filter orders are 27 and 30, respectively.

A third stage, FIR3, performs passband shaping and out-of-band signal attenuation. Passband frequency response errors introduced by the modulator, FIR1, and FIR2 are corrected by FIR3. Overall filter passband ripple is thus reduced to  $\pm 0.001\text{dB}$  from dc to  $22\text{kHz}$ . The passband compensation function prevents the use of a half-band filter for FIR3. Data is truncated to

16 bits at the output, and this operation is the major noise contributor in the system.

FIR1, FIR2, and FIR3 also combine to provide antialiasing filtering. All analog input frequencies from  $26\text{kHz}$  to  $3046\text{kHz}$  are attenuated by at least  $86\text{dB}$ . Phase response is precisely linear.



**Application Note**

**CS5326 to DSP56000 Interface**

By Clif Sanchez

This application note describes the interface needed to connect the CS5326 to the Motorola DSP56000 Digital Signal Processor.

Since the CS5326 is a stereo delta-sigma oversampled analog-to-digital converter, it requires three clocks: a master clock to sample the analog input, a serial clock to shift out data,

and a left/right clock to select the channel. The 74HC590 synchronous counter from TI, along with a couple of inverters, provide all the clocks that the CS5326 requires. The output previous to L/R,  $Q_F$ , is used as a frame sync for the DSP56000 and connects to SC2 which is configured as FSr. For the DSP56000, the FSL bit must be set equal to zero.

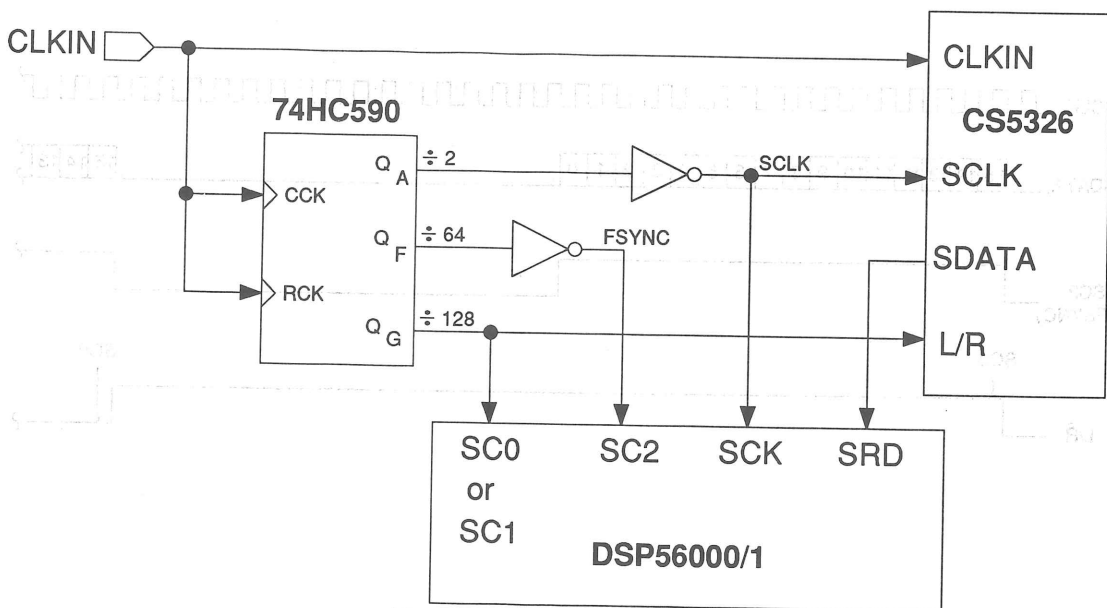
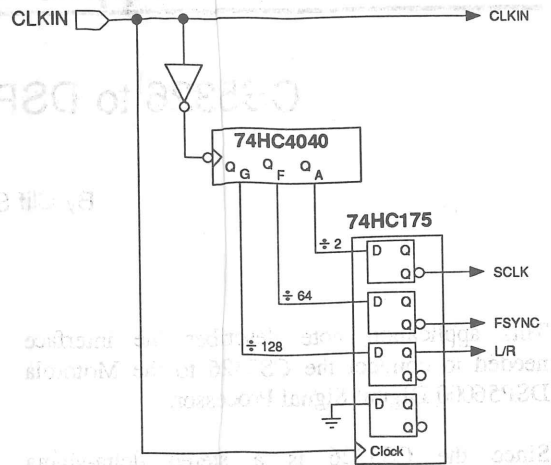


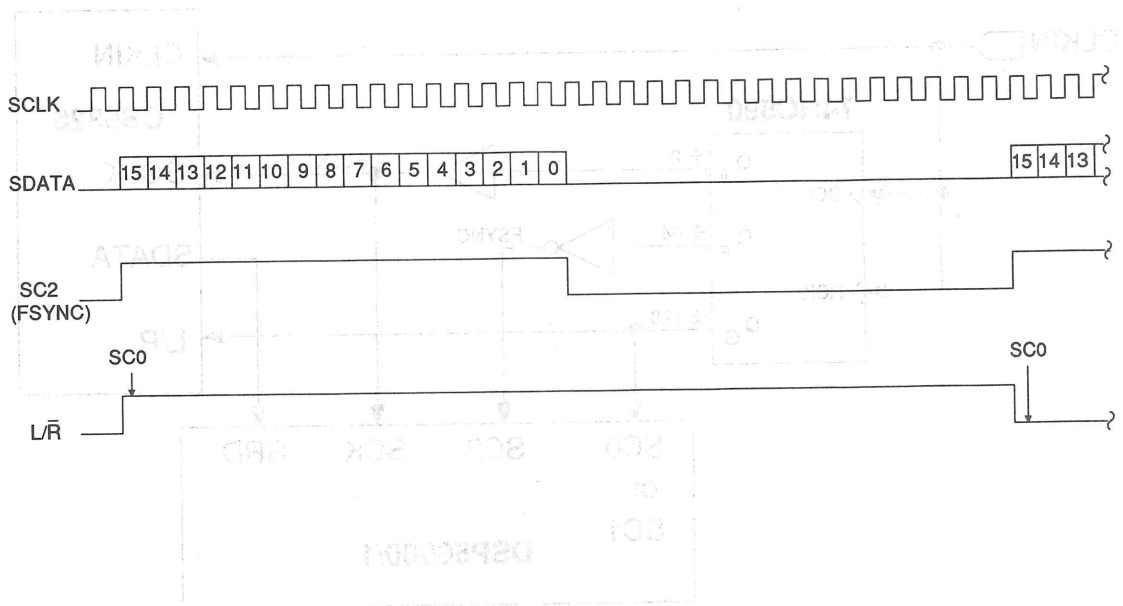
Figure 1. CS5326 to DSP56000 Connection Diagram

If the DSP56000 serial port is in the synchronous mode, then the serial port transmit and receive sections used the same serial clock. This releases two pins, SC0 and SC1, and one can be configured as an input flag indicating the channel, left or right. They are latched in the DSP56000 at the same time as the MSB (see Figure 2) and can be used to synchronize left/right pairs.

If a synchronous counter is not available, a similar circuit can be constructed from a ripple counter and latch as shown in Figure 3. Since the D flip-flops provide inverted outputs, the output inverters are not needed. But the 74HC4040 ripple counter's clock must be inverted to give it enough time, one full clock instead of one half clock, to settle before the flip-flops latch the data.



**Figure 3. Alternate to 74HC590**



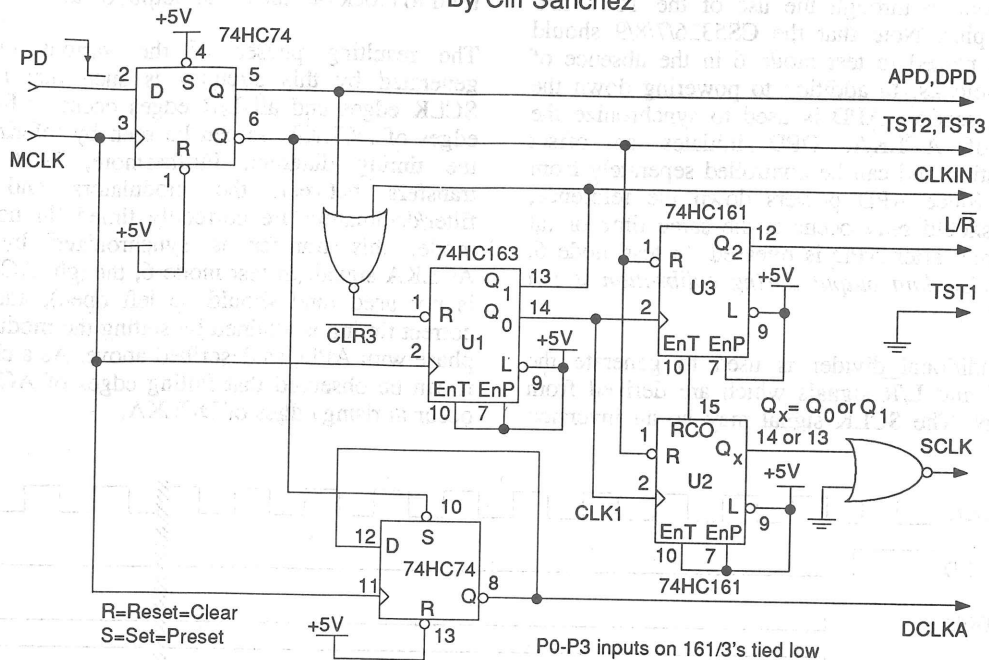
**Figure 2. CS5326 to DSP56000 Timing Diagram**



## Application Note

### CS5326/7/8/9 Low Frequency Operation

By Clif Sanchez



This circuit places the CS5326/7/8/9 in test mode 6 and provides clocks with the proper frequencies and relative phases to operate the converter at speeds lower than specification.

In normal operation (i.e., not in a test mode), the CS5326/7/8/9 utilizes a phase lock loop circuit to implement a 3X clock frequency multiplier, the output of which paces the digital filter/decimators. The limited range of the PLL results in a lower bound to the speed of operation. The ACLKA output is normally connected to the DCLKA input, and it is this clock signal that is the input to the 3X frequency multiplier.

In test mode 6, the 3X multiplier is disabled, and the clock required for the digital filter/decimators

is instead received directly on the DCLKA pin. The lower bound on the speed of operation is dramatically reduced (still non-zero due to internal dynamic logic), but the DCLKA signal frequency must be appropriately generated. The requisite frequency is 1.5X the frequency of the CLKIN signal. This ratio mimics the combination of the divide-by-two between CLKIN and ACLKA/DCLKA and the multiply-by-three between ACLKA/DCLKA and the filter/decimators' clock that occurs in normal operation.

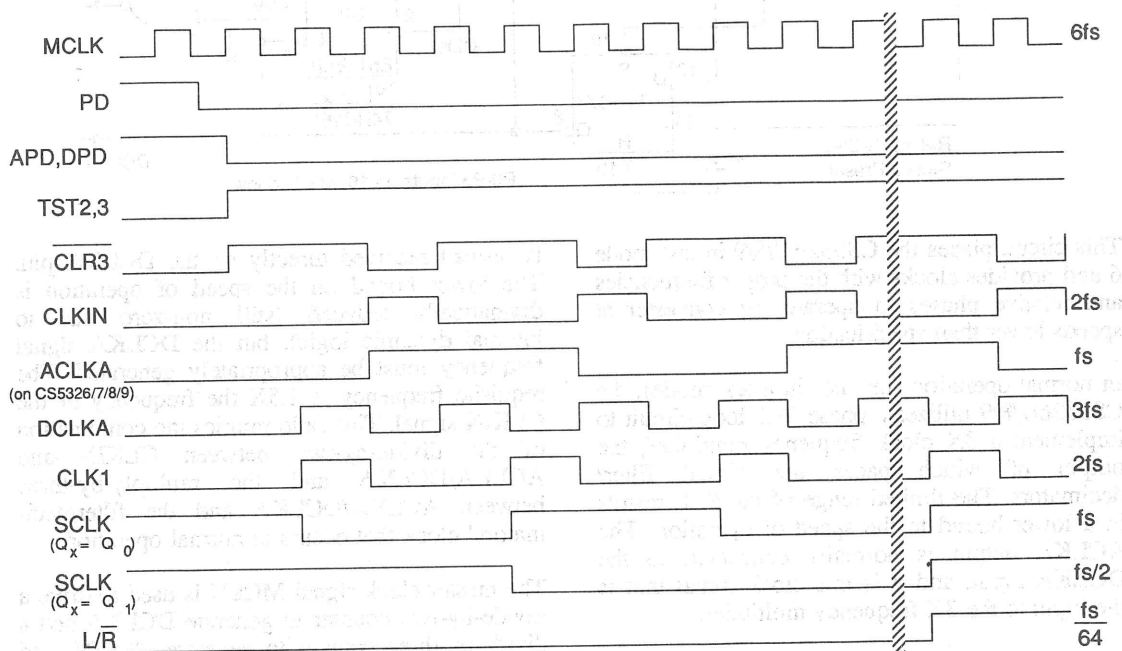
The master clock signal MCLK is used to drive a divide-by-two counter to generate DCLKA and a divide-by-three counter to generate CLKIN, and to synchronize the PD (Power-Down) signal. The latter is used to appropriately reset the phase of

the counters as well as that of the delta-sigma modulators in the CS5326/7/8/9 (this is done through the use of the APD signal). In addition, when PD falls, the complementary output of the synchronizing flip-flop places the converter in test mode 6 through the use of the TST2 and TST3 pins. Note that the CS5326/7/8/9 should not be placed in test mode 6 in the absence of active clocks. In addition to powering down the analog section, APD is used to synchronize the start of ACLKA. DPD initiates an offset calibration and can be controlled separately from APD. Since APD powers down the reference, DPD should only occur at the same time or (at any time) after APD is released. In test mode 6, the serial data output during calibration is not all zeros.

An additional divider is used to generate the SCLK and L/R signals which are derived from CLKIN. The SCLK signal may be an inversion

of either Q0 or Q1. Using Q1, though, results in an SCLK frequency that can slightly raise the noise floor of the CS5326/7/8/9 through interference effects with the modulators. If receive circuitry speed permits, Q0 should be used to clock out the serial output data.

The resulting phases of the various clocks generated by this circuitry is such that rising SCLK edges and all L/R edges occur at falling edges of DCLKA, as can be seen by referring to the timing diagram. Furthermore, 1-bit data transfers between the modulators and the filter/decimators are correctly timed. In normal mode, this transfer is synchronized by the ACLKA signal. In test mode 6, though, ACLKA is not used (and should be left open), and the correct timing is attained by setting the modulator phase with APD, as described above. As a check, it can be observed that falling edges of ACLKA occur at rising edges of DCLKA.



- Notes:
1.  $Q_x = Q_0$  is recommended for SCLK to avoid adverse analog interference effects caused by  $fs/2$  signals.
  2. L/R is a square wave with edges coincident with SCLK rising edges.
  3. fs is analog sampling frequency.

## **An 18-Bit Dual Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example**

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### **ABSTRACT**

The architecture and performance of a stereo 18-bit delta-sigma analog-to-digital converter are discussed. This 28-pin device contains dual delta-sigma modulators and dual digital filters/decimators. Special emphasis is placed on applications examples using the A/D converter in various common audio environments including AES/EBU integrated circuits and digital signal processors. In addition, an example application is discussed in which the dual channel 18-bit part is configured as a single 19-bit A/D converter yielding a dynamic range of 100 dB.

### **0 INTRODUCTION**

The benefits of using digital to store and process audio information are well documented[1]; however, the number of bits required to reproduce the analog signal to an acceptable level is still in flux. Consumer products are standardizing on the 16-bit level[2] while professional equipment manufacturers are asking for more[3,4].

Sec. 1 describes the architecture of the CS5328, a stereo 18-bit delta-sigma analog-to-digital (A/D) converter. Sec. 2 illustrates the performance of the A/D converter under a variety of test conditions. Also discussed is a 19-bit monaural example in which both input channels are tied together and the output words are summed, achieving a dynamic range of 100 dB over the 0-20 kHz audio band. Sec. 3 describes interfaces to common audio environments such as AES/EBU integrated circuits and the Philips I<sup>2</sup>S bus, while Sec. 4 discusses DSP interfaces. Sec. 5 discusses a method of attaching the channel indication, left or right, as a tag to the end of the serial data stream.

### **1 ARCHITECTURE**

The architecture of the CS5328, as seen in Figure 1, consists of two one-bit delta-sigma modulators[5] that oversample the analog input at a frequency that is 64 times the output word rate. Each delta-sigma modulator is followed by a 3-stage FIR filter. Dividing the filtering function into

three stages allows for an overall reduction in the number of required taps and incremental decimation to arrive at the output word rate. The output of each channel is latched and multiplexed on the SDATA pin under control of the L/R (left/right) signal. L/R also starts the convolution for the FIR filters.

The digital filter response is illustrated in Figure 2 for a 48 kHz output word rate and has a stopband rejection of greater than 86 dB. Since the filter is digital, the frequency response will scale with clock frequency allowing the use of other sample frequencies. Table 1 lists the master clock frequency, passband edge, -3 dB point, and stopband edge for typical digital audio frequencies. An expanded view of the passband showing less than 0.001 dB passband ripple appears in Figure 3 while the transition band is expanded in Figure 4.

## 2 PERFORMANCE

To test the A/D converter, the analog input of a CDB5328 evaluation board[6] is driven with a signal generator having distortion lower than the A/D converter's noise floor. Any distortion produced from such a setup is assumed to be from the A/D converter[7]. For the FFT tests produced in this paper, the analog input is either a Krohn-Hite Model 4400A or a Brüel & Kjær Type 1051. The data is collected for 1024 consecutive samples. The FFT expects the sample set to be periodic; therefore, if the samples at each end of the sample set do not align exactly, the FFT will produce distortion products that don't exist in the analog input. If the A/D converter were synchronized to the analog input, the end points could be aligned, but to align to the 18-bit level is very difficult. Since the analog input is not synchronized to the A/D converter, the time-domain samples are windowed to avoid discontinuities at the end points. Windowing drives the end points to zero making the first point and last point is the sample set equal. The window is a minimum 5-term which widens the fundamental and harmonics, but doesn't affect the specifications being tested such as S/N+D and dynamic range[8]. Since the noise is uncorrelated, sample sets of points can be averaged to produce a plot in which the noise shape and low level harmonics are distinguishable. The noise spreads itself equally among the frequency bins while the fundamental, harmonics, and tones present, if any, remain unchanged. The data for this paper was gathered with a personal computer which also calculates the FFT[9].

### 2.1 CS5328 Results

A plot of 100 sample sets averaged, using the previously mentioned setup with an analog input at full scale, appears in Figure 5. A full-scale input is not the optimum test for digital audio since any excursions above full scale cause clipping and large distortions. Digital audio equipment usually defines -10 dB as a maximum signal level to guardband against clipping. A signal 10 dB below full scale would be a better test of an A/D converter for this environment. As can be seen from Figure 6, a -10 dB signal shows slightly better performance than the full scale signal and the harmonics are practically below the noise floor. In Figure 7 the input signal is 80 dB down from full scale and is considered a more difficult test of A/D converter performance[10]. On-chip dither minimizes tones that are normally associated with delta-sigma A/D converters. Figure 8 plots input signal level versus signal-to-(noise+distortion) for a 1, 10, and 20 kHz input signal. This plot illustrates the CS5328's lack of significant distortion for low signal levels over the entire audio band.

## 2.2 19-Bit Monaural Mode

The hardware illustrated in Figure 9 ties the two analog inputs together and adds the two 18-bit outputs, generating a 19-bit number. Utilizing the CDB5328 evaluation board, the serial data for each channel is shifted into the serial-to-parallel converter during the first 18 serial clocks after L/R changes state and is then latched on the parallel output. The serial-to-parallel converter has a separate shift register and latch so the parallel output is valid until the next parallel latch update. On the evaluation board, the left channel data is latched 14 serial clocks before  $L/\bar{R}$  falls and the adder circuitry latches the left channel on the falling edge of  $L/\bar{R}$ . The right channel is latched on the evaluation board 14 serial clocks before  $L/\bar{R}$  rises. The two 18-bit numbers propagate through the adder during the latter 14 serial clocks of the  $L/\bar{R}$  low time and the 19-bit result is latched when  $L/\bar{R}$  rises.

The FFT plot in Figure 10 shows an improvement of approximately 3 dB using summed channels over the single channel approach. The extra bit generates a 6 dB improvement since the signal level is doubled, but the noise from the second channel invokes a 3 dB penalty. Figure 11 illustrates a 19-bit FFT with the analog input down 60 dB. Notice the dynamic range for the 19-bit mono mode is 100 dB over the 0-20 kHz audio bandwidth.

## 3 TIMING IN AUDIO ENVIRONMENTS

In a typical audio environment such as CD, DAT, or digital audio workstations, the traditional analog front end consists of an 11th-order Chebyshev anti-aliasing filter[11], followed by a sample-and-hold (S/H), and completed by an A/D converter for each channel as shown in Figure 12a. The timing section is required to synchronize the S/H, A/D converter, output multiplexer, and digital signal processing system. If oversampling is utilized, the diagram would look more like Figure 12b in which oversampling by two decreases the anti-alias filter requirements to a 7th-order Butterworth[11]. This anti-aliasing filter provides better group delay characteristics than the traditional approach. In 2X oversampling the A/D converter and S/H must be capable of operating twice as fast as the traditional approach, and the timing section has to accommodate the decimation filter between the A/D converter and the system. Figure 12c shows the analog front end using the CS5328 that oversamples the analog input by 64 generating a sample frequency,  $F_s$ , of  $64 \times \text{OWR}$  (output word rate). The CS5328 requires frequencies of  $128 \times \text{OWR}$  for the master clock,  $2 \times \text{OWR}$  for the serial data clock, and  $\text{OWR}$  for the  $L/\bar{R}$  signal indicating the channel: left or right. The anti-aliasing filter requirements are minimized to a single pole passive filter and the group delay characteristics for this approach provide a flat delay over the entire passband. The high frequency clocks required are usually available for other system functions and can be derived from a 74HC590 synchronous counter.

### 3.1 Philips I<sup>2</sup>S Bus

The "inter-IC sound" bus is a digital audio interface as defined by Philips[12]. The I<sup>2</sup>S interface uses word select,  $WS$ , (inverted  $L/\bar{R}$ ) to indicate both the channel and start of data. The data is output on the falling edge of SCK one SCK cycle after  $WS$  changes state. In the configuration illustrated in Figure 13, the 74HC590 counter is considered the master since it provides the word select and serial data clocks. The data output by the CS5328 must be delayed one SCLK cycle and is considered 32

bits in length with the receiving device ignoring unused bits as defined by the interface specifications.

### 3.2 Sony Digital Interface

Both the CX23033 and CXD1211 from Sony Corp. are digital transmitting chips designed to send data in a format similar to the AES/EBU specifications[13]. The CS5328 interface for these chips would be straightforward if the A/D converter was only 16 bits because both interface ICs provide a 16-bit MSB-first format. Figure 14 illustrates the circuitry needed to connect the CS5326, a 16-bit A/D converter, to the Sony chips. Since the CS5328 outputs 18 bits, the 24-bit format of both interface chips must be used, and that format only accepts data LSB first. If the interface chips allowed the specification of the MSB/LSB-first option separate from the 16-bit/24-bit option, the interface would be greatly simplified. Another feature of the interface chips is that the data must be right justified in the channel, whereas the data output from the CS5328 is left justified. Using the 16-bit format as an example, the 16 bits *preceding* LRCK ( $L/\bar{R}$ ) changing state are latched for right-justified data, whereas the 16 bits *following* LRCK changing state are latched for left-justified data. Figure 15 illustrates a method of converting from MSB-first to LSB-first using three cascaded 74HC299 shift registers oscillating between channels. When the right channel is shifting into the shift registers from the A/D converter, the left channel is shifting out of the shift registers to the digital interface chip and vice versa. LRCK for the CXD1211 has the same polarity as the CS5328, high for the left channel and low for the right channel, whereas LRCK in the CX23033 has the opposite polarity. Figure 16 illustrates the flow of serial data for each channel. While the CS5328 is clocking left-channel data into the 24-bit shift register via pin 'A', the shift register is clocking the previous right-channel data out of the  $Q_H$  pin and through a multiplexer into the interface chip. In Figure 16b the shift register's shifting direction is reversed and still contains the left-channel data. When the CS5328 starts shifting right-channel data into the shift register via pin 'H', the left-channel data contained in the shift register is clocked out of the  $Q_A$  pin and through the multiplexer into the interface chip. The multiplexer is needed to select the appropriate output of the 24-bit shift register to input to the interface chip, whereas the two inputs to the shift register may be tied directly together. The shift register clocks are disabled for eight serial clock cycles since only 24 bits of the 32 bit-periods in a channel are stored. Since the CS5328 outputs zeros after the 18 data bits, the shift register stores six zeros. In the timing diagram shown in Figure 17, the 'z's reflect the stored zeros. All combinational logic can be programmed into a PAL for compactness. To configure the interface chips for the 24-bit format, MSBF is set to zero for the CXD1211, whereas the CX23033 is used in operation mode 1 or, if a microcontroller is present, mode 3 with control register bits D7 and D6 both set to one.

## 4 INTERFACING TO DIGITAL SIGNAL PROCESSORS

Digital signal processors are used extensively in digital audio environments[14]. Although the digital signal processors, DSPs, discussed below are not an exhaustive set of DSPs capable of handling greater than 16 bits, they do illustrate the circuitry needed to interface to common serial ports.



#### **4.1 Motorola DSP56000**

The interface for the DSP56000 is straightforward as shown in Figure 18 with the timing diagram appearing in Figure 19. The counter needed for the various timing signals on the CS5328 provides other divided outputs that can be used by the DSP56000. The counter output previous to  $L/\bar{R}$ , FSYNC, is twice the frequency of  $L/\bar{R}$  and can be used to indicate the beginning of a word. This output will rise concurrently with  $L/\bar{R}$  changing state; however, FSYNC will fall after the 16th data bit is output. This is not a concern since the DSP56000 only uses FSYNC to start a serial data transmission and stops transmission when the specified number of bits are received. The DSP56000's serial port is configured to receive 24 bits ( $WL1, WL0 = 1,1$ ), normal operation ( $MOD = 0$ ), continuous clock ( $GCK = 0$ ), and word-length frame sync ( $FSL1 = 0$ ). If the transmit and receive ports are synchronous ( $SYN = 1$ ),  $L/\bar{R}$  can be used as a serial port flag indicating the channel. Section 5 has more information on the serial port flag.

#### **4.2 Texas Instruments TMS320C30**

The TMS320C30 has an interface similar to the DSP56000, with the exception of serial port flags. Figure 20 shows the interface diagram and Figure 21 illustrates the timing. If  $L/\bar{R}$  must be known to the DSP, one of the alternate methods described in Section 5 must be employed. The interface diverges from previous TI DSPs but has become more flexible in the process. For the serial port, the variable data rate mode with 24 or 32 bits is utilized. In this scenario, FSR goes active concurrently with the MSB of the data. (In fixed data rate mode, FSR goes active one CLKR cycle before data.) The DSP also inputs the programmed number of bits after FSR indicates the start of serial data transmission. The polarity of CLKR and FSR are programmable, thereby eliminating one inverter from the previous DSP interface.

#### **4.3 AT&T DSP32/DSP32C**

The DSP32 incorporates the data skewing technique utilized in the Philips I<sup>2</sup>S interface although there is no provision for stereo. The delay is one ICK (serial data clock) cycle on the ILD pin. ILD is a word sync as opposed to an WS signal which indicates the channel: left or right. The DSP32 accepts 32 bits, whereas the DSP32C can accept 24 or 32 bits, and both latch data on the rising edge of ICK. As with the two previous DSPs, ILD is only used to start serial data transmission. Figure 22 shows the connection diagram while Figure 23 illustrates the timing.

### **5 CHANNEL INDICATION**

Many systems do similar processing to both left and right channels; therefore, the DSP may not need to know which channel it is currently operating on. The channel indication,  $L/\bar{R}$ , may be connected to the A/D converter and digital out or D/A converter, thereby synchronizing the input and output, without connecting to the DSP. However, if the processing is different for each channel, the DSP must know which channel it is operating on. As this function is only needed at initialization, an interrupt line could be utilized, with the interrupt being disabled after synchronization is achieved. This method requires a dedicated interrupt line which is usually in short supply. Another common

method is to map  $L/\overline{R}$  to a memory location allowing the DSP to read that location while in the serial port service routine, thereby determining the channel. This method requires address decode logic and a high impedance latch to connect  $L/\overline{R}$  to the data bus. A third method connects  $L/\overline{R}$  to a general purpose input pin on the DSP if any exist.

If the serial port transmitting and receiving sections are synchronous on the DSP56000 from Motorola, two pins are liberated and can be configured as serial port flags. One of these flags can be utilized to capture the  $L/\overline{R}$  signal. As shown in Figure 19, the SC0 flag is latched concurrently with the MSB of the serial data. This flag can be tested on initialization to determine the channel.

Since all the DSP serial ports mentioned require a minimum of 24 bits, and the CS5328 is only 18 bits, 6 trailing bits are unused. If  $L/\overline{R}$  is appended to the serial data, the DSP could read the lower bits which identify the channel. The DSP could subsequently mask the lower bits or ignore them since they appear as a DC offset at a minimum of the 19-bit level. The circuit in Figure 24 appends  $L/\overline{R}$  to the serial data stream by ORing  $L/\overline{R}$  with the zeros output after the 18-bit serial word. The alternate circuit provides a single-chip-package implementation that multiplexes between SDATA and  $L/\overline{R}$ . Since the CS5328 outputs 18 bits, a flip-flop is needed to delay the rising edge of the QF (which rises after the 16th bit) until the 19th bit. A benefit produced by this configuration is that a larger-divide output of the 74HC590 can delay the  $L/\overline{R}$  "tag" information until later bit times making the DC offset less significant. Figure 24 shows two configurations for adding the  $L/\overline{R}$  tag to the data. In the "bit-19 tag" configuration, the  $L/\overline{R}$  tag immediately follows the data, whereas in the "bit-21 tag" configuration the tag doesn't appear until the 21st-bit position. Figure 25 illustrates timing for the "bit-21 tag" configuration. Notice that the left channel data is followed by two zeros, then twelve ones; therefore, the first "one" of the channel tag is in the 21st-bit position. If the DSP's serial port is configured for 32 bits, a "bit-25 tag" could be generated by using the QE output of the 74HC590 counter as the clock input to the flip-flop.

## 6 CONCLUSION

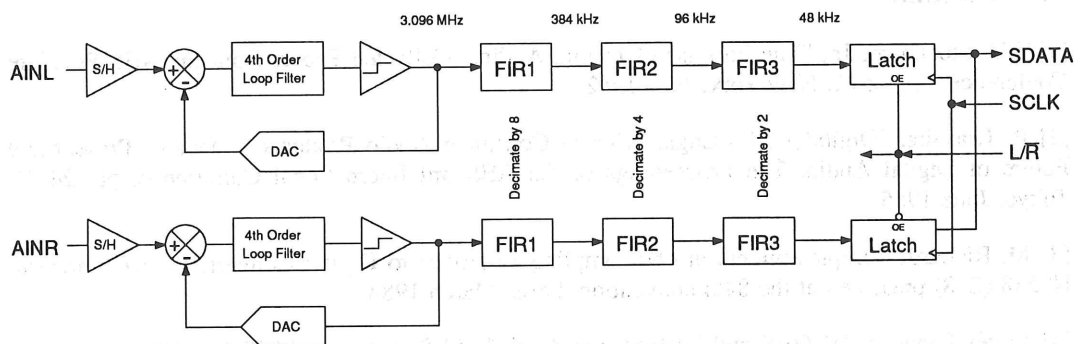
The architecture and performance of the CS5328 18-bit dual channel delta-sigma A/D converter were discussed along with detailed interface and timing diagrams to AES/EBU chips, the I<sup>2</sup>S bus, and a number of DSPs. A method of adding a channel identifier to the serial data stream was also explored.

Low input signal levels were shown not to degrade performance, and an example application using both 18-bit channels to generate a single 19-bit part was shown to improve the dynamic range to 100 dB over the audio band.

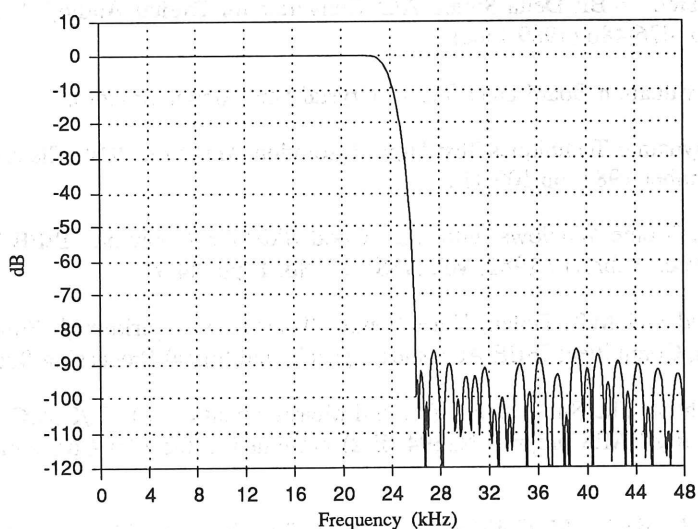


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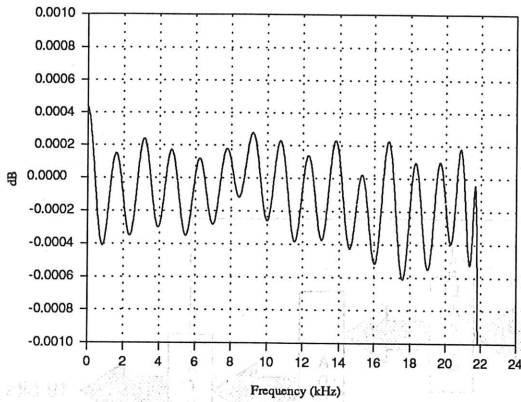
**Figure 1. CS5328 Block Diagram**



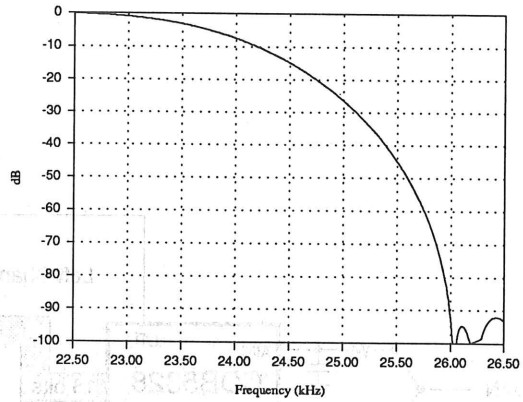
**Figure 2. Frequency Response**

Output Word Rate	CLKIN Frequency	Passband Edge	-3 dB Point	Stopband Edge
32 kHz	4.096 MHz	14.5 kHz	15.6 kHz	17.3 kHz
44.1 kHz	5.6448 MHz	20.0 kHz	21.6 kHz	23.9 kHz
48 kHz	6.144 MHz	21.8 kHz	23.5 kHz	26.0 kHz

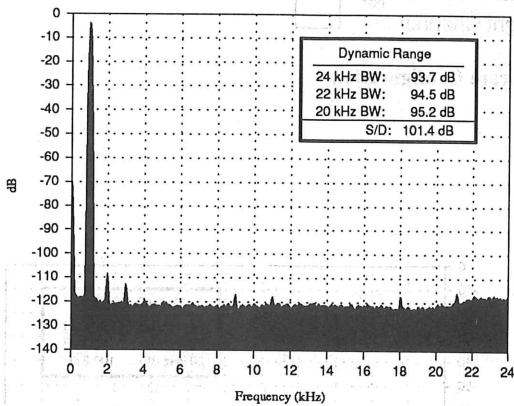
**Table 1. Audio Output Word Rates**



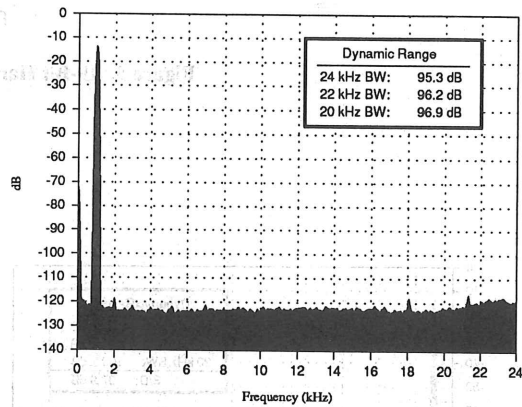
**Figure 3. CS5328 Passband Ripple**



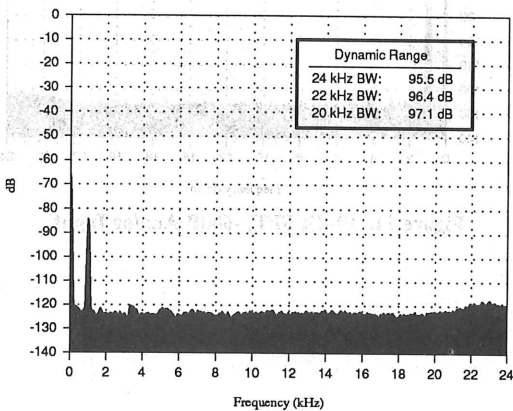
**Figure 4. CS5328 Transition Band**



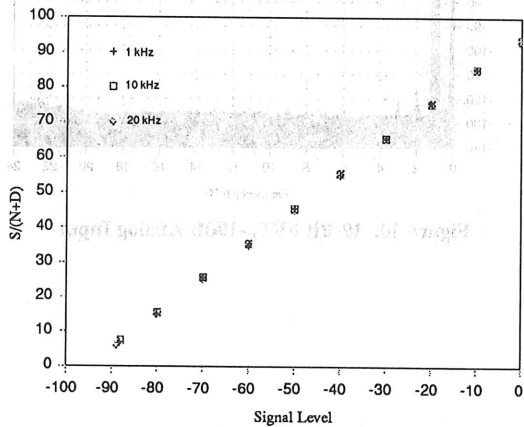
**Figure 5. CS5328, Full Scale Analog Input**



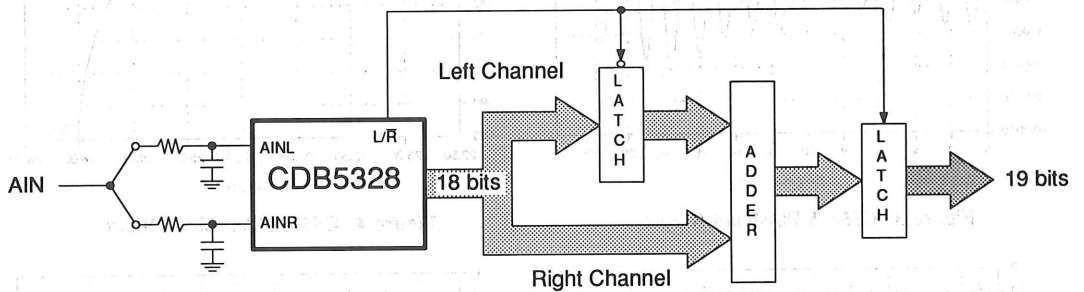
**Figure 6. CS5328, -10dB Analog Input**



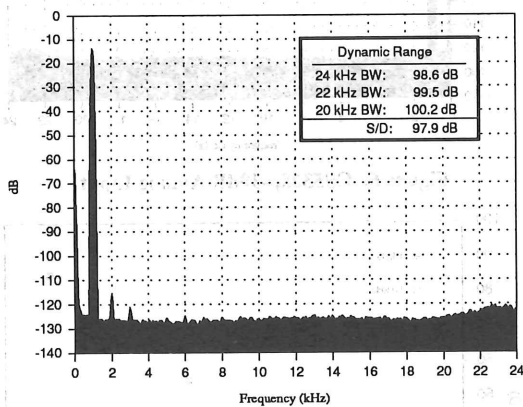
**Figure 7. CS5328, -80 dB Analog Input**



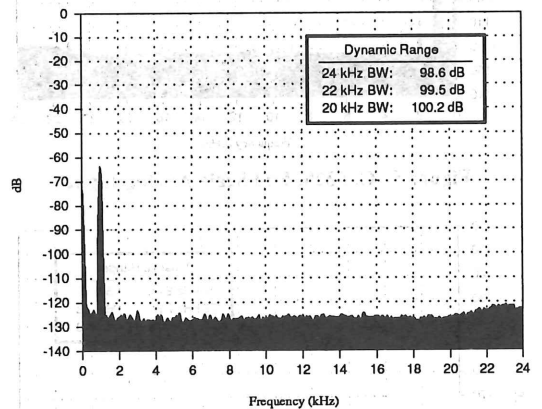
**Figure 8. Signal-to-Noise vs. Signal Level**



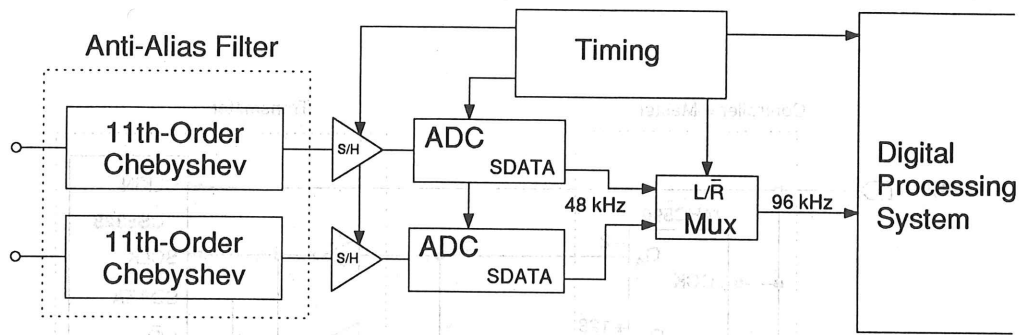
**Figure 9. 19-Bit Hardware Configuration**



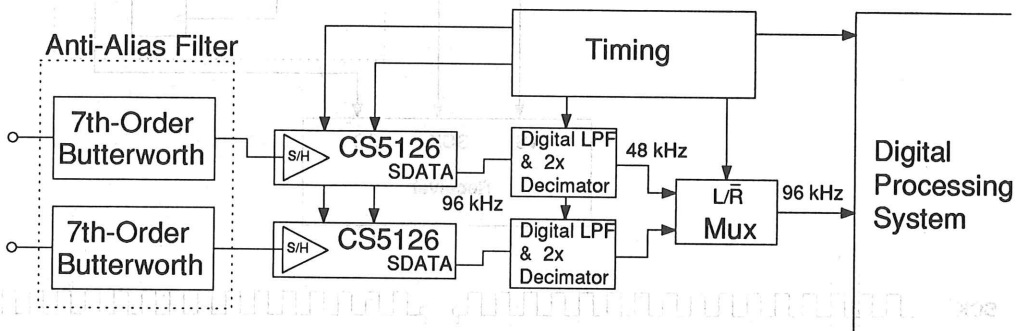
**Figure 10. 19-Bit FFT, -10dB Analog Input**



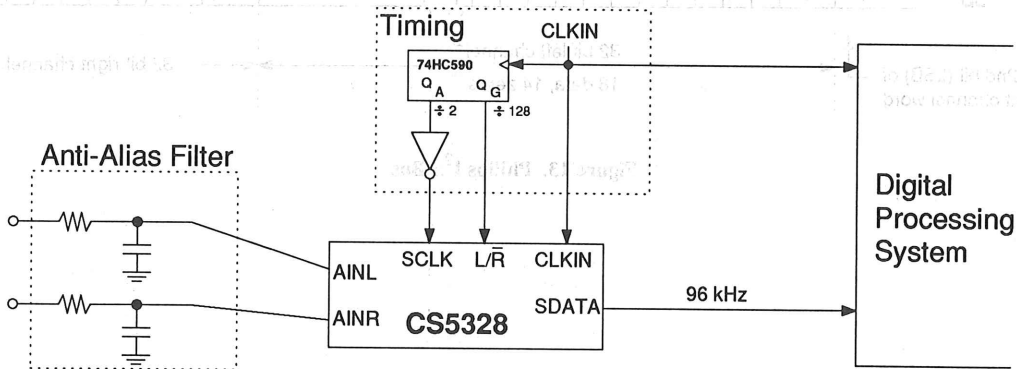
**Figure 11. 19-Bit FFT, -60dB Analog Input**



a. Traditional Approach

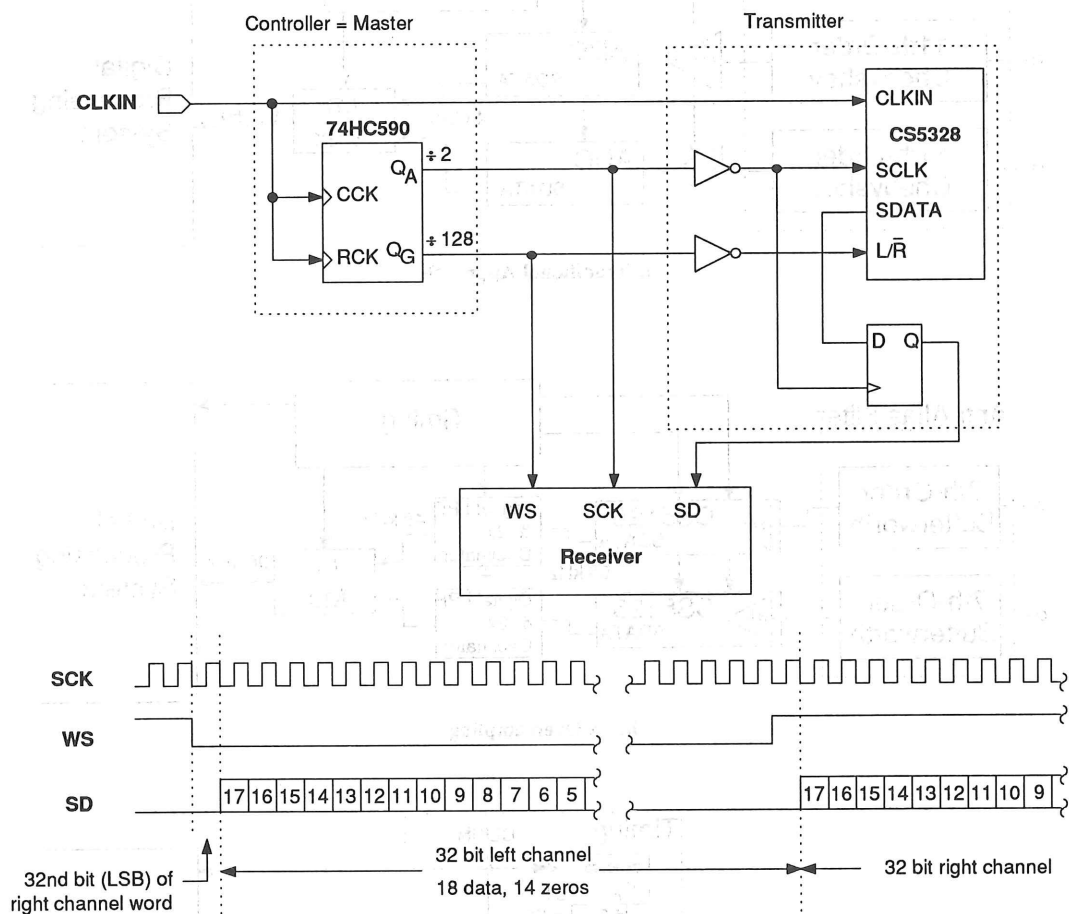


b. 2x Oversampling



c. 64x Oversampling

Figure 12. Analog Front End



**Figure 13. Philips I<sup>2</sup>S Bus**

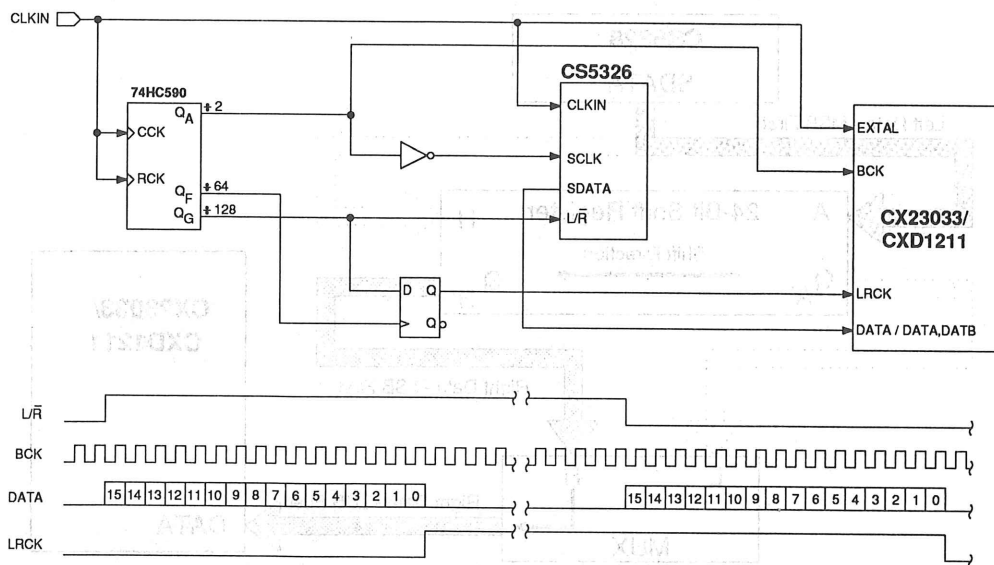


Figure 14. Sony Digital Interface, 16-bit Format

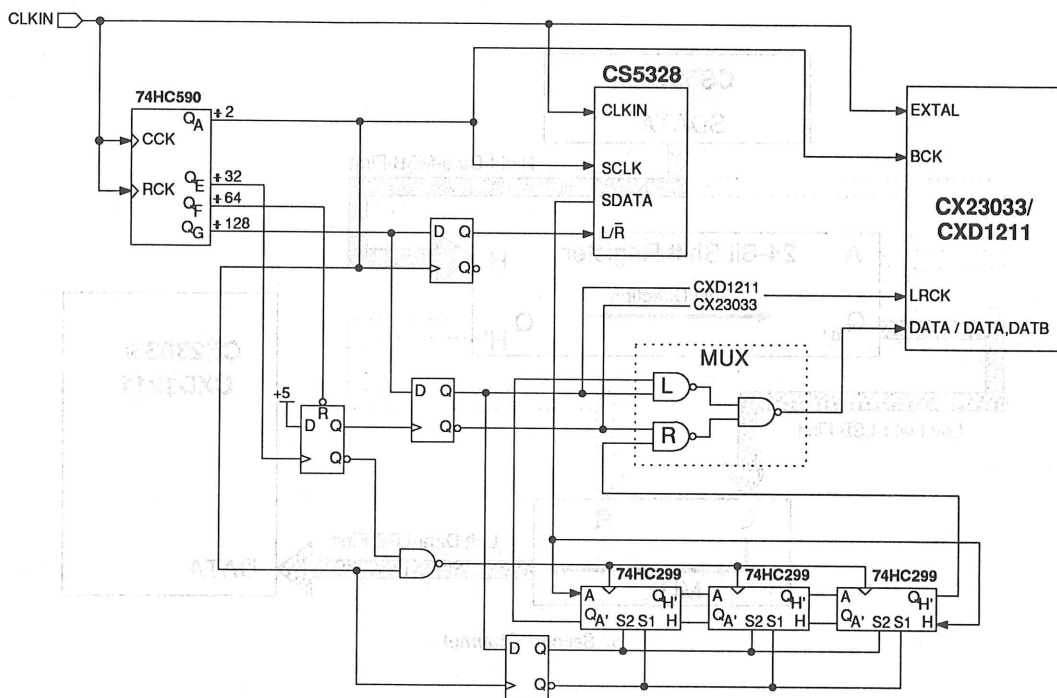
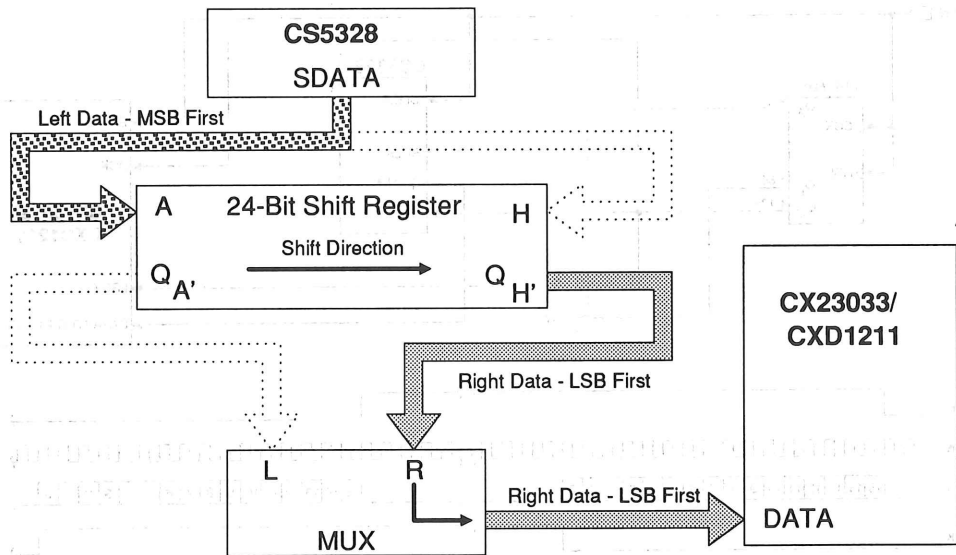
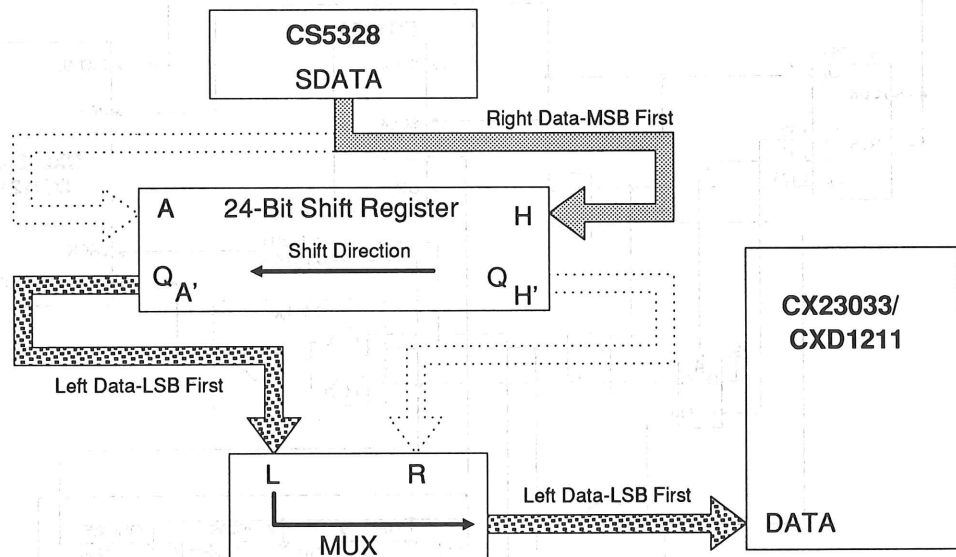


Figure 15. Sony Digital Interface, 24-Bit Format





**a. First Channel**



**b. Second Channel**

**Figure 16. Sony Interface Serial Data Flow**

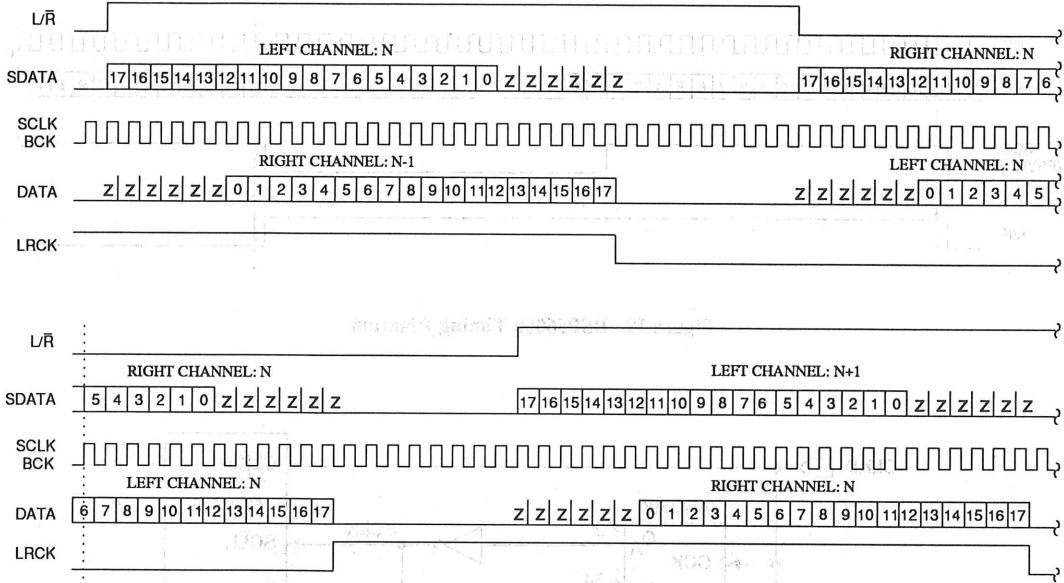


Figure 17. Sony Digital Interface Timing Diagram, 24-bit Format

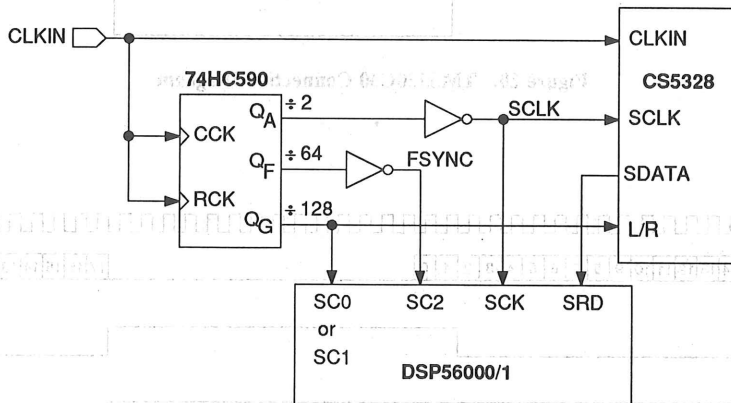
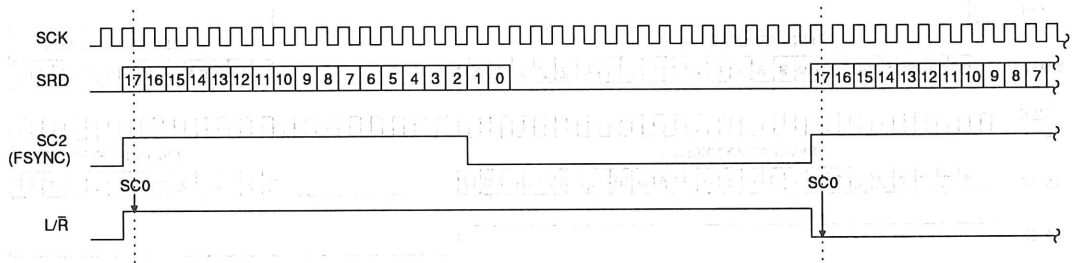
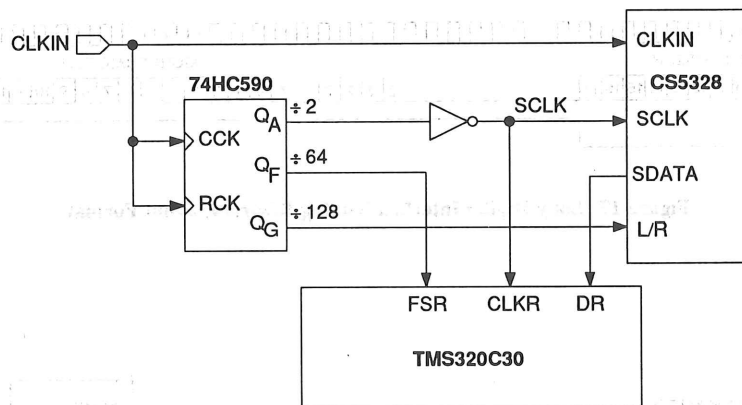


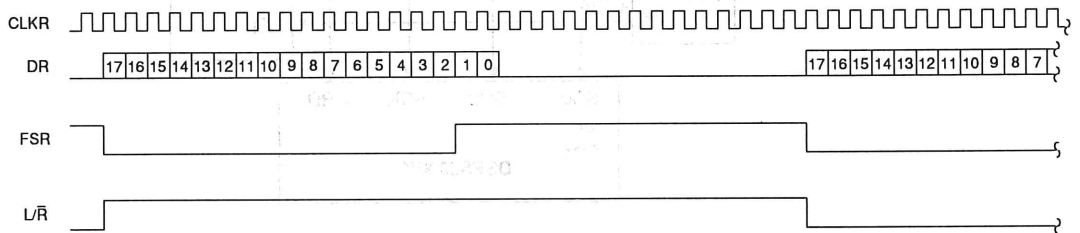
Figure 18. DSP56000 Connection Diagram



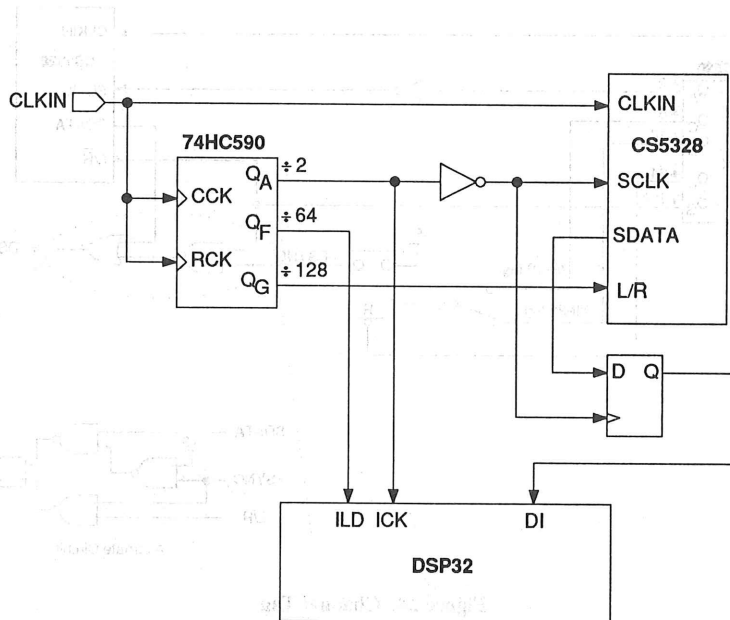
**Figure 19. DSP56000 Timing Diagram**



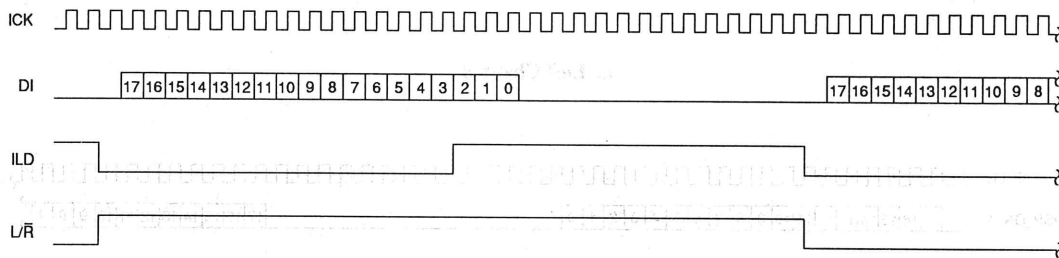
**Figure 20. TMS320C30 Connection Diagram**



**Figure 21. TMS320C30 Timing Diagram**



**Figure 22. DSP32 Connection Diagram**



**Figure 23. DSP32 Timing Diagram**

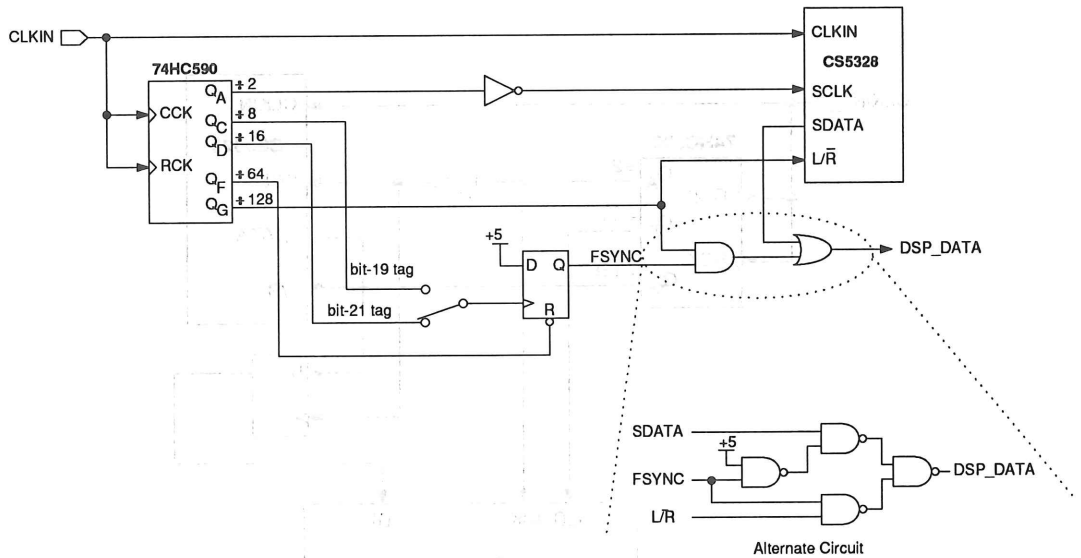
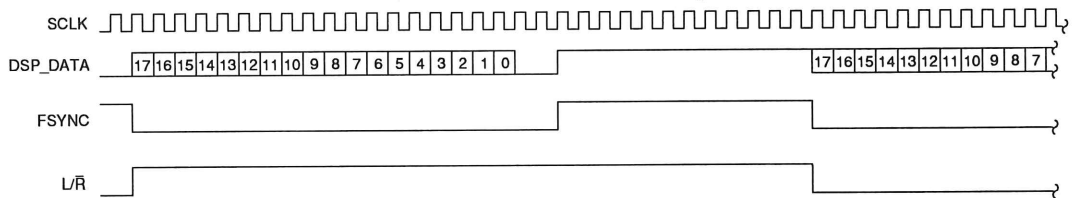
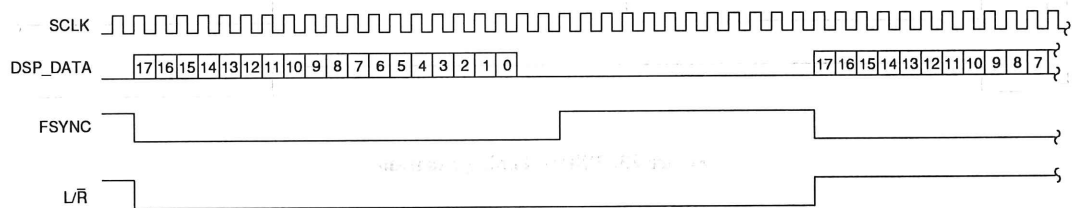


Figure 24. Channel Tag



a. Left Channel



b. Right Channel

Figure 25. Channel Tag Timing Diagram (bit-21 tag)

# A Stereo 16-Bit Delta-Sigma A/D Converter for Digital Audio

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A two channel 16-bit A/D converter employing oversampling techniques has been developed. The device contains two fourth order delta-sigma modulators with 1-bit outputs, each followed by a digital finite impulse response filter/decimator. The analog inputs are sampled at 3.072 MHz and the digital words are output at 48 kHz.

## 0. INTRODUCTION

The emergence of digital audio has increased the demand for high performance A/D converters. Delta-sigma conversion has been gaining recognition as having advantages over more classical audio band conversion techniques. In particular, it obviates the need for sample and hold amplifiers, eases the design of anti-aliasing filters, and is free of differential non-linearity errors that distort low level signals.

This paper discusses the development of a two channel 16-bit audio band delta-sigma converter featuring a high degree of integration and suitable for use in stereo digital audio applications. Section 1 gives an overview of the concepts pertaining to delta-sigma conversion. The device architecture and a functional partitioning strategy are presented in Section 2. Sections 3 and 4 discuss design of the two major functional blocks, and measured results are presented in Section 5.

## 1. DELTA-SIGMA CONVERSION

### 1.1 Quantization Noise

Analog to digital conversion is a process that necessarily introduces errors into a signal due to quantization. The difference between the output of

an otherwise perfect converter (or "quantizer") and that which might be expected of a converter with unlimited resolution can be modelled as an additive noise signal. The level of this "quantization noise" is reduced in converters of higher resolution with finer quantization levels, but nonetheless must remain non-zero. If the analog input is sufficiently large and/or if the input is sufficiently random, the spectrum of the quantization noise can be approximated as white [1] with its energy equally distributed between dc and  $f_s/2$ , where  $f_s$  is the sampling and conversion rate (it is assumed the signal is sampled before it is converted). The effective resolution of a converter can be increased by filtering the output and thereby reducing the level of the quantization noise. A commensurate reduction in the available signal bandwidth must be accepted as a consequence of the filtering, but may prove acceptable if the conversion rate is high. The sampling and conversion of a signal at a rate much higher than the signal frequency is a technique termed "oversampling". The "oversampling ratio" is the ratio of the actual sampling rate to the Nyquist rate (i.e., twice the highest signal frequency of interest).

This process is illustrated in Figure 1, where an analog sinusoid of frequency  $f_0$  is converted to a digital, quantized sinusoid at a rate  $f_s$  by a linear

pulse-code modulation (PCM) converter. The input spectrum is shown in Figure 1A, and Figure 1B shows the effects of the quantization process with the addition of white noise (this and following spectra repeat at multiples of  $f_s$ , of course, due to the discrete time nature of the sampled signal). Processing by a digital filter with a baseband cutoff frequency of  $f_b$  as illustrated in Figure 1D yields the output spectrum in Figure 1E. The baseband cutoff frequency  $f_b$  is presumed to be equal to the highest signal frequency of interest. The remaining quantization noise voltage level will be lower than the original level by a factor of  $\sqrt{f_s/2f_b}$  (the quantization noise *energy* is lowered directly by the oversampling ratio  $f_s/2f_b$ ).

The utility of this technique when applied to audio signals with a baseband frequency of

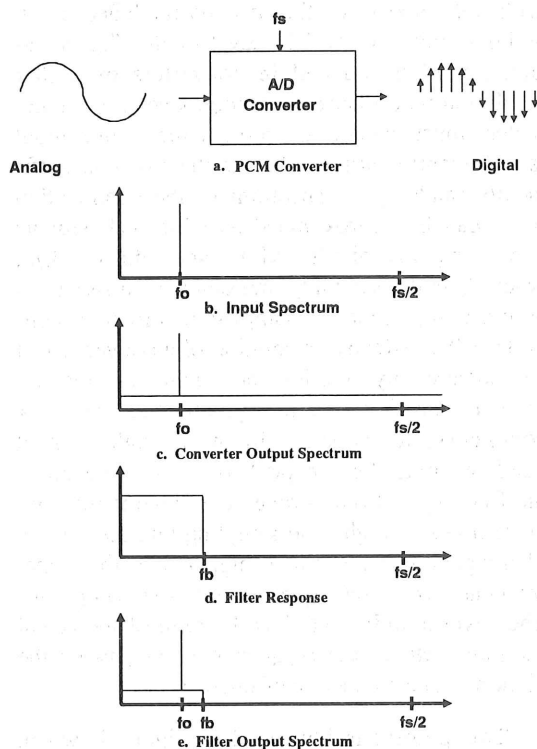


Figure 1. Increasing Resolution with Filtering

$f_b = 20\text{kHz}$  is questionable. To obtain the equivalent of 16-bit performance from, say, a 12-bit converter, the 12-bit quantization noise would have to be lowered by  $2^4=16$ . This would in turn require an oversampling ratio of  $f_s/2f_b = 256$ , or  $f_s \approx 10\text{MHz}$ .

Delta-sigma conversion is a technique that employs oversampling to obtain high resolution (low quantization noise) digital signals from low resolution (high quantization noise) quantizers. As will be shown below, the delta-sigma converter contrasts with the previous example in that the quantization noise *at the output* of the low resolution quantizer is not white, but rather frequency "shaped", such that noise in the baseband ( $f < f_b$ ) is suppressed at the expense of slightly higher out-of-band ( $f > f_b$ ) noise. The power of digital filtering can then be applied to the resultant spectrum to pass the signal (and the residual baseband quantization noise) while rejecting the out-of-band quantization noise.

The converter consists of a modulator and a digital filter. As can be seen in Figure 2, embedded in the modulator is the low resolution N-bit quantizer, around which frequency dependent feedback is applied by means of a N-bit DAC and an analog filter. The analog filter has a frequency response of  $H(f)$ . The analog input is

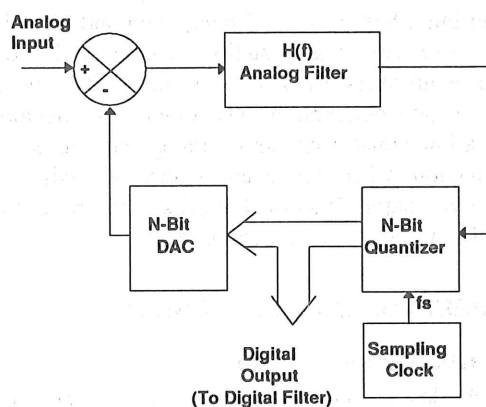


Figure 2. Delta-sigma modulator

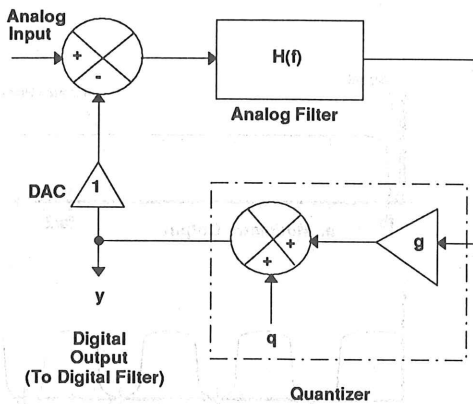


Figure 3. Linearized delta-sigma modulator

summed into the modulator loop at a point where, for frequencies with high loop gain, the output of the DAC will be substantially equal to the input. To the extent that the DAC faithfully reproduces the quantizer digital output, this signal, too, must be substantially representative of the analog input again, for frequencies with high loop gain.

## 1.2 Loop Analysis

The presence of the non-linear quantizer renders exact analysis of the loop difficult. A typical and useful approach is to linearize the quantizer by replacing it with a gain stage and a quantization noise source [2]. Again, the latter is only a contrivance to account for the difference between the quantized output and the amplified input. This is illustrated in Figure 3. The DAC has been replaced by a unity gain stage, as its function is irrelevant for analyzing the effects of quantization noise. Note, though, that non-idealities in the DAC can be the chief limitation to the modulator's performance [3].

The actual value of the gain  $g$  and the rms value of the quantization noise signal  $q$  need not be known to obtain an understanding of how the modulator shapes the quantization noise. It must be assumed, however, that successive values of the quantization error are uncorrelated — i.e., the quantization noise spectrum is white. The validity of this assumption is borne out empirically.

The modulator output signal  $y$  is a function of the analog input  $x$  and quantization noise  $q$ , as follows:

$$y = (x - y) H(f)g + q$$

$$y [1 + H(f)g] = xH(f)g + q$$

$$y = \frac{H(f)gx}{1 + H(f)g} + \frac{q}{1 + H(f)g}$$

If the loop gain  $H(f)g \gg 1$ , then

$$y \approx x + \frac{1}{H(f)g} q$$

That is, the output will be the sum of the input and the quantization noise spectrally shaped by the inverse of the analog filter frequency response.

A glance at the approximate expression for  $y$  may lend hope to the prospect of reducing quantization noise by increasing the value of  $H$  at all frequencies. However, the effective value of  $g$  would change to compensate such a maneuver. Reducing  $q$  by introducing a higher resolution quantizer would indeed offer improved performance. But the most effective method of achieving lower baseband quantization noise (for a given oversampling rate) is the selection of filter function  $H(f)$  that possesses high in-band gain and high out-of-band attenuation, thereby shaping the quantization noise spectrum advantageously. Note that the poles of the filter are zeros of the noise transfer function.

## 1.3 Integrator

A simple integrator has the desired spectral qualities for a filter. A cascade of two integrators would appear more attractive, and indeed such a "second order" filter more effectively shifts quantization noise to out-of-band frequencies than the "first order" filter. Extension to higher order filters is problematic, though, due to stability considerations. A second-order design requires the placement of a single zero in the filter response to obtain a well-behaved modulator.



Higher-order filters can also have zeros included as an aid to stability, but even so they are conditionally stable due to the high phase shift at baseband frequencies. Conditionally stable loops can become unstable if a frequency independent gain parameter in the loop is reduced. The effective quantizer gain  $g$  is such a parameter and is subject to change under varying operating conditions. As such, stability of modulators with third and higher order filters is at risk. Nevertheless, the attractiveness of higher order filters has led to a number of solutions to the stability problem [4],[5]. The device discussed in this paper utilizes a fourth-order filter. Stability will be discussed below.

Another approach that leads to performance similar to higher-order modulators without the attendant stability question has been reported [6]. This architecture has cascaded lower order modulators, with successive modulators measuring the residual in-band quantization noise of previous modulators. The various modulator outputs are digitally processed to lower overall in-band noise. However, accurately matched components and high gain integrators are necessary to achieve the desired performance.

#### 1.4 Filtering and Decimation

Once the quantization noise has been appropriately shaped, it remains the task of the digital filter to remove the out-of-band quantization noise. A straightforward approach of synthesizing a low pass filter with sufficient stop-band attenuation and acceptable pass-band response would prove inefficient. Instead, a strategy of staged filtering and decimation can be adopted to ease the computational burden [7]. Decimation is the process of sampling a discrete time signal at a rate lower than its own. The advantage of decimation is that signal processing after decimation can proceed at the lower rate. As a sampling process, though, decimation is subject to the ill effects of aliasing.

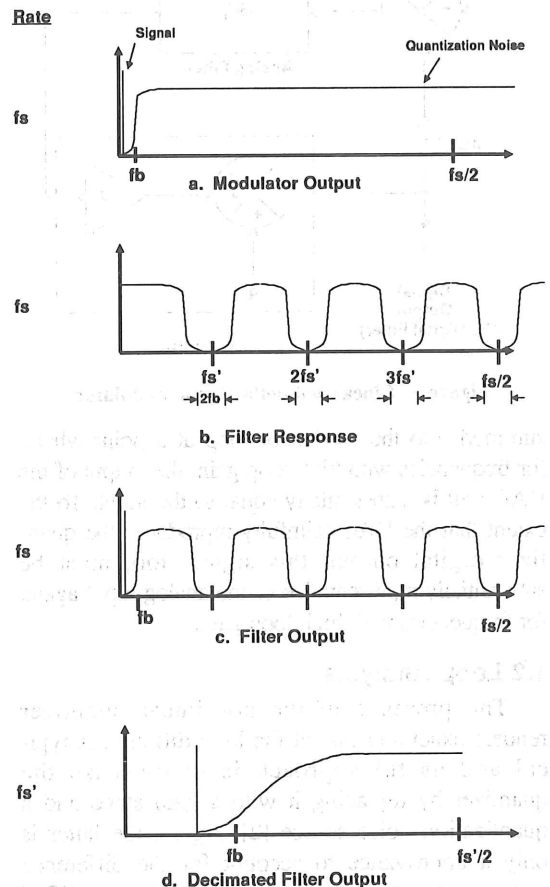


Figure 4. Filter Strategy

In this application, each stage of filtering need only reject signals that will be aliased into the baseband by the immediately subsequent decimation process, since later filter stages will reject signals aliased elsewhere. Figure 4 illustrates this approach. A signal with a spectrum characteristic of a modulator output signal is input to a filter at a rate  $f_s$ . The output of this filter is to be

decimated to a new rate  $f_s'$ , where  $f_s = Nf_s'$ , before being processed further. Aliasing will occur throughout the spectrum, but only components within  $\pm f_b$  of integer multiples of  $f_s'$  will get aliased into the baseband. A filter designed to have rejection only in these frequency "pockets" requires much less computation than one with rejection across the entire stop-band. As the sampling rate gets lower, of course, the pockets become proportionately wider and the filters become more complex. However, they can proceed with their computations at a more leisurely pace.

The final filter stage, operating at the slowest rate, can be a true low pass filter, eliminating the accumulated out-of-band quantization noise. In addition, it can "tweak" the frequency response of the pass-band if previous filter stages, the modulator, or even analog processing prior to the modulator have warped the response.

The need to reject the out-of-band quantization noise also represents a benefit. Namely, signals outside the baseband up to half the modulator sampling frequency do not get aliased by the modulator and are rejected by the digital filter. Indeed, spurious input signals approaching the sampling frequency do not get aliased into the baseband unless they are within  $\pm f_b$  of  $f_s$ , and are likewise rejected. This characteristic can greatly relax analog anti-aliasing requirements and, for some applications, stands as one of the leading benefits of delta-sigma conversion.

## 2. ARCHITECTURE

### 2.1 Overall Architecture

The device described in this paper contains two delta-sigma converters suitable for stereo digital audio applications. It is packaged in a 28 pin dual-in-line package with a standard 0.600 inch wide footprint. The cavity of the package is occupied by two silicon dice. One die contains the two modulators, a voltage reference (the value of which determines full scale signal level), clocking circuitry, and a small amount of digital

housekeeping circuitry. The second die contains the digital filter/decimators.

### 2.2 Reasons for Two Die

Partitioning of the system in such a fashion was motivated by the following considerations:

1) The complexity of the digital filter necessarily creates a large amount of electrical noise during normal operation. Placing this circuitry on a silicon substrate separate from the modulators eases the task of preventing this noise from interfering with the modulators' analog signal processing.

2) The great majority of the silicon area is occupied by the digital filter/decimators, and the manufacturing cost is dominated by this circuitry. Shrinking of the geometries comprising this circuitry as the product matures can lead to cost reductions without affecting performance. Shrinking of analog circuitry is risky and difficult; hence, the advantage of removing this circuitry from the more cost-sensitive digital die.

3) With separate die, different processes can be used to fabricate the analog and digital portions on the converters.

Regarding the last item, the digital die is manufactured using a standard 5V, 2 micron double-metal digital CMOS process. A 10V process was chosen for the analog die to allow more headroom for the analog signals. CMOS was chosen to support the switched capacitor design discussed in the next section. The selected process has 3 micron line widths, double polysilicon layers for capacitors, and a single metal layer.

### 2.3 Shared Functions

To a large extent, the two channels function independently. However, some circuit blocks are shared. On the analog die, all clocking is common between the two channels to facilitate simultaneous sampling of the left and right channel signals. Additionally, a single voltage reference

circuit is utilized by both channels. The voltage reference employs both lateral and vertical bipolar *npn* transistors (both of which are useful parasitics in this process) in a bandgap configuration. Its output is connected to a pin so that it can be capacitively bypassed to reduce crosstalk between the two channels. This capacitor and two simple RC anti-alias filters are all the external elements required of the device other than standard power supply decoupling elements.

The two digital filter/decimators also have common clocking. The various filter coefficients are stored in a single ROM which is accessed by both right and left channels.

### **3. MODULATOR**

#### **3.1 Major Characteristics**

The major characteristics that need be determined in the design of a delta-sigma modulator are filter technology, oversampling ratio, quantizer resolution, and filter order.

#### **3.2 Discrete Time Implementation**

Although continuous time filters can be employed in the implementation of a delta-sigma modulator (sampling occurs at the quantizer only), three considerations dictated the choice of sampled data filters for use in the product. First is the ease with which sampled data filters can be integrated in comparison to continuous time filters. Second is that continuous time filters are sensitive to timing errors in the feedback of the modulator's DAC signal [3], whereas sampled data filters are not. Third, with proper design care sampled data circuits can provide greater isolation between channels in a stereo application since signal currents are transient. They can be made quite small at the sampling instances and are of no consequence at other times (both technologies are subject to capacitive crosstalk). Thus, sampled data switched capacitor technology was chosen for the design of the modulator.

#### **3.3 Oversampling Ratio**

The oversampling ratio is limited by the achievable settling time of analog components as well as the maximum computation rate of the digital filter. It is also preferable that the oversampling ratio be a factor of  $2^N$  to ease applications. With a standard baseband of 24kHz, the oversampling ratio of 64 was chosen for a sampling rate of 3.072MHz. In a switched capacitor network each cycle is divided into two phases. With design margin, all modulator circuit blocks were designed to settle in 100ns to 0.1%.

#### **3.4 1-bit Quantizer**

As was mentioned in Section 1, higher resolution quantizers embedded in the modulator loop yield lower levels of in-band quantization noise. However, a 1-bit quantizer (i.e., a comparator) is simple to implement and minimizes the number of connections between the modulators and their digital filters. More importantly, a very attractive attribute of the use of a 1-bit quantizer is that errors in the 1-bit feedback DAC are not sources of distortion and/or excess noise, but only gain and offset errors [8]. Therefore, no precision components are necessary. Further, a one bit output simplifies the design of the first (and highest speed) digital filter stage.

#### **3.5 Modulator Filter Order**

The selection of a 1-bit quantizer operating at an oversampling rate of 64 requires at least a third order modulator filter to obtain 16-bit performance at the digital filter output. The addition of other noise sources (e.g., quantization effects in the digital filter) eliminated the candidacy of a third order filter. A fourth order modulator filter comprised of four cascaded integrators would provide sufficient rejection of baseband quantization noise. However, the modulator's baseband quantization noise can be rendered insignificant by optimization of a fourth order filter, as follows.

In Section 1 it was noted that the poles of the modulator filter are the zeros of the quantization noise transfer function. A filter with four cascaded integrators results in a noise transfer function with four zeros at dc. Lee and Sodini [9] found that spreading these zeros by application of local feedback around the integrators was effective in lowering the total baseband quantization noise output by the modulator. Optimal placement of all four zeros (two conjugate pairs) results in an 11dB improvement in baseband quantization noise rejection. Optimal placement of a single conjugate pair with two zeros left at dc results in a 10dB improvement.

Implementation of the two-conjugate-pair filter requires feedback to the input summing junction. This requirement has associated undesirable consequences (PSRR degradation, for example) and the two pair configuration offers little additional noise shaping improvement above the single pair. So, the single conjugate pair configuration was adopted.

### 3.6 Modulator Design

Figure 5 is a block diagram of the modulator. Coefficient  $b$  is fed back around the third and fourth integrators to form the conjugate pair of poles in the filter transfer function. The analog input is represented by  $x$ , and the single bit digital output is  $y$  (which is inverted and summed with  $x$  in analog form). The feedforward coefficients  $a_1$  through  $a_4$  are necessary (although not sufficient) for stable operation. The value of one coefficient is arbitrary. The value of the other three coefficients determine the location of filter zeros, but the effect of these on modulator operation is not easily predictable. Higher ratios of  $a_1$  to  $a_4$  lead to more stable, noisier operation.

### 3.7 Stability Considerations

As was mentioned in Section 1, low values of the "effective gain" of the quantizer (in this case comparator)  $g$  can lead to instability. Since the output levels of the comparator are fixed, and since in an unstable mode the integrator output levels can be expected to grow, any linearization

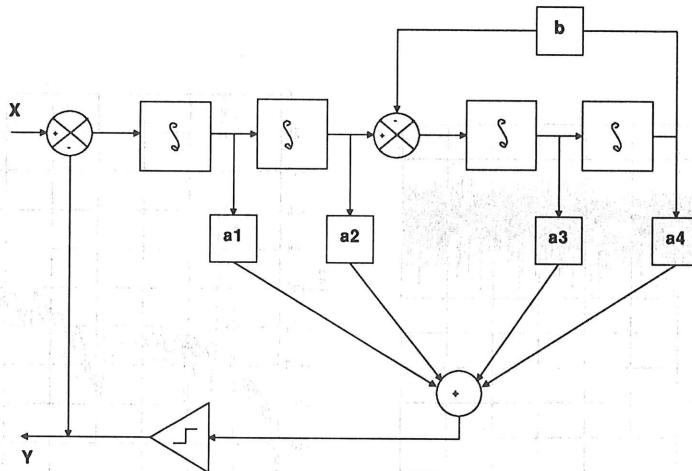


Figure 5. Modulator Block Diagram

criterion for evaluating  $g$  should lead to an ever decreasing value. Similarly, it would not be unreasonable to expect that large values of the input would lead to small effective values of  $g$ , initiating instability.

Simulation and laboratory experience has shown that the modulators do indeed exhibit this behavior. Fortunately, stable regions of operation also exist. The strategy adopted in the design of these modulators is to allow normal operation only well within the stable state space. Circuitry is provided to detect excessively high integrator levels as an indication of unstable operation. If such levels are detected, the integrators are reset to a stable condition. In practice, the reset circuitry is never utilized except at power-up (whereupon the modulator filter may or may not be in a stable state) or during periods when the input is excessively high. "Excessively high" means much higher than full scale, in which case the converter's digital output would be clipped and occasional modulator resets would be of no consequence. As the input returns to a level near full scale, the latest reset event leaves the modulator in a stable state.

### 3.8 Measured Spectra

Figure 6 shows a typical spectrum of a simulated modulator including a sinusoid input signal (very close to dc on the linear frequency scale) plus the quantization noise from dc to  $f_s/2$ . An expansion of the low frequency portion of this figure is shown in Figure 7. Here, the effect of the conjugate pair of quantization noise zeros is evident, as well as that of the pair at dc.

## 4. FILTER/DECIMATOR

### 4.1 Overall Architecture

Linear-phase finite-impulse-response (FIR) filters are used for decimation. The 1-bit, 3.072MHz outputs of the modulators are decimated in steps of 8, 4, and 2 to yield 16-bit, 48kHz results. A functional block diagram of the digital die appears in Figure 8. Timing, control, and coefficient ROMs (FIR2 and FIR3) are shared by the two channels. Left and right channel data paths operate independently. FIR2 and FIR3 use a per-channel multiplier/accumulator.

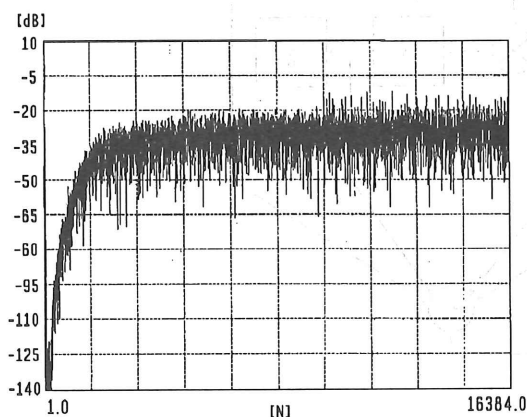


Figure 6. Simulated modulator output spectrum

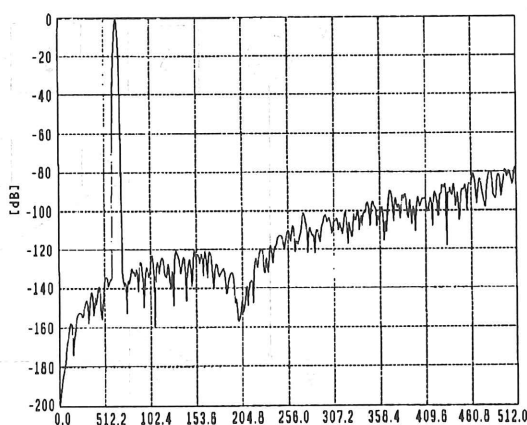


Figure 7. Expanded simulated modulator output spectrum

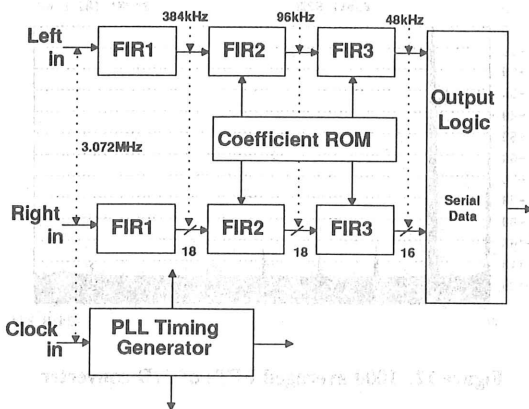


Figure 8. Filter/decimator block diagram

## 4.2 Decimation

The decimation strategy includes two stages, FIR1 and FIR2, whose primary responsibility is attenuation of quantization noise prior to decimation and aliasing. As Figure 6 shows, modulator out-of-band quantization noise spectral density is very high. FIR1 and FIR2 use 17 and 18-bit coefficients to attenuate this noise — and out-of-band

input signals — into the converter noise floor. Filter orders are 27 and 30, respectively. Data is processed with 18-bit fixed point arithmetic.

## 4.3 Passband Shaping

FIR3 performs passband shaping and out-of-band signal attenuation. Passband frequency response errors introduced by the modulator, FIR1, and FIR2 are corrected by FIR3. Overall filter passband ripple is thus reduced to  $\pm 0.001\text{dB}$  from dc to 22kHz. The passband compensation function prevents the use of a half-band filter for FIR3. The filter has 124 non-zero, 18-bit coefficients. Again, data is processed with 18-bit fixed point arithmetic. Data is truncated to 16 bits at the output, and this operation is the major noise contributor in the system.

## 4.4 Antialiasing Filtering

As indicated in Section 1, FIR1, FIR2, and FIR3 also combine to provide antialiasing filtering. All analog input frequencies from 26kHz to 3046kHz are attenuated by at least 86dB. The magnitude response of the complete modulator/decimator from dc to 48kHz is shown in Figures 9 and 10. Phase response is precisely linear.

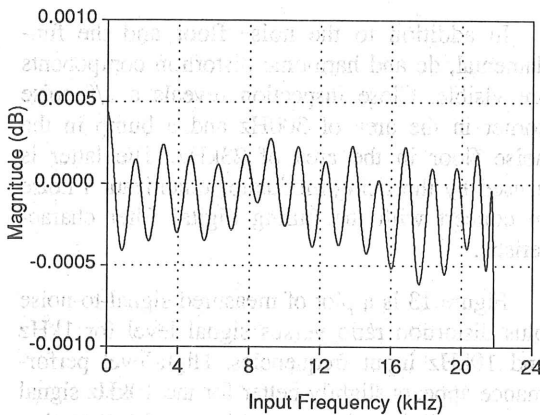


Figure 9. Filter passband ripple

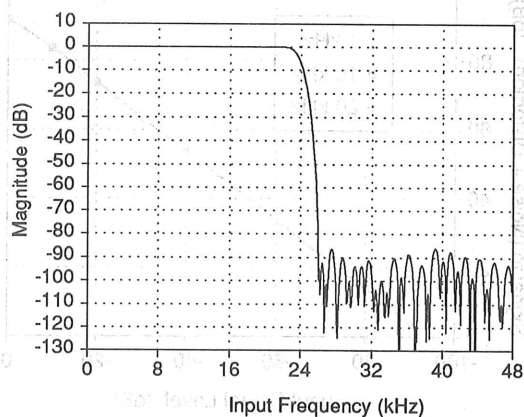


Figure 10. Filter frequency response



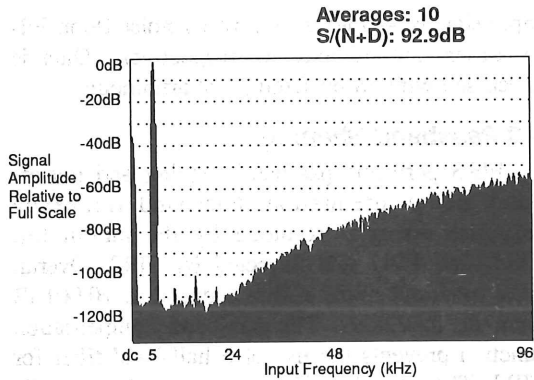


Figure 11. Partial 16K point FFT of modulator output

## 5. RESULTS

### 5.1 Modulator Output

Testing of the key specification parameters was performed with the aid of Fast Fourier Transform (FFT) routines. Figure 11, for instance, shows the low frequency portion of an FFT performed on a modulator's single bit output. The quantization noise shaping is evident in this plot. Absent, however, is the null due to the conjugate pair noise shaping zeros that is visible in Figure 6. The quantization noise of the modulator is masked

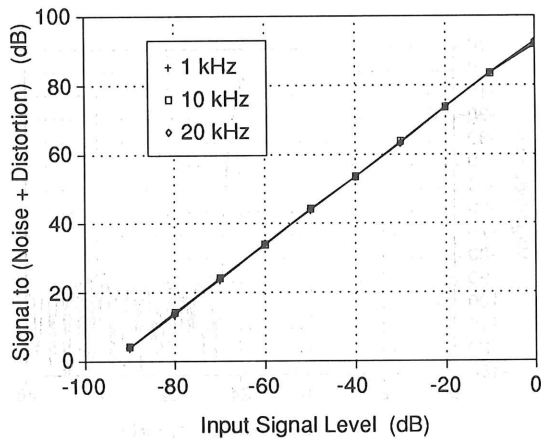


Figure 13. Signal-to-noise ratio versus signal level

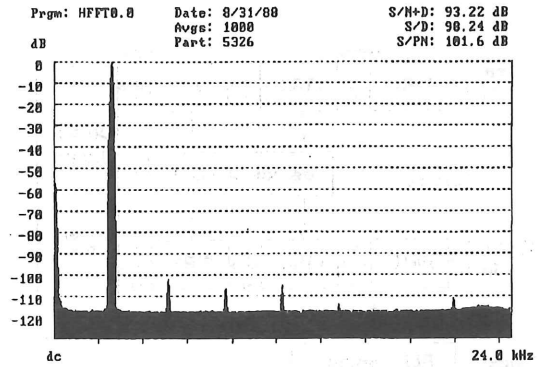


Figure 12. 1000 averaged FFTs of A/D converter

by the device's more classical noise mechanisms. Quantization noise can only be seen rising out of the thermal noise floor at frequencies above the audio band.

### 5.2 Digital Filter Output

Figure 12 shows a plot of the result of an average of one thousand FFT's performed on the 16-bit words output by the digital filter. Averaging of numerous FFT's serves only to cosmetically smooth the noise floor and does not change the ratio of the signal to noise level. The width of the fundamental is due to the application of a low side-lobe window to the data stream [10].

In addition to the noise floor and the fundamental, dc and harmonic distortion components are visible. Close inspection reveals a  $1/f$  noise corner in the area of 300Hz and a bump in the noise floor in the area of 23kHz. The latter is caused by the rising modulator quantization noise in concert with the falling digital filter characteristic.

Figure 13 is a plot of measured signal-to-noise plus distortion ratio versus signal level for 1kHz and 10kHz input frequencies. High-level performance appears slightly better for the 10kHz signal because all but the second-harmonic distortion components fall outside the baseband.

### 5.3 Specifications

Table 1 lists the key specifications and their measured values.

Oversampling ratio	64X
Signal-to-noise plus distortion	92 dB
Dynamic range	94 dB
Filter passband ripple	<0.001 dB
Filter stop-band rejection	>86 dB
Calibration error	5 LSB
Chanel-to-channel crosstalk	-103 dB at 20 kHz
Channel-to-channel gain mismatch	0.04 dB
Gain temperature coefficient	80 ppm/°C
PSRR	50 dB
Power dissipation	450 mW

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## •Notes•

The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's.

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**Abstract**

Sampling clock jitter is inevitable in a digital studio environment. This paper discusses the audio effects of clock jitter on an Analog-to-Digital Converter (ADC). The clock jitter sensitivity of a conventional Nyquist sampling ADC is compared and contrasted to that of a 3 MHz 64X oversampling delta sigma ADC.

**0 INTRODUCTION**

The increasing density of digital equipment in studios has prompted much discussion on synchronization of multiple items of digital audio equipment. The distribution of a master clock, for example via the AES/EBU interface, will inevitably add jitter to the clock. Each item of digital audio equipment that contains an analog-to-digital converter (ADC), or a digital-to-analog converter (DAC), will require a stable sampling clock, which is frequency locked to the distributed master clock. This paper investigates the amount and nature of jitter that an ADC can tolerate.

Included in the paper are a theoretical analysis of the effect of clock jitter on the sampling process, the results of a computer simulation, and measured results taken from actual ADC's with deliberately jittered clocks. Different types and amplitudes of jitter are investigated. In addition, the jitter sensitivity of a 76.8 kHz sampling ADC is compared and contrasted to that of a 3 MHz oversampling delta sigma ADC.

## 1 Clock Jitter Theory

The effects on ADC performance of jittering the sampling clock bear a strong resemblance to classical FM modulation. The input frequency is equivalent to the carrier frequency, and the clock jitter frequency (or spectrum) is equivalent to the modulation frequency. For simplicity of initial analysis, consider an ADC with a sine wave input signal, and a sampling clock time modulated (jittered) by a low frequency sine function. If a record of data is taken from the ADC and analyzed using Fourier analysis, then the effect of the clock jitter is to reduce the height of the input sine component, and to introduce sideband frequency components. The sideband frequencies are equally spaced either side of the input component, at a distance equal to multiples of the jitter frequency. The amplitude of the sidebands varies with the amount of clock jitter. However clock jitter is not precisely FM modulation; there are some important behavioural differences. The equation for sinusoidal sampling clock time jitter is:

$$v(t) = A \cos[\omega_i(t + J \sin \omega_j t)] \quad (1)$$

where  $A$  is the ADC input signal amplitude,  $\omega_i$  is the input signal frequency,  $J$  is the peak amplitude of the jitter, and  $\omega_j$  is the jitter frequency. Notice that if  $\omega_i$  is increased then the contribution of the jitter term also increases. This agrees with the intuitive reasoning that if the slew rate of the input signal increases, then the amplitude error caused by clock jitter will increase. Notice also that the units of  $J$  is time, in seconds.

Equation (1) may be re-written as:

$$v(t) = A \cos[\omega_i t + J\omega_i \sin \omega_j t]$$

Substituting  $\beta = J\omega_i$  gives:

$$v(t) = A \cos[\omega_i t + \beta \sin \omega_j t] \quad (2)$$

Equation (2) is the classical FM modulation equation, where  $\beta$  is the modulation index. Analysis of the height of sidebands in terms of  $\beta$  is well documented using Bessel functions [1], where  $J_0(\beta)$  is the relative amplitude of the input frequency component, and  $J_1(\beta)$  is the relative amplitude of the first pair of sidebands. Since we are only concerned with small amounts of clock jitter, and therefore small  $\beta$ , only the first pair of sidebands are significant.

As an example of using these formulae, let's set the input frequency to 10900 Hz, and the clock jitter peak amplitude to 1 ns. Therefore, since  $\beta = J\omega_i$ ,  $\beta = 6.848 \times 10^{-5}$  radians. Unfortunately, commonly available tables of Bessel functions have  $J_0(\beta)$  and  $J_1(\beta)$  values for  $\beta = 0$ , and then for  $\beta = 0.1$ , and are therefore useless for determining sideband heights for very small  $\beta$ . However, as a result of previous work at Crystal Semiconductor concerning testing T1 line interface parts for very low jitter specifications [2], a useful relationship between  $\beta$  and  $J_1(\beta)/J_0(\beta)$  was noticed:

$$J_1(\beta)/J_0(\beta) = \beta/2 \quad (\text{only for very small } \beta) \quad (3)$$

This relationship is also confirmed by approximations for Bessel coefficients given in [3].

Using (3) gives us a  $J_1(\beta)/J_0(\beta)$  ratio of  $3.424 \times 10^{-5}$ , which is -89.3 dB. Quantization noise for a 16-bit, Nyquist sampling ADC is -122 dB peak with respect to a 0 dB full scale input. Assuming the ADC is normally run at -10 dB input level for full amplitude music, then the sidebands have to be -112 dB down to guarantee non-audibility. Therefore for our example, the sidebands may be audible (ignoring masking effects of the ear).

How much clock jitter will cause a sideband to rise above the quantization noise floor, and therefore be potentially audible? Using the above equations, and for an input frequency of 10900 Hz, assuming a 16-bit ADC, the answer is 232 ps peak clock jitter. This result aligns well with previously published estimates [4].

## 2 Clock Jitter Simulations

In order to facilitate the understanding of the effects of clock jitter, a simulation program was written, as shown in Figure 1. Line 160 through line 210 form the main program loop, which increments the time sample count, G, by one for each pass. Line 170 calculates the jitter amplitude for each sample. Line 180 simulates a pure cosine input signal, jittered by an amount of time, J. Notice the use of double precision arithmetic. Lines 185 and 200 quantize the output values to X bits. The output of the program is a set of numbers which are written to a file.

To confirm the accuracy of the simulation compared to theory, the program was run with the same input conditions as used in the theory example. The resulting file of numbers was then processed by a standard FFT analysis and display program in routine use at Crystal Semiconductor for testing all types of ADCs [5]. Figure 2 shows the resulting spectrum. The two sidebands are 89.66 dB down from the input frequency amplitude, which agrees closely with the theoretical result.

Modifying line 170 allows changing the nature of the clock jitter. Changing line 180 allows investigation of different ADC input signals.

## 3 Measured Results

A CS5101 sampling successive approximation ADC was used to verify the theoretical and simulation results. Figure 3 shows the test set-up. A 6.144 MHz clock was used to allow later substitution of an alternate delta-sigma ADC. Using a 6.144 MHz clock determines the sample rate of 76.8 kHz. Figure 4 shows the Phase Lock Loop (PLL) circuit used to inject clock jitter. The set-up was verified to introduce no additional distortion compared to a jitter free crystal based clock source. Clock jitter is added by injecting the desired jitter modulation signal into the Voltage Controlled Oscillator (VCO) of the PLL.

Using the same conditions as used for the theoretical and simulation example, the sidebands were shown to be 89.74 dB down from the input frequency component, shown in Figure 5. This validates the theory and simulation results. The clock jitter was checked by displaying a divided down version

of the jittered clock on a delayed time base oscilloscope. Figure 6 shows a rising edge of the divided clock, corrupted by 1 ns peak jitter. This measurement was taken at the same time as the Figure 5 test result plot.

Correlation between clock jitter amplitude and side-band height has previously been verified at Crystal Semiconductor by compared the jitter readings of an HP 3785A jitter test unit with the same clock jittering an ADC sampling clock [2].

#### **4 Oversampling ADC Clock Jitter Sensitivity**

Oversampling delta-sigma ADC's have several advantages over more traditional Nyquist sampling successive approximation ADC's and are also becoming more available [6]. The CS5326 from Crystal Semiconductor has an oversampling ratio of 64, sampling the input at 3 MHz. The output of the delta sigma modulator is a 3 MHz serial bit stream which is then digitally filtered (dc to 22 kHz) and decimated to produce 16-bit numbers at a 48 kHz word rate. How sensitive is such an ADC to clock jitter?

As a proportion of clock period, a given amount of jitter is more significant to a 3 MHz sampling clock, compared to a 50 kHz sampling clock. However the amount of amplitude error resulting from the clock jitter is the same in both cases, since the slew rate of the input signal is the same. Also, for noise induced jitter, the extra noise induced by the jitter will be spread out between dc and 1.5 MHz, and then low pass filtered by the 22 kHz cut-off digital filter. Thus it is reasonable to speculate that an oversampling delta-sigma ADC will be no more sensitive to clock jitter than a Nyquist sampling ADC. To prove this hypothesis, a theoretical simulation was performed, along with measured results.

Figure 7 shows the results of the CS5326 oversampled ADC simulation program. The input conditions were the same as previously used, that is an input frequency of 10900 Hz, 1 ns peak sinusoidal 980 Hz jitter, and -10 dB input amplitude. The difference in amplitude between the fundamental and the jitter induced sidebands is 89 dB, which is the same result as obtained in the Nyquist sampling case. The lack of low frequency noise in Figure 7 is because the simulation did not include the final truncation to 16-bits after the filter.

Figure 8 shows the measured results from the CS5326 oversampled ADC. The test conditions were the same as above, and the test set-up was the same as shown in Figure 3, using a CDB5326 evaluation board. The plot shows that the difference in amplitude between the fundamental and the jitter induced sidebands is 89.5 dB, which agrees well with the oversampled ADC simulation results, and with the previously given non-oversampled ADC test results.

The above results confirm that an oversampled delta-sigma ADC has the same sensitivity to clock jitter as a Nyquist sample rate ADC.

## 5. Non Sinusoidal Jitter

In practical hardware, clock jitter will not be sinusoidal. It is likely to consist of noise components and some periodic components. To investigate the effects of white noise jitter, the simulation program given in Figure 1 was modified, replacing the sine jitter equation with a random number generator equation (Figure 9).

A number of simulations were run which show that white noise clock jitter results in an overall elevation of the noise floor of the ADC system. This will degrade the available dynamic range. For example, 2 ns peak white noise clock jitter will degrade a perfect 16-bit ADC from a dynamic range of 98 dB to 91 dB (Figures 10 & 11). To reduce clock jitter effects to less than 0.5 dB impact on dynamic range, the peak jitter amplitude has to be less than 400 ps (Figure 12).

For oversampling ADC's, we speculated that the effects of clock jitter noise would be treated like quantization noise, that is spread out between DC and half the input sample rate, and then filtered by the audio bandwidth digital filter. Figure 13 shows the results of a delta sigma ADC simulation, with 2 ns peak white noise clock jitter. Compared to Figure 11, this confirms that the delta sigma ADC is much less sensitive to white noise clock jitter. As with Figure 7, Figure 13 does not include 16-bit quantization noise.

## 6. Conclusions

A combination of theoretical analysis, computer simulations and practical measurements has allowed the confident prediction of the audible effects of sampling clock jitter. As the resolution, and therefore dynamic range, of ADC's and DAC's increase beyond 16-bits, sampling clock jitter will become more significant. The analysis techniques presented allow maximum allowable levels of clock jitter to be determined.

It has been demonstrated that delta-sigma oversampling ADC's are no more or less susceptible to the effects of clock jitter than Nyquist sampling architectures. It has also been shown that delta-sigma oversampling ADC's are less sensitive to random noise clock jitter than Nyquist sampling ADC's.

## 7. Acknowledgements

My sincere thanks go to Greg Stearman, Bruce Del Signore, Dan Caldwell, John Lamay and Eric Swanson at Crystal Semiconductor for their theoretical and practical help in preparing this paper.

## 8. References

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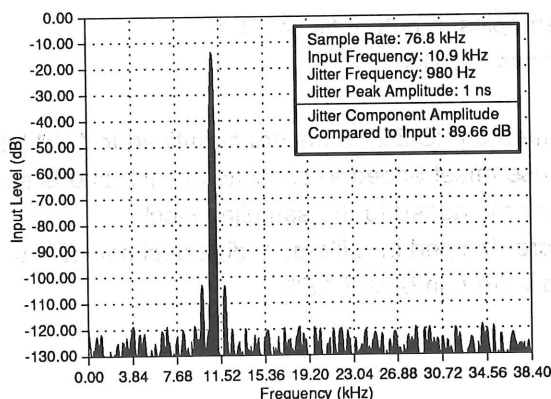
10 REM  ADC SIMULATION PROGRAM "JITSINE"      Steven Harris  8/3/89

95 INPUT "Number of samples in output file ?",SIZE
96 REM Set X = to # of bits in ADC
97 LET X = 16
100 PRINT "JITSINE generates ";SIZE;" numbers quantised to ";X;" bits"
102 PRINT "Random phase offset added to simulate asynchronous sampling"
103 PRINT "Sine wave jitter is added to the sampling clock"
110 REM The numbers are dumped in a file as 5 digit decimal values
112 INPUT "File name to write numbers ? ",F$
113 OPEN "O",#1,F$
116 Offset=RND
117 Offsetj=RND
135 LET PI#=3.141592654
143 INPUT "Sample Frequency ?",FS#
145 INPUT "Input Signal Frequency ?", FIN#
146 INPUT "Input Signal Amplitude relative to full scale (=1) ", INAMP#
147 INPUT "Jitter Frequency ?",FJ#
149 INPUT "Peak amplitude of clock jitter in seconds ?",JPA#
160 FOR G = 1 TO SIZE
168 REM Form jitter amplitude for this time sample
170 LET J# = JPA#*SIN(Offsetj + ((G-1)*2*PI#*FJ#/FS#))
172 REM Form unquantized clock jittered cosine value for this sample
180 LET A# =INAMP#*COS(2*PI#*FIN#*(((G-1)/FS#)+J#)+Offset)
182 REM Scale to X bits
185 LET A# = A#*(((2^X)/2)-1)
198 REM Quantize levels (round to nearest integer)
200 LET S = CINT(A#)
205 REM PRINT "#="G;"Value=";A#;"Quantized value=";S
207 PRINT #1, USING "#####";S
210 NEXT G
220 CLOSE #1

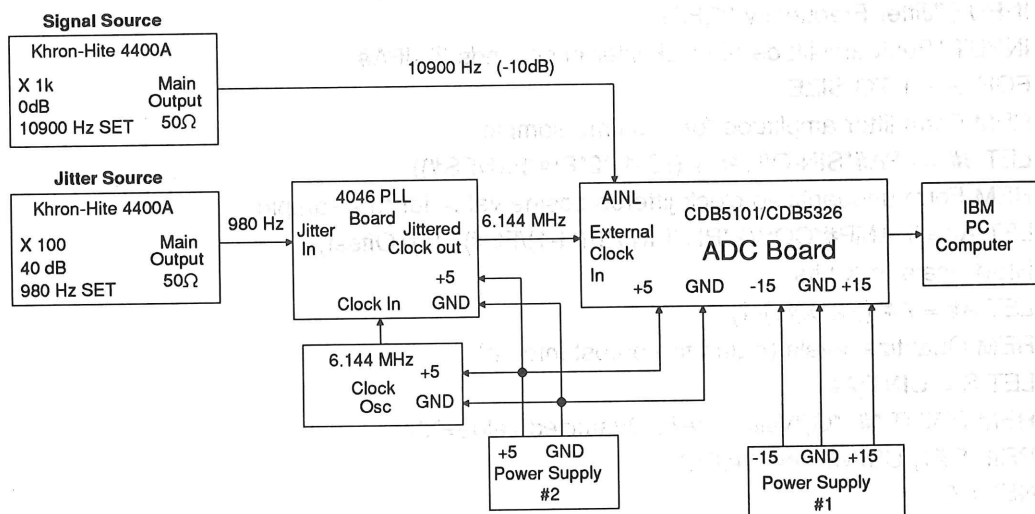
```

Figure 1. BASIC program which simulates a perfect N-bit ADC with sinusoidal clock jitter





**Figure 2. Nyquist Sampling ADC Simulation with 1 ns Peak Sine Clock Jitter**



**Figure 3. Jitter Experiments Test Set-up**

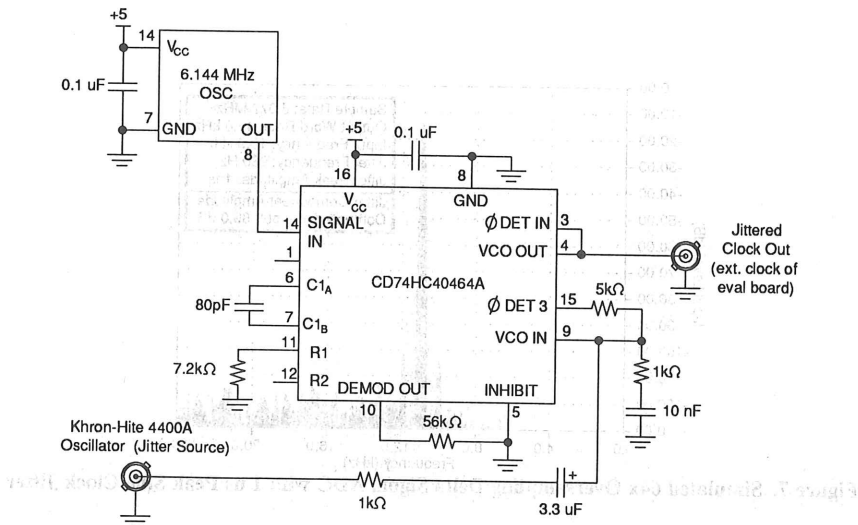


Figure 4. Phase Locked Loop Jitter Generator Schematic

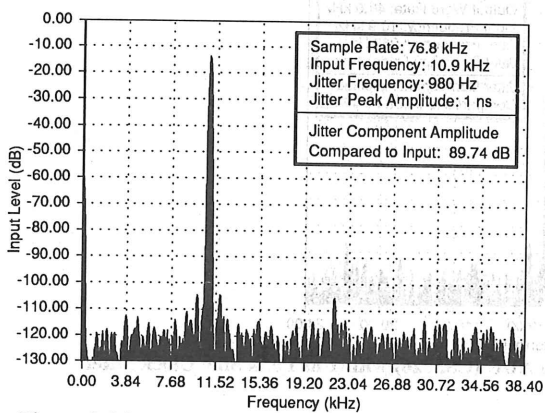


Figure 5. Measured Nyquist Sampling ADC (CS5101) with 1 ns Peak Sine Clock Jitter

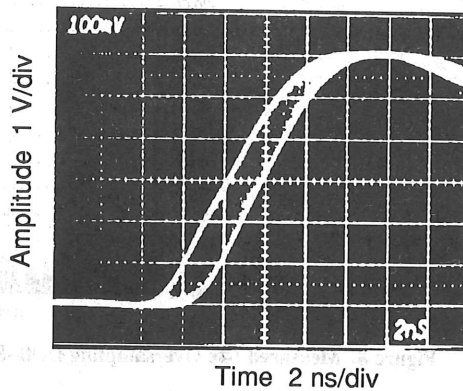


Figure 6. ADC Sampling Clock Jitter Measured at the Output of the Clock Jitter Generator Shown in Figure 4

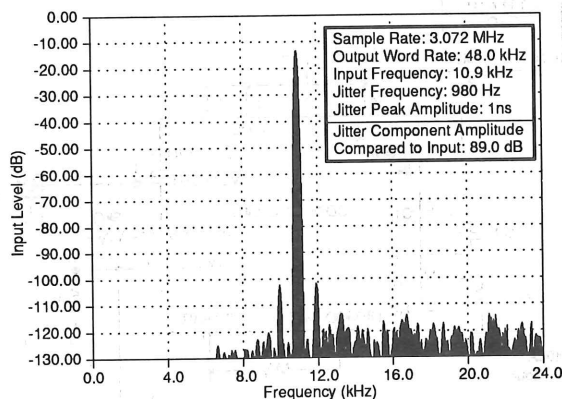


Figure 7. Simulated 64x Oversampling Delta Sigma ADC with 1 ns Peak Sine Clock Jitter

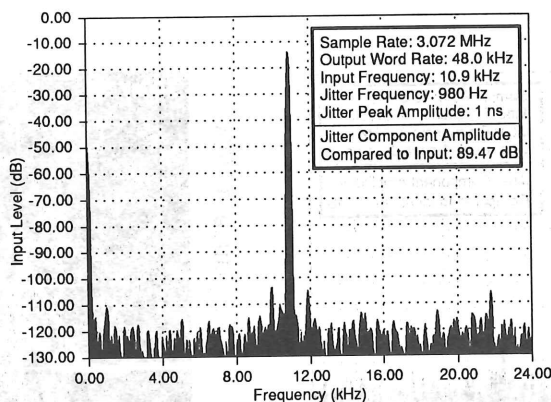


Figure 8. Measured 64x Oversampling Delta-Sigma ADC (CS5326) with 1 ns Peak Sine Clock Jitter

```
10 REM  ADC SIMULATION PROGRAM  "JITNOISE"  Steven Harris 8/3/89

95 INPUT "Number of samples in output file ?",SIZE
96 REM Set X = to # of bits in ADC
97 LET X = 16
100 PRINT "JITNOISE generates ";SIZE;" numbers quantised to ";X;" bits"
102 PRINT "Random phase offset added to simulate asynchronous sampling"
103 PRINT "White noise jitter is added to the sampling clock"
110 REM The numbers are dumped in a file as 5 digit decimal values
112 INPUT "File name to write numbers ? ",F$
113 OPEN "O",#1,F$
116 Offset=RND
117 Offsetj=RND
135 LET PI#=3.141592654
143 INPUT "Sample Frequency ?",FS#
145 INPUT "Input Frequency ?", FIN#
146 INPUT "Input signal amplitude relative to full scale (=1) ?", INAMP#
149 INPUT "Peak amplitude of clock jitter in seconds ?",JPA#
160 FOR G = 1 TO SIZE
169 LET NOISE=RND
170 LET J# = JPA#*(NOISE*2-1)
172 REM Form perfect clock jittered sine
180 LET A# = INAMP#*COS(2*PI#*FIN#*(((G-1)/FS#)+J#)+Offset)
182 REM Scale to X bits
185 LET A# = A#*(((2^X)/2)-1)
198 REM Quantize levels (round to nearest integer)
200 LET S = CINT(A#)
205 REM PRINT "#="G;"Value=";A#;"Quantized value=";S
207 PRINT #1, USING "#####";S
210 NEXT G
220 CLOSE #1
230 GOTO 95
```

Figure 9. BASIC program which simulates a perfect N-bit ADC with noise jittered clock

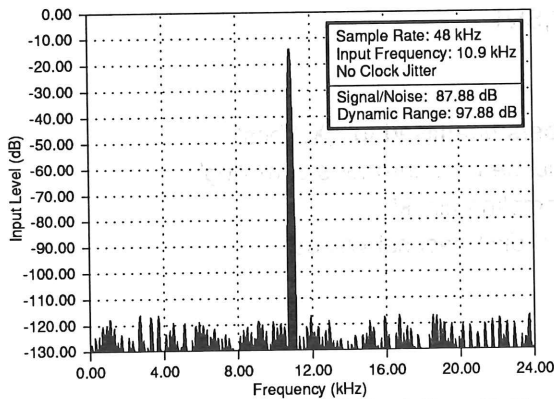


Figure 10. Nyquist Sampling ADC Simulation with No Clock Jitter

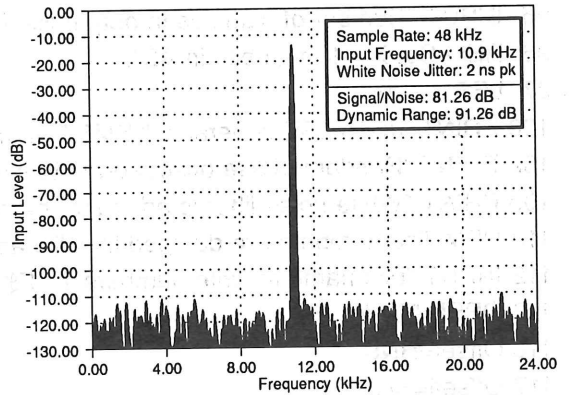


Figure 11. Nyquist Sampling ADC Simulation with 2 ns Peak White Noise Clock Jitter

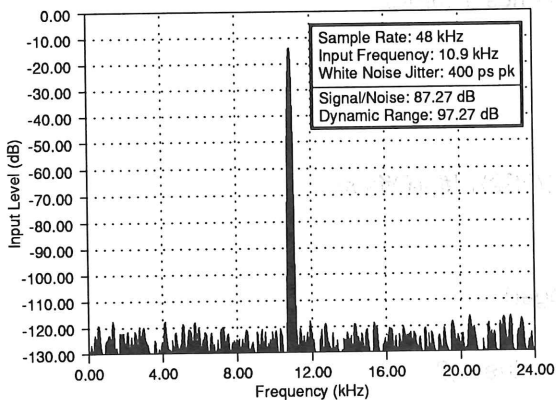


Figure 12. Nyquist Sampling ADC Simulation with 400 ps Peak White Noise Clock Jitter

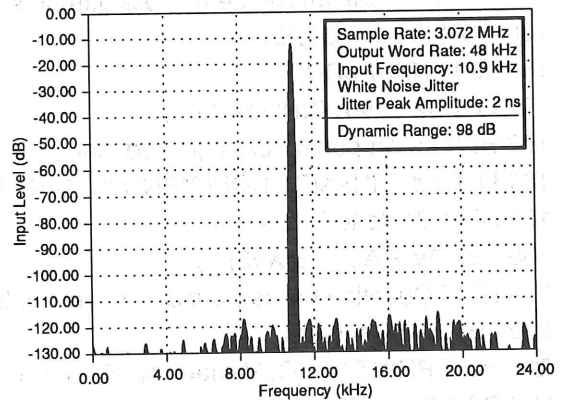


Figure 13. Simulated 64x Oversampling Delta-Sigma ADC with 2 ns Peak White Noise Clock Jitter

## **18-BIT STEREO D/A CONVERTER WITH INTEGRATED DIGITAL AND ANALOG FILTERS.**

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### **ABSTRACT**

This paper describes an integrated digital audio Digital-to-Analog output system. The circuit consists of an 8x digital interpolation filter followed by a 64x oversampled Delta-Sigma modulator. The modulator output controls the reference voltage input to an ultra-linear analog low pass filter. The total D/A system provides a linear phase response.

### **INTRODUCTION**

Delta-sigma modulation has become the conversion technology of choice for audio-band data converters. Analog-to-Digital converters using the delta-sigma conversion principle have been available for many years. The several advantages of delta-sigma modulation already demonstrated for A/D converters also apply to D/A converters. The benefits of delta-sigma modulators over conventional laser trimmed converters include:

1. No differential linearity error.
2. No distortion mechanisms due to component mismatch.
3. No laser trimming.
4. No linearity error drift over time and temperature.

Previous delta-sigma audio D/A converter implementations have either not integrated the analog filter or required several external filter components [1],[2]. These implementations require component value changes for large variations in conversion rate. This paper presents an 18-bit stereo D/A converter employing delta-sigma modulation that integrates digital and analog filters that track the conversion rate. No external components are required.

The block diagram of the complete system is shown in figure 1. An 8x interpolation filter removes out-of-band images. The output of the interpolator is held for eight,  $64f_s$  cycles and fed into a 5th order delta-sigma modulator. An analog filter removes high frequency quantization noise in the modulator output and presents a signal suitable for playback. The interpolation filter and modulator are implemented on a  $1.6\ \mu\text{m}$  double metal CMOS chip. The analog filter is implemented in a  $3\ \mu\text{m}$  CMOS chip. Both chips are packaged in one 28-pin DIP.

## **INTERPOLATION FILTER**

The purpose of the digital interpolation filter is to remove images of the baseband audio signal that exist in the sampled data signal. Figure 2a shows the spectrum of the sampled data signal that is input to the D/A converter. The spectrum (chosen here to have near uniform frequency content) has images of the baseband audio signal that repeat at the input sample rate ( $f_s$ ) of the D/A converter. Although the frequency content of the images is above the human hearing range (20kHz), inevitable nonlinearities downstream from the D/A converter require removal of these images. Intermodulation of the signals above the audio band by these nonlinearities can result in audible by-products. Figure 2f is the desired signal that should be output by the D/A converter.

The interpolation filter is implemented in three consecutive interpolate by 2 stages as shown in Figure 3. This three stage FIR architecture meets two design goals. The first goal is adequate image rejection. The second design goal is to implement two channels of interpolation filters with a single hardware multiplier that operates at a maximum clock rate of  $256f_s$  (12.288MHz for sampling rate of 48kHz).

The first stage of interpolation is a 125 tap half-band FIR filter (i.e. every other coefficient except for the center coefficient is zero) [3]. The half-band topology is well suited for 2x interpolation and decimation filters since it provides rejection above one fourth the filter's sample rate reference. The spectrum at the output of the first stage is shown in figure 2b. Note that the first image is removed by this stage of filtering. The first stage is the most difficult of the three interpolation stages since it requires the steepest roll-off characteristics.

The second interpolate by two stage is a 24 tap FIR filter. The third interpolate stage is a 4 tap FIR filter. The spectra at the output of the second and third stages are shown in figure 2c and 2d, respectively. Note that the complete interpolation filter provides less attenuation for higher frequencies than for frequencies just outside the audio band. This is done with the knowledge that the analog filter will easily attenuate signals at higher frequencies but will have difficulty filtering signals just above the audio band.

Eighteen bit wide data paths with 19-bit coefficients are used throughout the interpolation filter. The S/N for a full scale sinewave (noise due to truncation) of the interpolation filter is over 107dB in the audio band.

## **DELTA-SIGMA MODULATOR**

The fifth-order delta-sigma modulator shown in figure 4 is used to convert the output of the interpolation filter into a 1-bit stream. The signal is converted to a 1-bit stream so that an inherently linear 1-bit D/A converter can be used. The modulator is sampled at  $64f_s$ . The output of the interpolation filter is held for eight consecutive modulator clock cycles yielding a sinc filter characteristic. The spectrum of the signal at the input to the modulator is shown in figure 2e. The fifth order modulator was chosen to keep all inband quantization noise peaks well below -130dB, and is similar to other high order modulator topologies [4]. The spectrum at the output of the & modulator is shown in figure 5 for a modulator sample rate of 3.072MHz. This figure is a simulation of the

modulator alone and does not include any effects of the digital or analog filters. The S/N of the modulator in the 20kHz audio band is 120dB.

### 1-BIT D/A

The many advantages of 1-bit D/A conversion can only be enjoyed if the D/A converter has only two distinct output levels. Errors in the two output levels caused by noise, interference, or dependence on previous states can substantially degrade the S/N ratio of the D/A converter. Many delta-sigma D/A converters perform the 1-bit conversion by holding an output voltage level for a finite duration of time defined by periods of a master clock source[1]. This waveform is then filtered by a continuous-time analog filter. The resulting output is highly dependent on purity of the clock signal used to gate the output voltage level. Jitter in the clock source directly translates to errors in the 1-bit D/A output.

The requirement for a low jitter clock can be essentially eliminated by the use of a switched capacitor structure. A switched capacitor filter processes packets of charge. The 1-bit D/A converter is implemented by charging a capacitor to a voltage reference and choosing the appropriate polarity of the charge by one of two switching arrangements. As long as the voltage reference value settles on the capacitor, the magnitude of the charge packet will be independent of the clock jitter.

### ANALOG FILTER

The block diagram of the analog filter is shown in figure 6. The first switched-capacitor filter has fourth-order Butterworth response with a -3dB frequency of 25kHz. The topology of the fourth-order switched capacitor filter is shown in figure 7. The multiple feedback loop topology is chosen over the traditional cascaded biquad configuration for its high noise rejection of integrators 2, 3, and 4. The sampling rate of the switched capacitor filter is  $64f_s$ , identical to that of the delta-sigma modulator.

Switched capacitor filters have generally been used in telecommunications circuits for their precise frequency response characteristics and their unique ability to scale frequency response directly with the clock rate. Switched-capacitor structures used as 1-bit D/A post filters offer the further benefit of easing the delicate transition from discrete-time to continuous-time processing. With the exception of the final stage, signal processing in a switched-capacitor filter is performed entirely in the sampled-data domain where nonlinear opamp settling behavior cannot distort signals of interest. Consequently, the strong high frequency energy of the 1-bit pattern is substantially reduced before it has the opportunity to excite any dynamic nonlinearities in subsequent continuous-time filtering.

The use of switched-capacitor filters in audio applications has been quite limited because of their traditionally inadequate dynamic range. The economics of integration have historically restricted switched capacitors to values that realize relatively high effective impedances. The result is a high thermal noise floor in the frequency range of interest. In this design, dynamic range is extended to 97dB (A-weighted) by appropriate selection of loop topology, opamp topology and capacitor values.



The distortion mechanisms traditionally associated with switched-capacitor structures have further limited their use in high performance applications. Distortion in switched capacitor filters is primarily caused by nonlinear charge injection during sampling, opamp dc nonlinearities and slewing of the final stage output waveform between settled output levels [5]. In this design charge injection is kept independent of input signal levels by appropriate switch phasing, and dc opamp nonlinearity is made negligible by sufficient open loop gain.

The third distortion mechanism, arising from opamp output slew limiting, is generally the most difficult to control. Since the output of the switched capacitor filter is being treated as a continuous-time waveform, the exact nature of the transition from one settled value to the next is critical in achieving a low distortion waveform. Nonlinear behavior in this transition must be avoided.

To ease the transition between the switched-capacitor domain and the continuous-time domain the switched-capacitor to continuous-time buffer of figure 8 is used. This buffer samples the output of the switched capacitor filter after it is settled and provides a continuous-time waveform free from distortion artifacts. The switching arrangement ensures that the charge transfer from C1 to C2 is done passively and not with the assistance of the amplifier. The amplifier only supplies the charge to the output load capacitance, which at low frequencies is minimal. This buffer has a single pole response with a -3dB frequency of 50kHz.

A continuous-time filter is used to remove the remaining images at multiples of the switched capacitor sample rate ( $64f_s$ ). The continuous-time filter has a second order butterworth response with a -3dB frequency of 80kHz. The output stage of the continuous-time filter is capable of driving a  $600\ \Omega$  load with less than 0.0015% THD at 10kHz.

## **MAGNITUDE AND PHASE RESPONSE**

Although the magnitude response of the analog filter is fairly flat due to the Butterworth response, it is not sufficient for digital audio quality. To achieve greater flatness the response of the analog filters is compensated in the digital interpolation filter: FIR2, the second stage of interpolation, performs the magnitude compensation. The total calculated magnitude response of the D/A system is shown in figure 9.

Since the nonlinear phase response of the analog filter is also a concern, the phase response of the analog filter is also equalized in the digital interpolation filter. Again, FIR2 is used for phase equalization. Figure 10 plots the deviation from linear phase for the analog filter, digital filter and the combined D/A system. Total deviation from linear phase is kept to less than  $0.7^\circ$  in the audio band. Since the frequency response of the analog filter is dominated by the switched capacitor filter, the magnitude and phase equalization will be valid at any sample rate of the D/A converter.

## **OFFSET CALIBRATION**

In any integrated analog filter significant dc offsets can be generated. In this design offset calibration is performed to lower the effective offset to approximately  $20\ \mu\text{V}$ . A comparator measures the analog output of the filter with respect to ground and a successive approximation search is used to

find the offset at the input to the delta-sigma modulator. Since the comparator does not band limit at 20kHz, its decisions are impacted by the entire out-of-band quantization noise left at the output of the analog filter. To achieve repeatable and accurate calibration the output of the comparator is averaged for 1024 cycles before a successive approximation decision is made.

The actual implementation of the comparator is shown in figure 11. The output stage of the continuous-time filter is disconnected from the chip output and is used as a comparator. This eliminates the need to design a zero offset comparator and also isolates the chip output from any audible clicks that may be generated by the successive approximation search.

Audio systems are susceptible to pops and clicks generated by active circuitry during power-up and power-down transients. This design incorporates a low power supply detect circuit which holds the output shorted to ground (i.e., same as calibration mode) until the supplies are sufficiently high to allow the remainder of the analog filter to operate correctly. Hysteresis in the low supply detect circuit prevents rapid toggling of the switches near the trip point. As a result, turn-off and turn-on power transients are inaudible even for loud listening levels.

## MEASURED RESULTS

The D/A has been characterized using a CBS Test Disk 1 and an Audio Precision System One. The measured magnitude response of the complete D/A system is shown in figure 12. The slight peaking near 20kHz of 0.1dB is due to a systematic mismatch of capacitors in the switched-capacitor filter. Unweighted THD+N (0-22kHz) versus input sinewave level is shown in figure 13. A considerable portion of the output noise is concentrated near the upper end of the audio range. Dynamic range from 0-20kHz is 93.8dB and A-Weighted dynamic range is 97dB. Figure 14 is a plot of the output spectrum of a -90dB dithered sinewave at 1kHz. Because of the ideal differential nonlinearity of the 1-bit D/A, the noise floor is quite smooth. A key test of D/A converters is the fade-to-noise linearity test shown in figure 15. A monotonically decreasing sinewave is fed into the D/A converter. The energy of the output sinewave is compared with the energy of the input. Deviations from 0dB are a result of differential nonlinearity or noise. The D/A exhibits excellent performance down to -95dB where the residual output noise starts to dominate the measurement. Figure 16 is a plot of the idle channel output spectrum from 0 to 100kHz showing the relatively low level of out-of-band quantization noise. The total energy from 0-100kHz is 78dB below full scale. Table 1 is a summary of the system performance specifications.

## CONCLUSION

An 18-bit D/A converter using delta-sigma modulation has been presented. The design integrates an 8x interpolation filter with a fifth order delta-sigma modulator. On a separate chip an analog filter using a combination of switched-capacitor and continuous-time filters is implemented.

Switched-capacitor filters have the ability to change bandwidths without changing component values. One bit D/A converters implemented with switched-capacitors offer excellent clock jitter tolerance. The design difficulties associated with high quality switched-capacitor filters have been mastered. In the future even higher dynamic range switched-capacitor filters can be expected.

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**TABLE 1**

Dynamic range	97dB
A-weighted (18-bit mode)	
S/THD 1kHz	92dB
Interchannel Isolation 1kHz	-110dB
Power Consumption	
Digital	150mW
Analog	420mW
Deviation from flat magnitude	
Total D/A System	0.1dB
Deviation From Linear Phase	< 0.7°
Total D/A System	
Digital Filter Stop Band Attenuation	90dB
Digital Filter Pass Band Ripple	0.001dB

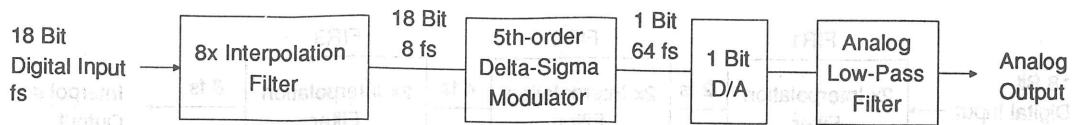


Figure 1. 18 Bit D/A Converter Architecture

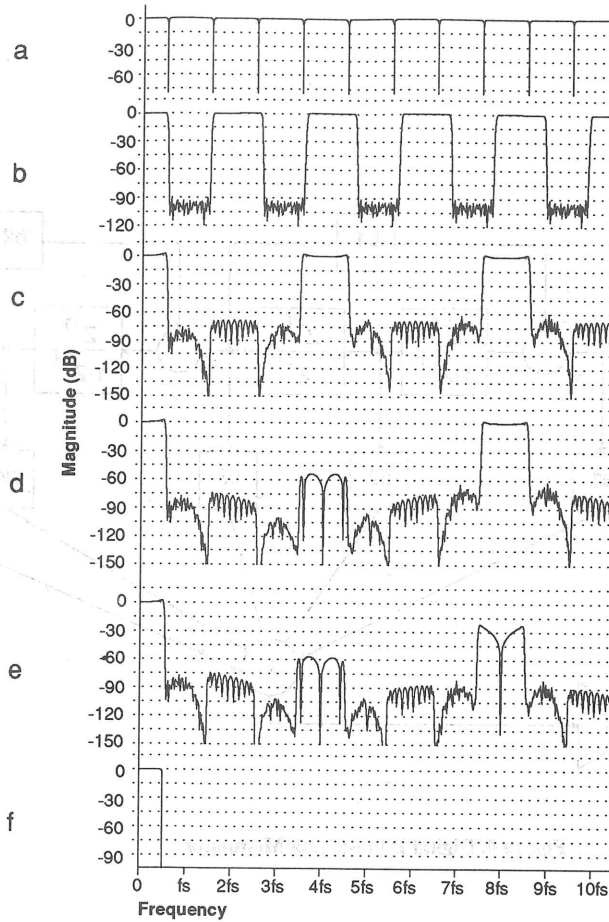


Figure 2.

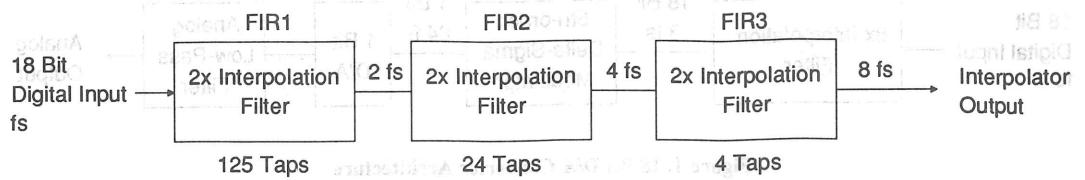


Figure 3. Interpolation Filter Architecture

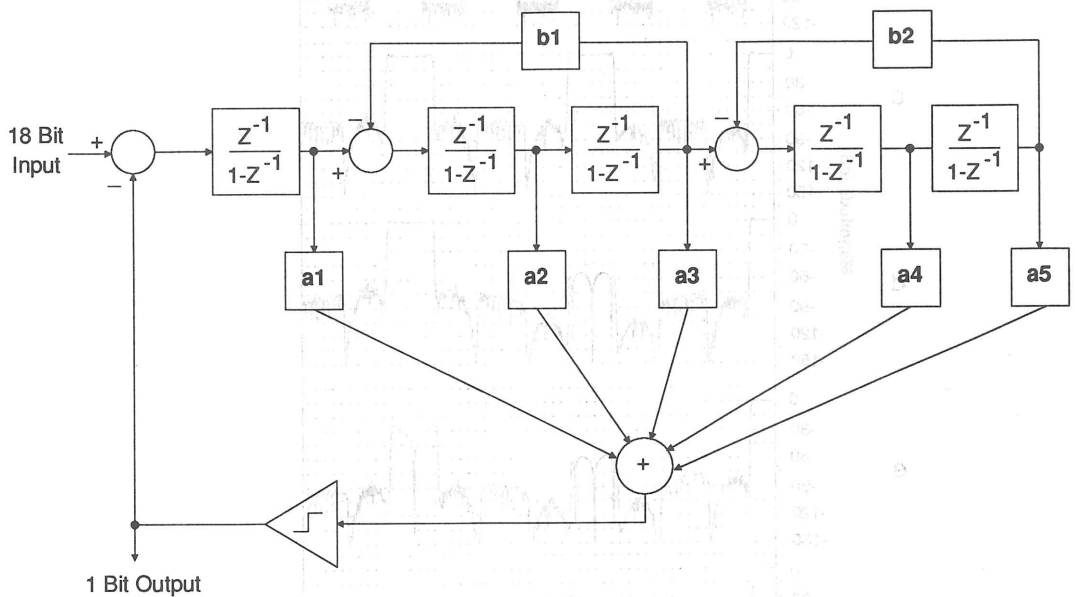
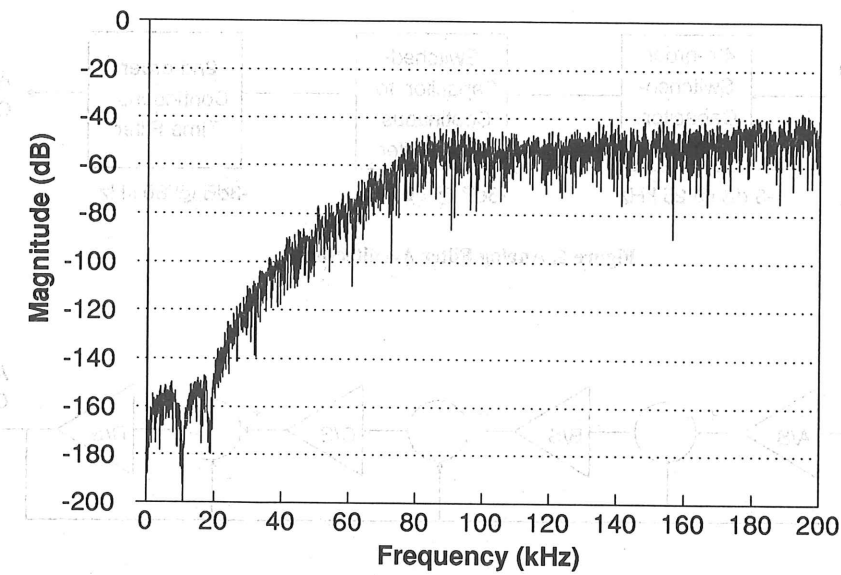


Figure 4. Digital Delta-Sigma Modulator



Modulator Output Spectrum

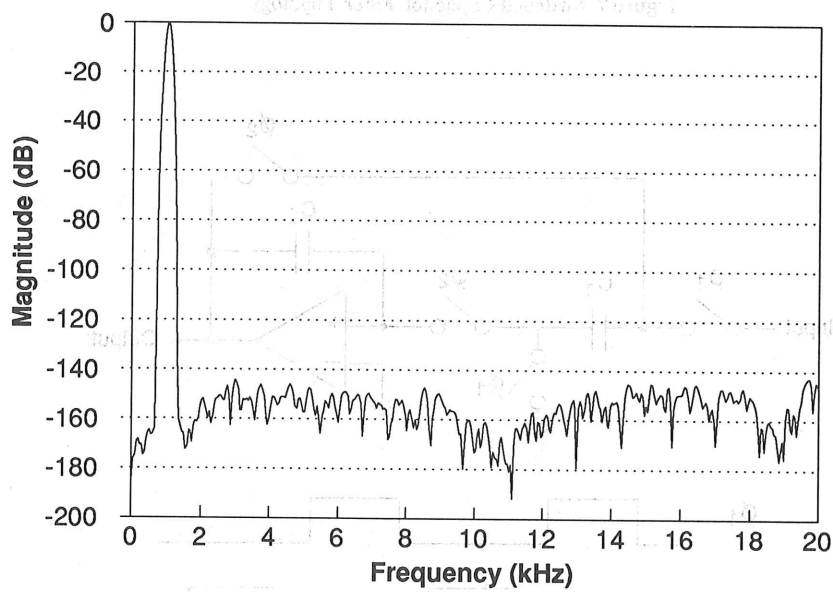


Figure 5. Expanded Modulator Output Spectrum

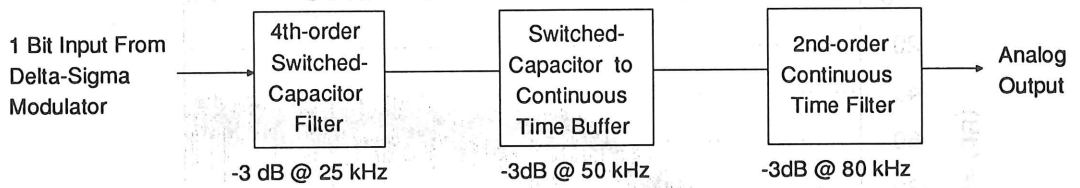
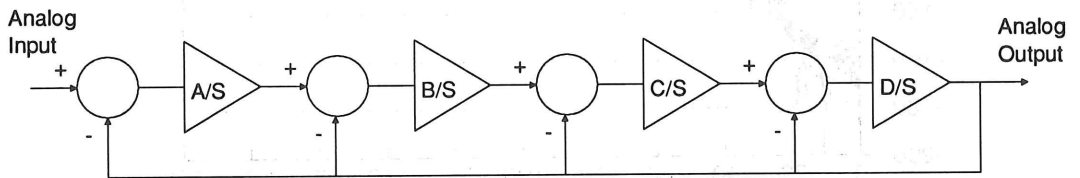


Figure 6. Analog Filter Architecture



$$\frac{V_o(s)}{V_{in}(s)} = \frac{ABCD}{S^4 + DS^3 + CDS^2 + BCDS + ABCD}$$

Figure 7. Switched Capacitor Filter Topology

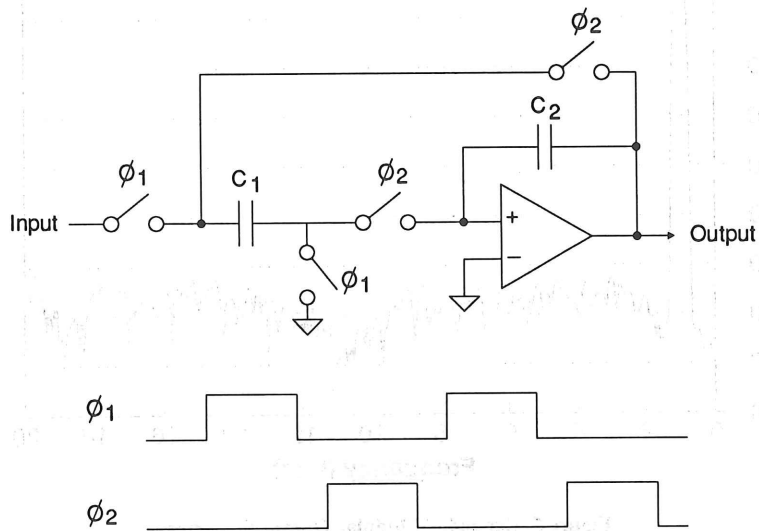


Figure 8. Switched-Capacitor to Continuous Time Buffer

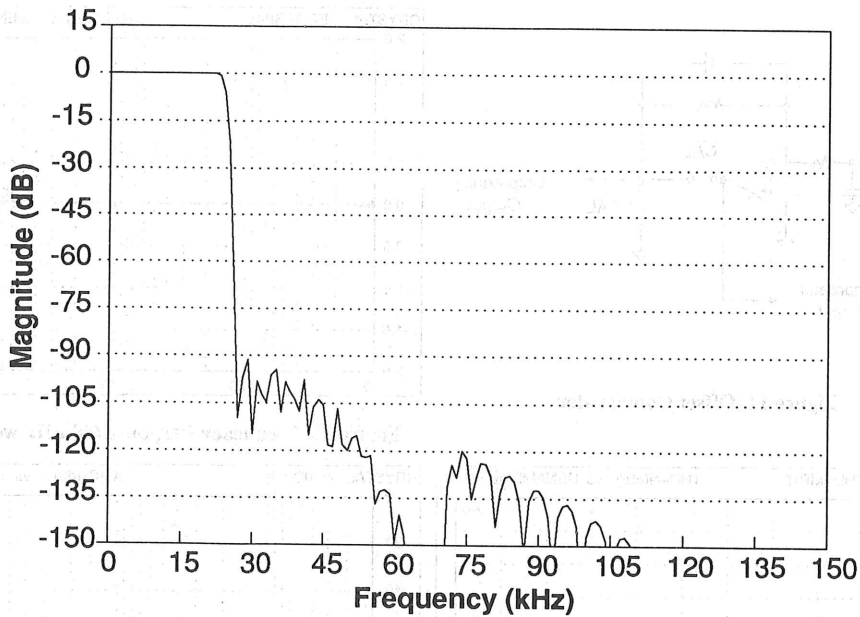


Figure 9. Total D/A System Magnitude Response

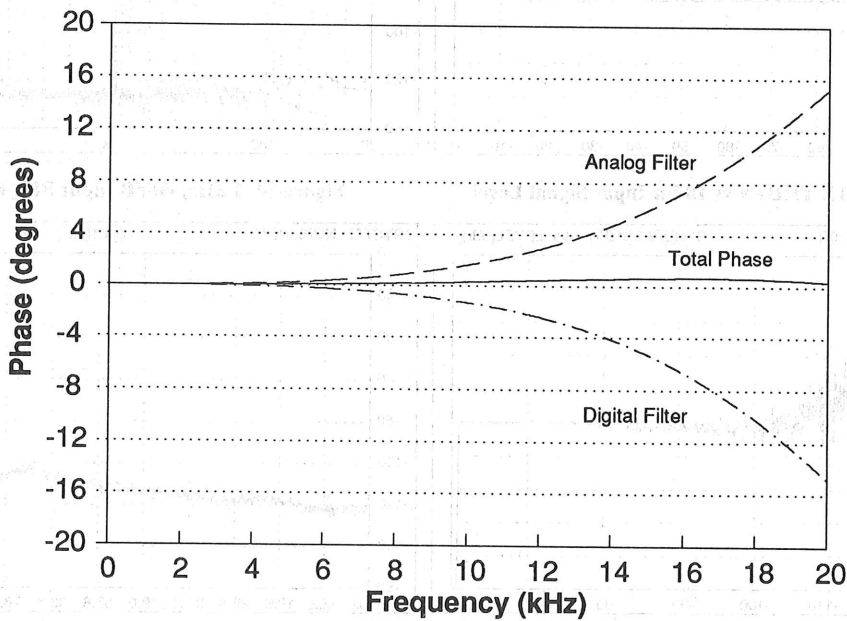


Figure 10. Deviation From Linear Phase



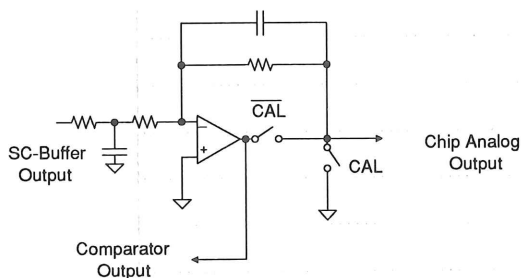


Figure 11. Offset Comparator

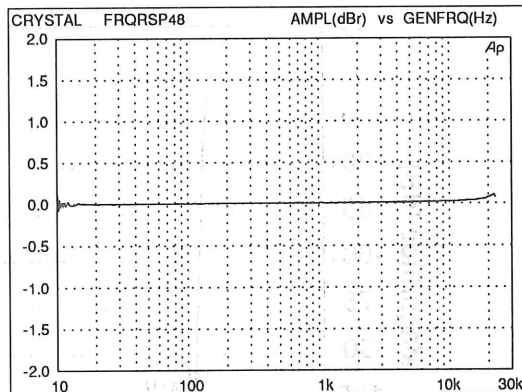


Figure 12. Frequency Response (48 kHz word rate)

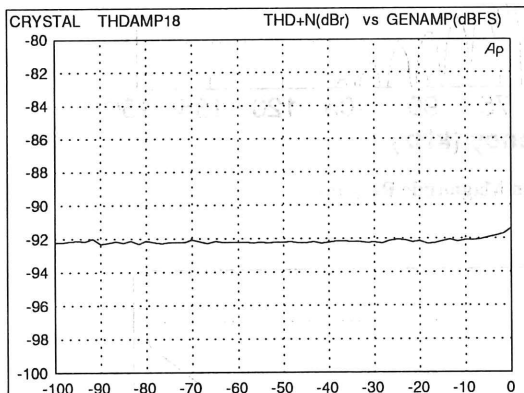


Figure 13. THD+N vs 18-bit Input Signal Level

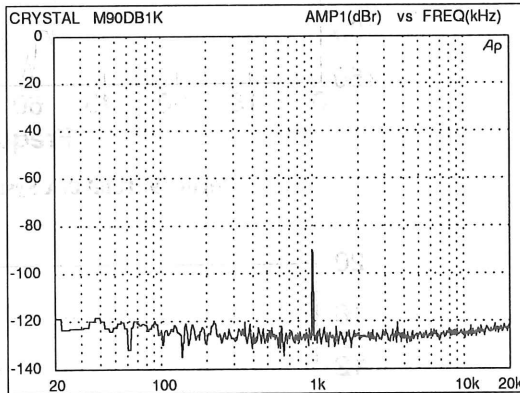


Figure 14. 1 kHz, -90dB Input FFT Plot

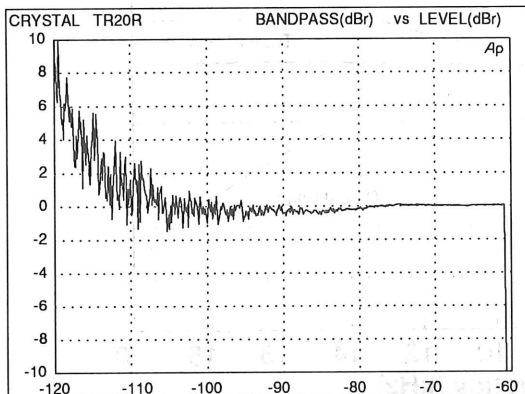


Figure 15. Fade-to-Noise Linearity

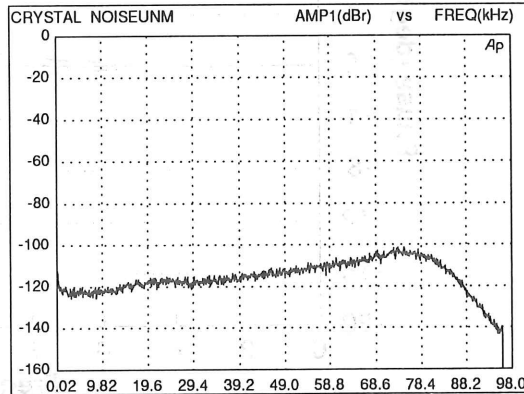


Figure 16. Unmuted Idle Channel Noise

## A Family of AES-EBU Interface Devices

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### ABSTRACT

This paper describes a family of digital audio transmitters and receivers which conform to the AES-EBU interface standard. Different versions are used to control the interface to various levels of complexity. Few external components are required to create a complete transmission link. The paper introduces the AES-EBU standard and illustrates the chip architectures.

### 1 INTRODUCTION

"The AES-EBU digital audio interface has been slow to gain market acceptance, partly because of interface complexity, specification ambiguities, lack of commercial IC's, and the effort required for discrete implementations." [1] To alleviate these problems and promote widespread use of the interface, Crystal Semiconductor has defined a family of integrated circuits that will facilitate the implementation of the AES-EBU standard. These IC's are general purpose, providing compatibility as the specifications mature, support the similar consumer-style interface, and consist of two versions of transmitters and receivers. Since the transmitters are commercially available today and the receivers are still in development, this paper will primarily discuss the transmitters, following a brief overview of the interface specifications.

### 1 AES-EBU SPECIFICATIONS

The AES-EBU interface, described in AES3-1985 [2], is a means for serially communicating digital audio data through a single transmission line. It provides 2 channels for audio data, a method for communicating control information, and some error detection capabilities. This control information is transmitted 1 bit per sample and accumulates in a block structure. Data is biphase encoded, which enables the receiver to extract a clock from the data, with coding violations identifying sample and block boundaries. The electrical specifications for the AES-EBU interface are compatible with RS-422 [3].

The structure of the serial word, called a subframe, is illustrated in Figure 1. The subframe consists of 4 bits of preamble, 4 bits of auxiliary data, 20 bits of audio data, a parity bit, and 3 bits called validity, user, and channel status. The preamble contains biphase coding violations and identifies the start of a subframe. The audio sample word length can vary up to 24 bits. If the word length is greater than 20 bits, the sample occupies both the audio and auxiliary data fields. If it is 20 bits or less, the auxiliary field can be used for other applications such as a voice channel. The parity bit generates even parity and can be used to detect an odd number of transmission errors. If an even number of bit errors occurred, the received parity will remain even and the errors will not be iden-

tified. The validity bit indicates if the audio sample is secure and error free. In some applications it identifies samples that have been interpolated due to errors. The user and channel status bits are sent once per sample and when accumulated over a number of samples can be used to transmit blocks of data. The user bit channel is undefined and is available to the user for any purpose. The channel status channel is defined and conveys important information about the audio data and transmission link. Each of the two audio channels has its own channel status channel with a block structure that repeats every 192 samples.

As shown in Figure 2, two subframes, one each from channels 1 and 2, create a frame and 192 frames generate a block. The preambles that identify the start of a subframe are unique for each channel with another third pattern identifying the beginning of channel status block. The 192 channel status bits in a block can be arranged as 24 bytes and are defined according to the AES-EBU standard as shown in Figure 3. Bytes 0 to 3 contain specific bits of information about the data and the link, bytes 4 and 5 are presently undefined, bytes 6 to 13 can be used for networking, bytes 14 to 17 function as a recording index counter by counting the number of transmitted blocks, bytes 18 to 21 record the time the signal was source encoded, byte 22 identifies which bytes of the block are valid, and byte 23 is a cyclic redundancy check character generated from the previous 23 channel status bytes (provides some error detection).

The primary difference between the AES-EBU interface and the consumer interface is the definition of the channel status bits. The definition for the consumer interface is illustrated in Figure 4. Bytes 0 to 3 contain specific bits of information about the data and the link, and bytes 4 to 23 can be used for music program production. More information on these bytes is available in the EIAJ CP-340 document [4].

The channel coding used in the AES-EBU and the consumer interface is biphasc mark. As shown in the example given in Figure 5, this means there is a transition at every data cell boundary and another transition in the middle of the data cell when transmitting a one. There is no transition in the middle of a data cell when transmitting a zero. Recovering a clock from data encoded this way is simpler than other coding schemes due to the frequent transitions. Biphasc coding also has no dc content, which allows ac coupling, and is immune to polarity inversions. Synchronization is achieved by producing biphasc coding violations in the preambles. A violation occurs when there is no transition at a data cell boundary and the patterns used to identify subframe, frame, and block boundaries are shown in Figure 6.

The electrical specifications of the AES-EBU interface require encoded data to be transmitted as a differential signal on a shielded twisted pair cable. The signal voltage can be 3 to 10 volts peak to peak when measured across a 110 ohm resistor. The consumer interface allows electrical or optical communication. As an electrical link, data is transmitted as a single ended signal on a coaxial cable with a signal amplitude of .5 volts +/- 20%, when measured across a 75 ohm load.

## **2 THE AES-EBU CHIP FAMILY**

Our AES-EBU IC'S are general purpose, support both the AES-EBU and consumer interfaces, and consist of two transmitters and two receivers. Having the line drivers on the transmitters and the line receivers and clock recovery circuits on the receivers, they provide a complete transmission link with minimal external components. Providing control of and access to all the user and channel status bits, these devices will remain compatible with the specifications as the standard matures. The two transmitter and receiver versions are appropriate for different applications. Both versions have serial ports for audio data. The first version, which consists of the CS8401 transmitter and the CS8411 receiver, has a buffer memory with a parallel port for storing control information and most of the non-audio subframe data, and should be driven by a processor. The second version, which consists of the CS8402 transmitter and the CS8412 receiver, will operate without a processor. This version is controlled by dedicated pins, and can accept and provide the non-audio data on a sample basis through serial input and output pins. Both transmitters, whose pinouts are shown in Figures 13 and 14, are available in 24 pin DIP's and SOIC's. The receivers will be available in similar 28 pin packages. Figure 7 illustrates the basic differences between the two transmitters.

Both transmitters, having RS422 differential line drivers, are compatible with the AES-EBU interface. To make these parts compatible with the consumer interface for an electrical link, the non-inverting driver output can be attenuated by an external resistive divider. This will provide the necessary single ended signal with the appropriate amplitude.

## **3 THE CS8401 TRANSMITTER**

As shown in Figure 8, the CS8401 has control registers, a status register, and a 28 byte buffer memory, which are all accessible through an 8 bit parallel port. The buffer memory holds channel status, user, and auxiliary data, and can be monitored by the status register and the interrupt pin. The device supports both the AES-EBU and the consumer interfaces by setting the channel status buffer according to the appropriate standard. When complying with the AES-EBU specification, the CS8401 can automatically generate the local sample address, the reliability flag, and the CRC character. The parity bit is always generated and audio data is entered through a serial port configured by a control register.

The buffer memory can operate in three modes. The address maps for these modes are shown in Figure 9 and are selectable by a control register. In all modes, 4 bytes of user data are buffered. This data is read cyclicly and shifted out one bit per audio sample, allowing user data to be different in channels 1 and 2. Consequently, this buffer must be reloaded every 32 samples. In buffer mode 0, in addition to the user data buffer, one entire block of channel status data is buffered. This block will be transmitted in both channel 1 and channel 2. Since an entire block is stored, only the data that changes from one block to the next needs to be updated.

In buffer mode 1, eight bytes are allocated for channel status data and 16 bytes for auxiliary data. The channel status buffer is divided into two sections. The first four locations always contain the first four bytes of channel status, identical to mode 0, and are read once per channel status block. The second four locations provide a cyclic buffer for the last 20 bytes of channel status data. Similar to mode 0, transmitted channel status data will be the same for channel 1 and channel 2. The

auxiliary data buffer is read in a cyclic manner similar to the user data buffer; however, four auxiliary data bits are transmitted per audio sample. Since the auxiliary buffer must be read four times as often as the user data buffer and is four times as large, they both need to be updated at the same rate.

In buffer mode 2, two 8-byte buffers are available for buffering both channel 1 and channel 2 channel status data independently. Both buffers are identical to the channel status buffer in mode 1, except that each channel can have unique channel status data. All modes use the status register and the interrupt pin to monitor the buffers. They can identify when the buffers are half full and empty.

When operating a digital audio interface according to the AES-EBU standard, the CS8401 can automatically generate channel status bytes 14 to 17, the local sample address, byte 22, the reliability flag, and byte 23, the CRC character, by setting the appropriate bits in a control register. The local sample address can be generated by a 32 bit counter incremented at every block boundary, the reliability flag can be transmitted with bits 5 and 7 set indicating that bytes 6 to 13 and bytes 18 to 21 are unreliable, and the CRC character can be generated independently for channel 1 and channel 2.

The serial port is used to enter audio data and consists of three pins: SCK, SDATA, and FSYNC. The serial port is double buffered with SCK clocking in data from SDATA, and FSYNC delineating audio samples and may define the particular channel, 1 or 2. A large number of input formats is supported to provide zero glue-logic interfaces to many DSP's, encoder chips, and standard audio interfaces. This port is configured by 7 bits in a control register allowing SCK and FSYNC to inputs or outputs, and allowing SDATA to sampled on the rising or falling edge of SCK and be entered MSB first, MSB last, or LSB last. In most modes audio data of 16 to 24 bits may be accepted.

#### **4 THE CS8402 TRANSMITTER**

The CS8402, since it is controlled by dedicated pins, can operate without the assistance of a microprocessor or DSP. The device accepts audio samples, through a serial port similar to the CS8401, in a limited number of formats. Several pins are dedicated to the most critical channel status bits, and all channel status, user, and validity bits can be serially input through serial port pins. The parity bit is always generated, and data is biphase mark encoded and driven through an RS422 line driver. The CS8402 can operate as an AES-EBU or consumer interface transmitter. As an AES-EBU interface device, the dedicated channel status input pins are defined according to that standard, the CRC characters are generated, and the local sample address and the reliability flag can be generated. As a consumer device, the dedicated channel status input pins are defined according to the consumer standard. When transmitting data from a compact disk, a CD subcode port can accept CD subcode data, extract channel status information from it, and transmit it as user data. Figures 10, 11, and 12 are block diagrams of Professional (AES-EBU) Mode, Consumer Mode, and CD Mode, respectively.

The audio serial port, consisting of SCK, SDATA, and FSYNC, is configured by three format control pins, and is double buffered. Like the CS8401, SCK clocks in SDATA while FSYNC delineates audio samples and may indicate the particular channel, 1 or 2. The format control pins select one of seven different formats for the serial port, which allow zero glue-logic interfaces to many data converters, DSP's, and standard audio interfaces.

Channel status, user, and validity bits can be entered through three serial port pins, which are sampled by FSYNC on a per sample basis. Any channel status data entered serially is logically OR'ed with data entered through the dedicated pins or internally generated.

Although channel status can always be entered serially, Professional, Consumer, and CD Modes offer different ways in which it can be generated. In Professional Mode, audio/non-audio mode, emphasis, sampling frequency, and some channel modes can be controlled by dedicated pins, CRC characters are inserted independently for both channels, and the local sample address and reliability flag byte can be generated. As in the CS8401, when this option is enabled, bits 5 and 7 of the reliability flag are set. In Consumer Mode and CD Mode, the copy bit, emphasis, some category codes, the generation status, and the sampling frequency can be controlled by dedicated pins. In CD Mode only, the copy bit, emphasis, and the 2 channel/4 channel bit are extracted from the CD subcode entered as user data.

## **5 THE CS8411 AND CS8412 RECEIVERS**

The CS8411 and CS8412 are receivers being developed to complement the CS8401 and CS8402, respectively. The CS8411 has a buffer memory and parallel port for control by a processor. The CS8412 is controlled by dedicated pins and operates as a stand alone device. Both parts will require only external capacitors for the clock recovery, and will be able to lock to audio sample rates of 25kHz to 55kHz. They will have schmitt trigger line receivers and will detect and report various errors conditions and information about the link, such as recovered clock frequency.

## **6 SUMMARY**

To eliminate some of the practical problems of implementing an AES-EBU digital audio interface, Crystal Semiconductor has defined integrated circuits which will permit economical and timely designs. Each version, consisting of a transmitter chip and a receiver chip, is targeted for a different application. The first version, with a parallel port and internal buffer memory, is aimed at systems requiring control of many aspects of the interface. The second version, while still able to implement the entire interface, is more suitable for systems requiring minimal control. Presently, the transmitters are available and the receivers are defined and being developed.

## **7 ACKNOWLEDGMENT**

The author would like to thank Clif Sanchez and the rest of the applications department at Crystal Semiconductor for their help in defining these products and preparing this document. Mike Callahan and Jeff Scott, also of Crystal, provided valuable assistance in circuit design.

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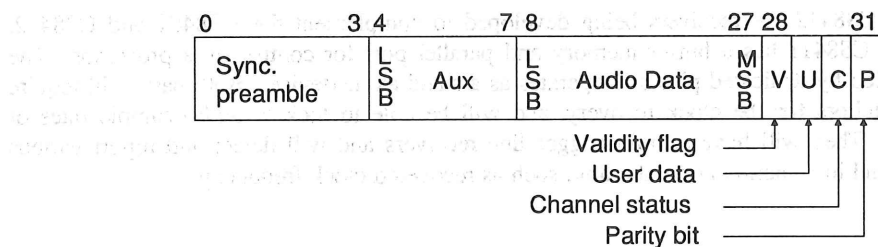


Figure 1. Subframe Format

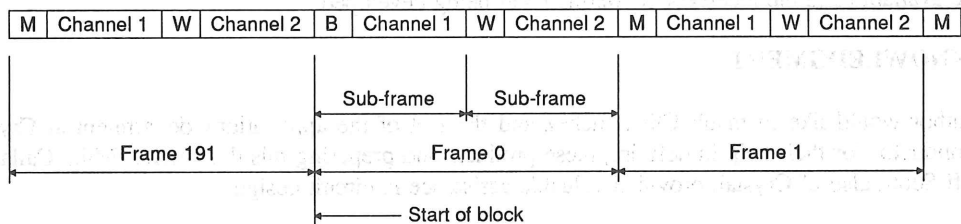
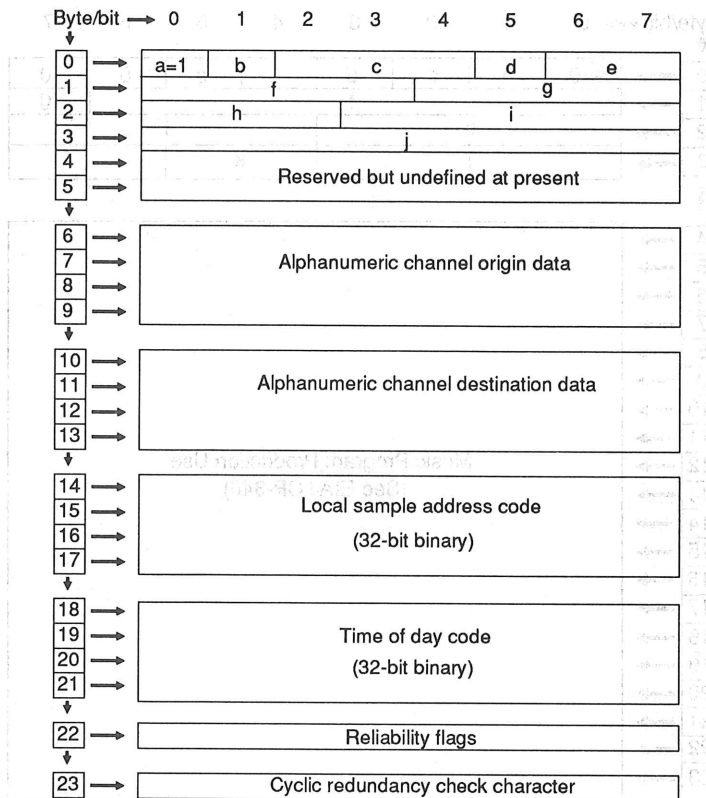


Figure 2. Frame Format

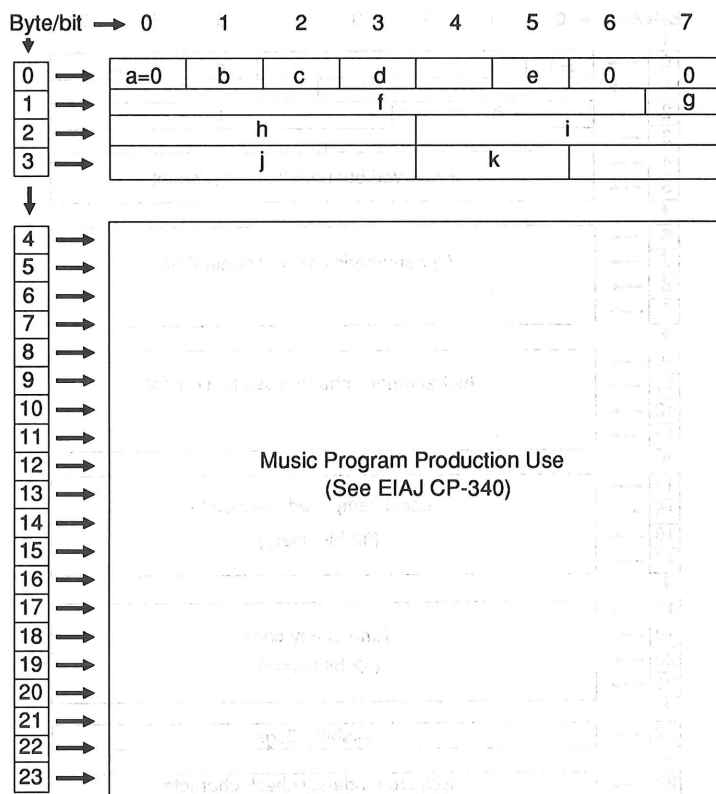




- a: Use of channel status block.      f: Channel mode.
- b: Audio/Non-audio mode.      g: User bits management.
- c: Audio signal emphasis.      h: Use of auxiliary sample bits.
- d: Locking of source sampling frequency.      i: Source word length and source encoding history.
- e: Sampling frequency.      j: Future multichannel function description.

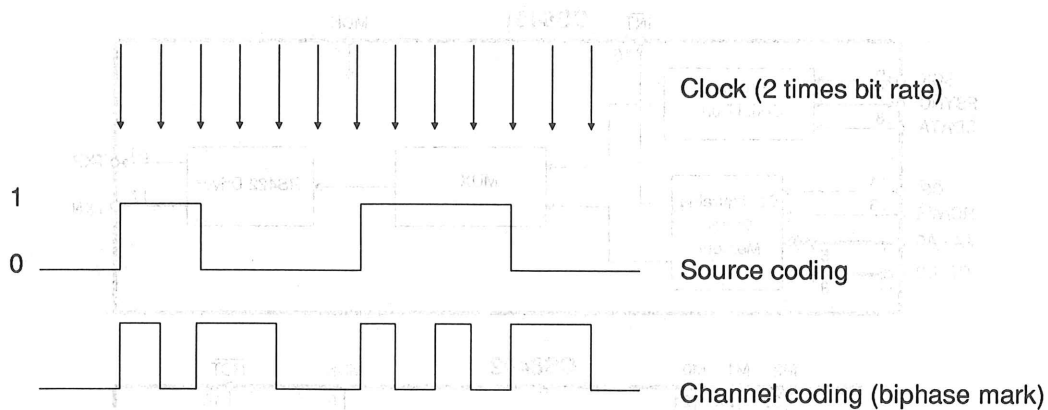
**Figure 3. AES-EBU Channel Status Data Format**



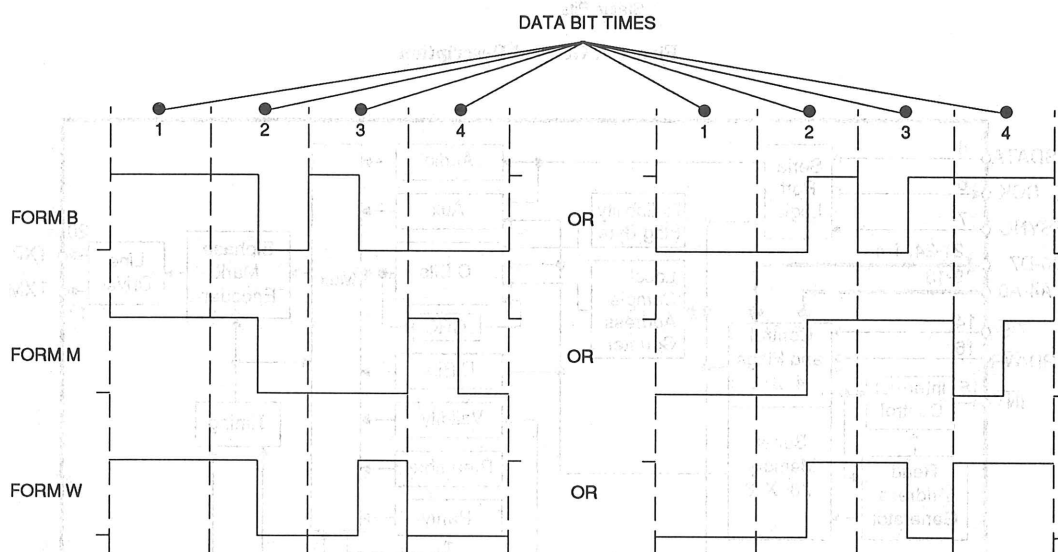


- |                                |                       |
|--------------------------------|-----------------------|
| a: Use of channel status block | g: Generation status  |
| b: Audio/Non-audio mode        | h: Source number      |
| c: Copy permitted              | i: Channel number     |
| d: Pre-emphasis                | j: Sampling frequency |
| e: 2 Channel/ 4 Channel        | k: Clock accuracy     |
| f: Category code               |                       |

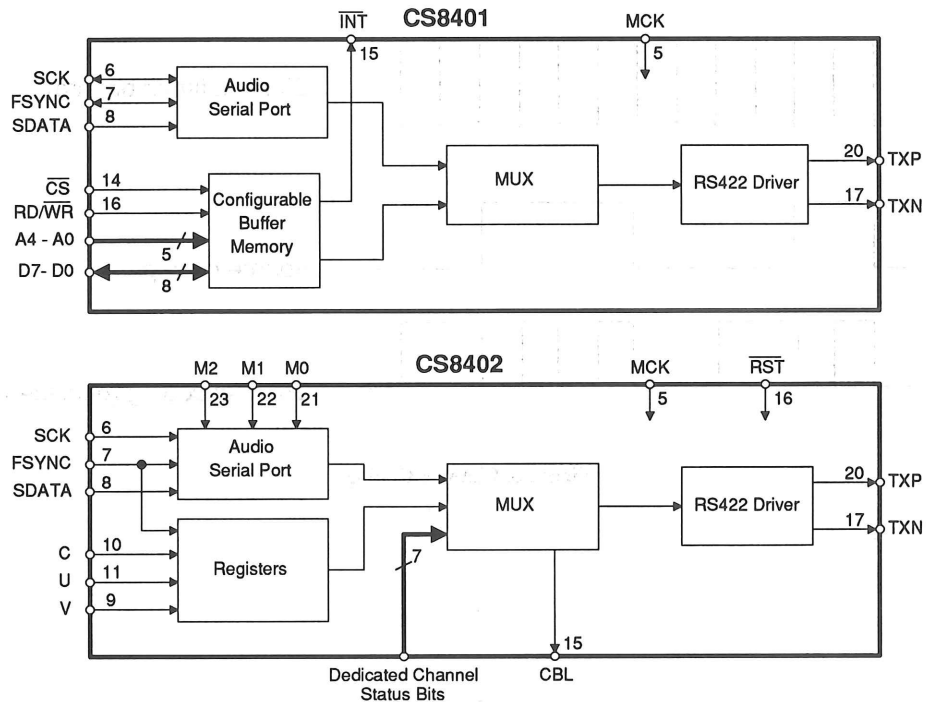
**Figure 4. Consumer Channel Status Data Format**



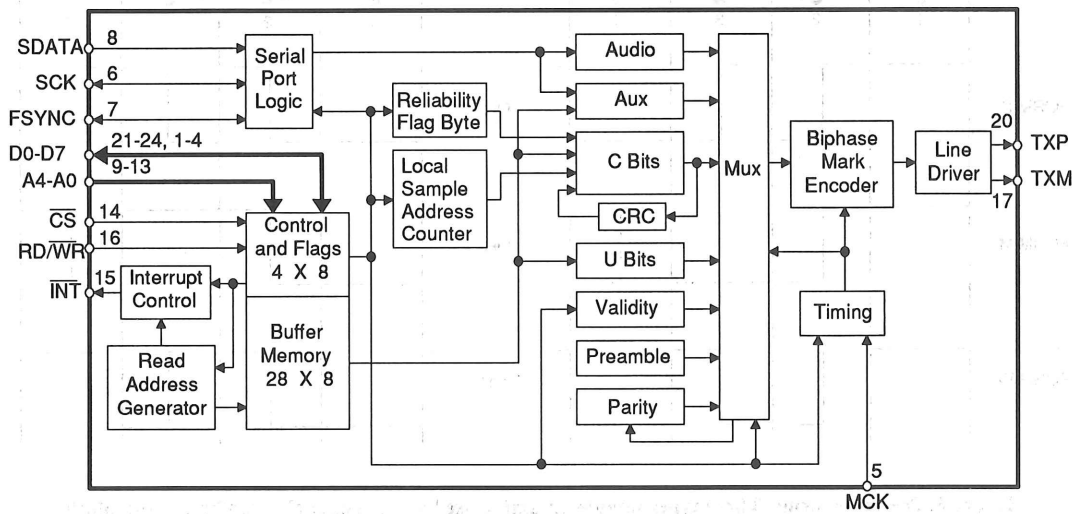
**Figure 5. Channel Coding**



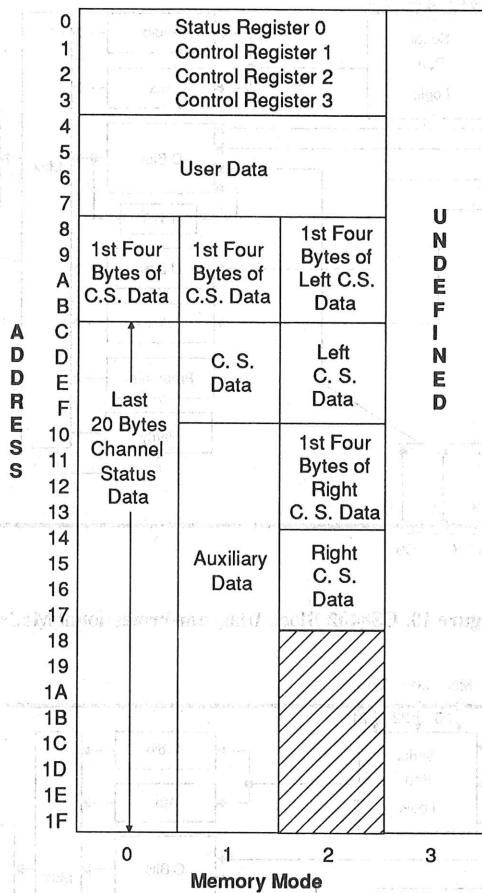
**Figure 6. Preamble forms. Three types sample preamble used are B) channel 1, subframe, and block synchronizing; M) channel 1, otherwise; W) channel 2.**



**Figure 7. General Description**



**Figure 8. CS8401 Block Diagram**



**Figure 9. CS8401 Buffer Memory Modes**

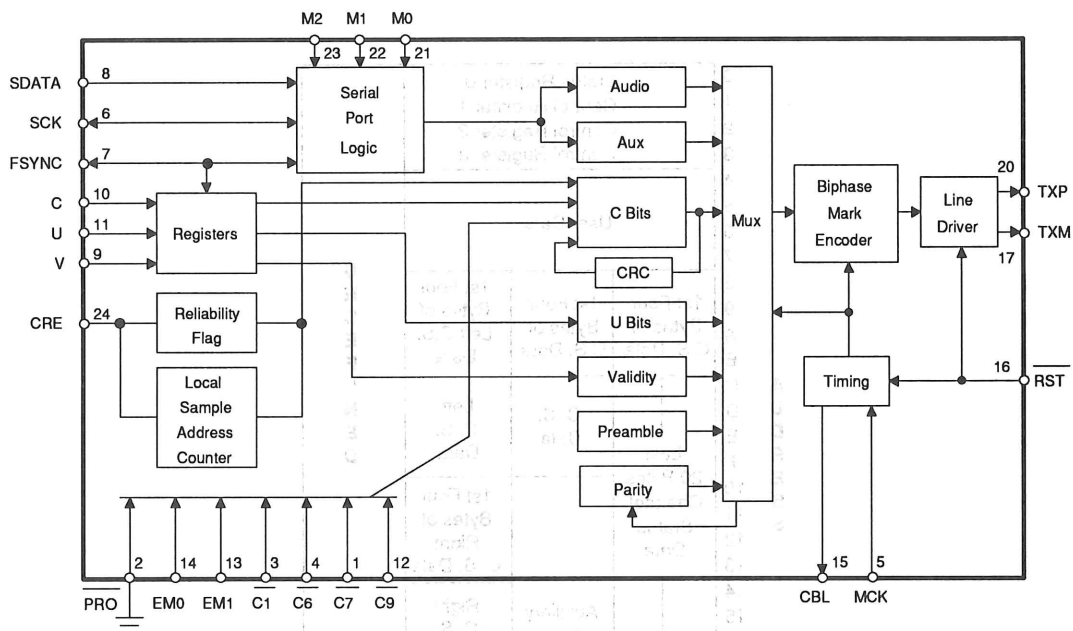


Figure 10. CS8402 Block Diagram-Professional Mode

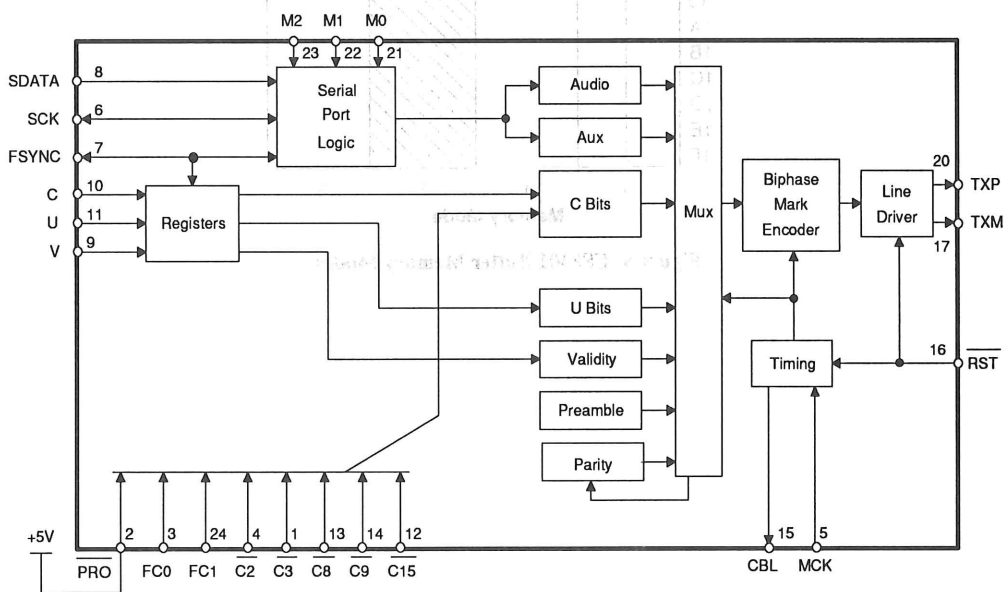


Figure 11. CS8402 Block Diagram-Consumer Mode

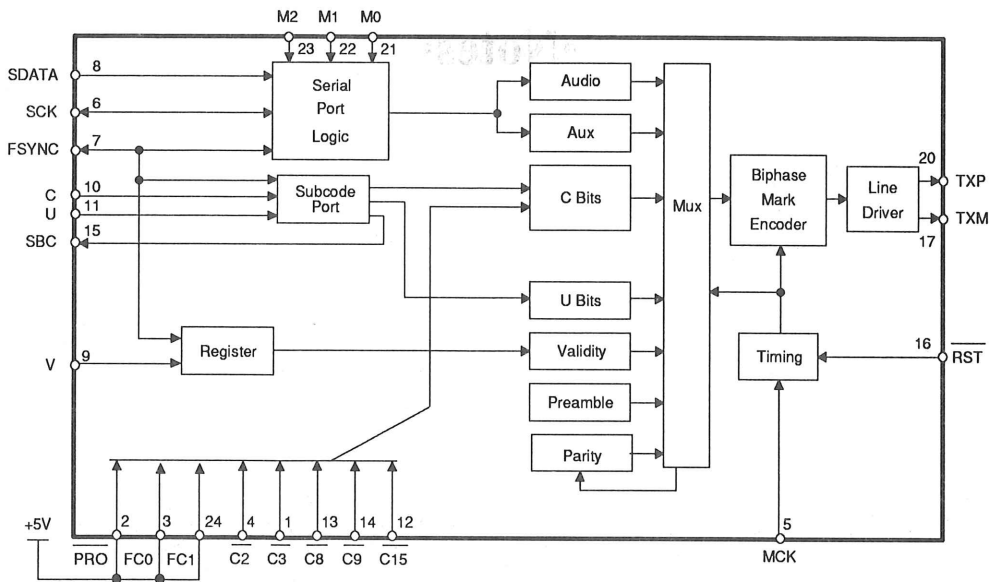


Figure 12. CS8402 Block Diagram-Consumer Mode, CD Submode

DATA BUS BIT 4	D4	1	24	D3	DATA BUS BIT 3
DATA BUS BIT 5	D5	2	23	D2	DATA BUS BIT 2
DATA BUS BIT 6	D6	3	22	D1	DATA BUS BIT 1
DATA BUS BIT 7	D7	4	21	D0	DATA BUS BIT 0
MASTER CLOCK	MCK	5	20	TXP	TRANSMIT POSITIVE
SERIAL DATA CLOCK	SCK	6	19	VD+	POWER
FRAME SYNC	FSYNC	7	18	GND	GROUND
SERIAL INPUT DATA	SDATA	8	17	TXN	TRANSMIT NEGATIVE
ADDRESS BUS BIT 4	A4	9	16	RD/WR	READ/WRITE SELECT
ADDRESS BUS BIT 3	A3	10	15	INT	INTERRUPT
ADDRESS BUS BIT 2	A2	11	14	CS	CHIP SELECT
ADDRESS BUS BIT 1	A1	12	13	A0	ADDRESS BUS BIT 0

Figure 13. CS8401 Pinout

CS BIT 7 / CS BIT 3	C7/C3	1	24	TST/FC1	SAMPLE ADDR. / FREQ. CTRL 1
PROFESSIONAL MODE	PRO	2	23	M2	SERIAL PORT MODE SELECT 2
CS BIT 1 / FREQ. CTRL. 0	C1/FC0	3	22	M1	SERIAL PORT MODE SELECT 1
CS BIT 6 / CS BIT 2	C6/C2	4	21	M0	SERIAL PORT MODE SELECT 0
MASTER CLOCK	MCK	5	20	TXP	TRANSMIT POSITIVE
SERIAL DATA CLOCK	SCK	6	19	VD+	POWER
FRAME SYNC	FSYNC	7	18	GND	GROUND
SERIAL INPUT DATA	SDATA	8	17	TXN	TRANSMIT NEGATIVE
VALIDITY INPUT	V	9	16	RST	MASTER RESET
CS SERIAL IN / SC FRAME CLOCK	C/SBF	10	15	CBL/SBC	CS BLOCK OUT / SC BIT CLOCK
USER DATA INPUT	U	11	14	EM0/C9	EMPHASIS 0 / CS BIT 9
CS BIT 9 / CS BIT 15	C9/C15	12	13	EM1/C8	EMPHASIS 1 / CS BIT 8

Figure 14. CS8402 Pinout

## •Notes•

## Application Note

# Overview of Digital Audio Interface Data Structures

Clif Sanchez & Roger Taylor



The following information is provided for convenience, but by no means constitutes the entire specification. Also included is information from the IEC 958 and the new AES3-199x and TC84 documents. The AES3-199x and TC84 documents have not received approval as of the printing of this data sheet. To guarantee conformance, a copy of the actual specification should be obtained from the Audio Engineering Society or ANSI (ANSI S4.40-1985) for the AES3 document, and the International Electrotechnical Commission for the IEC 958 document.

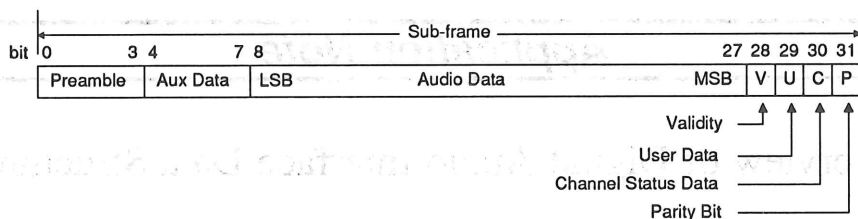
The AES/EBU interface is a means for serially communicating digital audio data through a single transmission line. It provides two channels for audio data, a method for communicating control information, and some error detection capabilities. The

control information is transmitted as one bit per sample and accumulates in a block structure. The data is biphasse encoded, which enables the receiver to extract a clock from the data. Coding violations, defined as preambles, are used to identify sample and block boundaries.

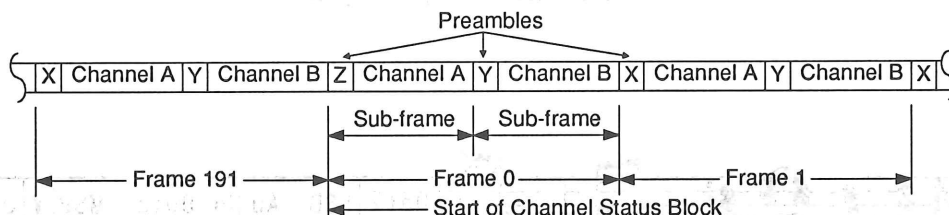
### Frames Sub-frames and Blocks

An audio sample is placed in a structure known as a sub-frame. The sub-frame, shown in Figure 1, consists of 4 bits of preamble, 4 bits of auxiliary data, 20 bits of audio data, 3 bits called validity, user, and channel status, and a parity bit. The preamble contains biphasse coding violations and identifies the start of a sub-frame. The audio sample word length can vary up to 24 bits and is transmitted LSB first. If the word length is greater than 20 bits, the sample occupies both the audio





**Figure 1. Sub-frame Format**



**Figure 2. Frame/Block Format**

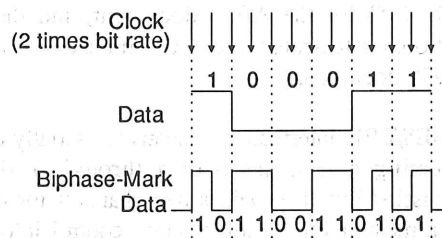
and auxiliary data fields. If it is 20 bits or less, the auxiliary field can be used for other applications such as voice. The parity bit generates even parity and can detect an odd number of transmission errors in the sub-frame. The validity bit, when low, indicates the audio sample is fit for conversion to analog. The user and channel status bits are sent once per sample and, when accumulated over a number of samples, define a block of data. The user bit channel is undefined and available to the user for any purpose. The channel status bit conveys, over an entire block, important information about the audio data and transmission link. Each of the two audio channels has its own channel status data with a block structure that repeats every 192 samples.

As shown in Figure 2, two consecutive sub-frames are defined as a frame, containing channels A and B, and 192 frames define a block. The preambles that identify the start of a sub-frame are different for each of the two channels with another unique one identifying the beginning of a channel status block.

### Modulation and Preambles

The data is transmitted with biphasemark encoding to minimize the DC component and to allow clock recovery from the data. As illustrated in Figure 3, the 1's in the data have transitions in the center, and the 0's do not, after biphasemark encoding. Also, the biphasemark data switches polarity at every data bit boundary. Since the value of the data bit is determined by whether there is a transition in the center of the bit, the actual polarity of the signal is irrelevant.

Each sub-frame starts with a preamble. This allows a receiver to lock on to the data within one sub-frame. There are three defined preambles:



**Figure 3. Biphasemark Encoding**

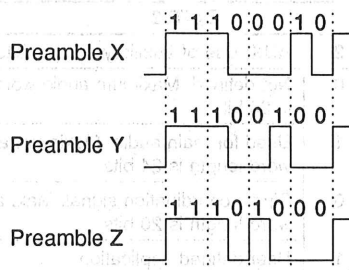
	Biphase Patterns	Channel
X	11100010 or 00011101	Ch. A
Y	11100100 or 00011011	Ch. B
Z	11101000 or 00010111	Ch. A & C.S. Block Start

**Table 1. Preambles**

one for each channel and one to indicate the beginning of a channel status block (which is also channel A). To distinguish the preambles from arbitrary data patterns, the preambles contain two biphase-mark violations. Biphase-mark data is required to transition at every bit period, but each preamble violates that requirement twice. In Figure 3 each bit boundary, indicated by the dashed lines, contains a transition in the biphase data. Each preamble shown in Figure 4 has two bit boundaries with no transition, which

BYTE 0	
bit 0	PRO = 1
0	Consumer use of channel status block
1	Professional use of channel status block
bit 1	Audio
0	Normal Audio
1	Non-Audio
bits 2 3 4	Encoded audio signal emphasis
0 0 0	Emphasis not indicated. Receiver defaults to no emphasis with manual override enabled
1 0 0	None. Rec. manual override disabled
1 1 0	50/15 $\mu$ S. Rec. manual override disabled
1 1 1	CCITT J.17. Rec. man. override disabled
X X X	All other states of bits 2-4 are reserved
bit 5	Lock: Source Sample Frequency
0	Locked - default
1	Unlocked
bits 6 7	Fs: Sample Frequency
0 0	Not indicated. Receiver default to 48 kHz and manual override or auto set enabled
0 1	48 kHz. Man. override or auto disabled
1 0	44.1 kHz. Man. override or auto disabled
1 1	32 kHz. Man. override or auto disabled

**Table 2. Professional Channel Status bytes 0-1**



**Figure 4. Preamble Forms**

enables the receiver to recognize the data as a preamble. Table 1 lists the preamble biphase-mark data patterns and what each designates. Since biphase-mark encoding is not polarity conscious, both phases are shown in the table. Preambles "X" and "Y" indicate a sub-frame containing channels A and B respectively. Preamble "Z" replaces preamble "X" once every

BYTE 1	
bits 0 1 2 3	Channel Mode
0 0 0 0	Mode not indicated. Receiver default to 2-channel mode. Manual override enabled
0 0 0 1	Two-channels. Man. override disabled
0 0 1 0	Single channel. Man. override disabled
0 0 1 1	Primary/Secondary (Ch. A is primary). Manual override disabled
0 1 0 0	Stereophonic. (Ch. A is left) Manual override disabled.
0 1 0 1	Reserved for user defined applications
0 1 1 0	Reserved for user defined applications
1 1 1 1	Vector to byte 3. Reserved
X X X X	All other states of bits 0-3 are reserved.
bits 4 5 6 7	User bits management
0 0 0 0	Default, no user info indicated
0 0 0 1	192 bit block structure Preamble 'Z' starts block
0 0 1 0	Reserved
0 0 1 1	User defined application
X X X X	All other states of bits 4-7 are reserved.

BYTE 2		
bits 0 1 2	AUX: Use of auxiliary sample bits	
0 0 0	Not defined. Maximum audio word length is 20 bits	
0 0 1	Used for main audio. Maximum audio word length is 24 bits	
0 1 0	Single coordination signal. Max. audio word length is 20 bits	
0 1 1	User defined application	
X X X	All other states of bits 0-2 are reserved	
bits 3 4 5	Source word length Max. audio based on bits 0-2 above	
	Max audio 24 bits	Max audio 20 bits
0 0 0	Not Indicated	Not Indicated (default)
0 0 1	23 bits	19 bits
0 1 0	22 bits	18 bits
0 1 1	21 bits	17 bits
1 0 0	20 bits	16 bits
1 0 1	24 bits	20 bits
X X X	All other states of bits 3-5 are reserved	
bits 6 7		
X X	Reserved	

BYTE 3	
bits 0-7	Vectored target byte
XXXXXXXX	Reserved

BYTE 4	
bits 0 1	Digital audio reference signal per AES11-1990
0 0	Not reference signal (default)
0 1	Grade 1 reference signal
1 0	Grade 2 reference signal
1 1	Reserved
bits 2-7	
XXXXXX	Reserved

BYTE 5	
bits 0-7	
XXXXXXXX	Reserved

BYTES 6 - 9	
Alphanumeric channel origin data	
7-bit ISO 646 (ASCII) data with odd parity bit. First character in message is byte 6. LSB's are transmitted first.	

BYTES 10 - 13	
Alphanumeric channel destination data	
7-bit ISO 646 (ASCII) data with odd parity bit. First character in message is byte 10. LSB's are transmitted first.	

BYTES 14 - 17	
Local sample address code (32-bit binary)	
Value is of first sample of current block. LSBs are transmitted first.	

BYTES 18 - 21	
Time-of-day sample address code (32-bit binary)	
Value is of first sample of current block. LSBs are transmitted first.	

BYTE 22	
bits 0 1 2 3	
X X X X	Reserved
bit 4	Channel status bytes 0 to 5
0	Reliable
1	Unreliable
bit 5	Channel status bytes 6 to 13
0	Reliable
1	Unreliable
bit 6	Channel status bytes 14 to 17
0	Reliable
1	Unreliable
bit 7	Channel status bytes 18 to 21
0	Reliable
1	Unreliable

BYTE 23	
CRCC: Cyclic redundancy check character	
CRCC for channel status data block that uses bytes 0 to 22 inclusive. Generating polynomial is	
$G(x) = X^8 + X^4 + X^3 + X^2 + 1$	
with an initial state of all ones.	

Table 3. Professional Channel Status Bytes 2-23

192 frames to indicate the start of a channel status block.

There are two channel status blocks, one for channel A and one for channel B. Since there are 192 frames in a block, each channel has a channel status block 192 bits long. These 192 channel status bits in a block can be arranged as 24 bytes. The blocks have one of two formats, professional or consumer. The first bit of the channel status block defines the format with 0 indicating consumer and 1 indicating professional.

### Channel Status Block - Professional Format

Setting the first bit of channel status high designates the professional or broadcast format. The channel status block structure for the professional format is illustrated in Figure 5 and shows bit 0 of byte 0, PRO, to contain a one. Tables 2 and 3 list the bits in each byte and their meaning. The areas designated "reserved" in the figures and tables, are currently not specified and must be set to 0 when transmitting. Most of the professional format data was obtained from the AES3-1985 document, and information from AES3-199x. Since the AES specification is currently being updated, the accuracy of this data is not guaranteed.

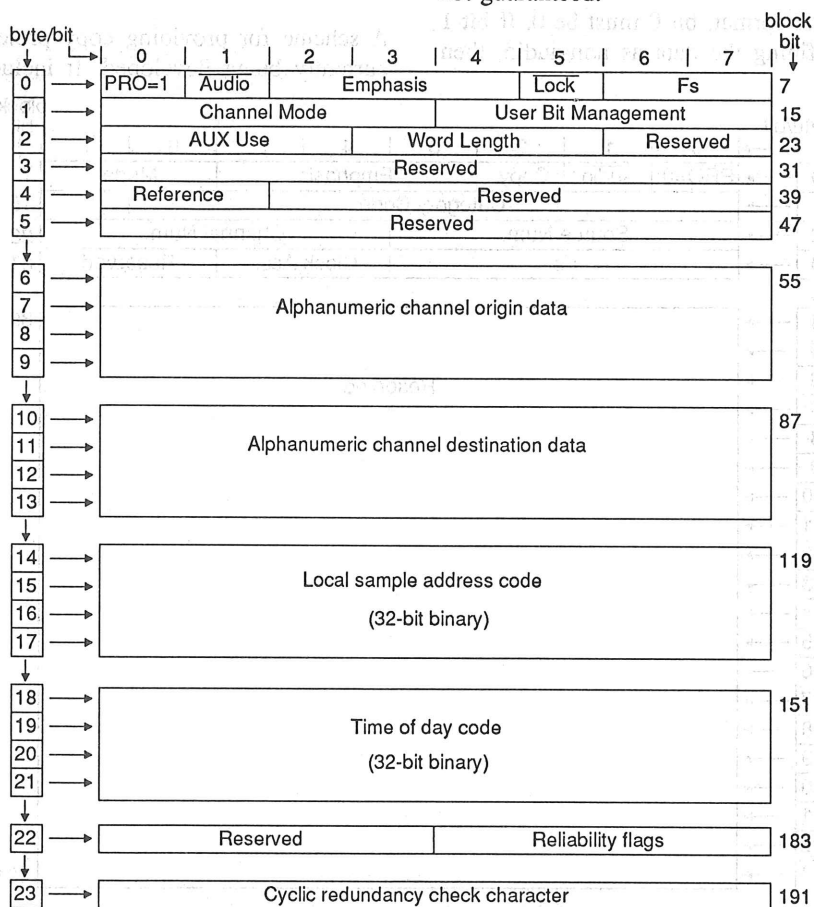


Figure 5. Professional Channel Status Block Structure

### Channel Status Block - Consumer Format

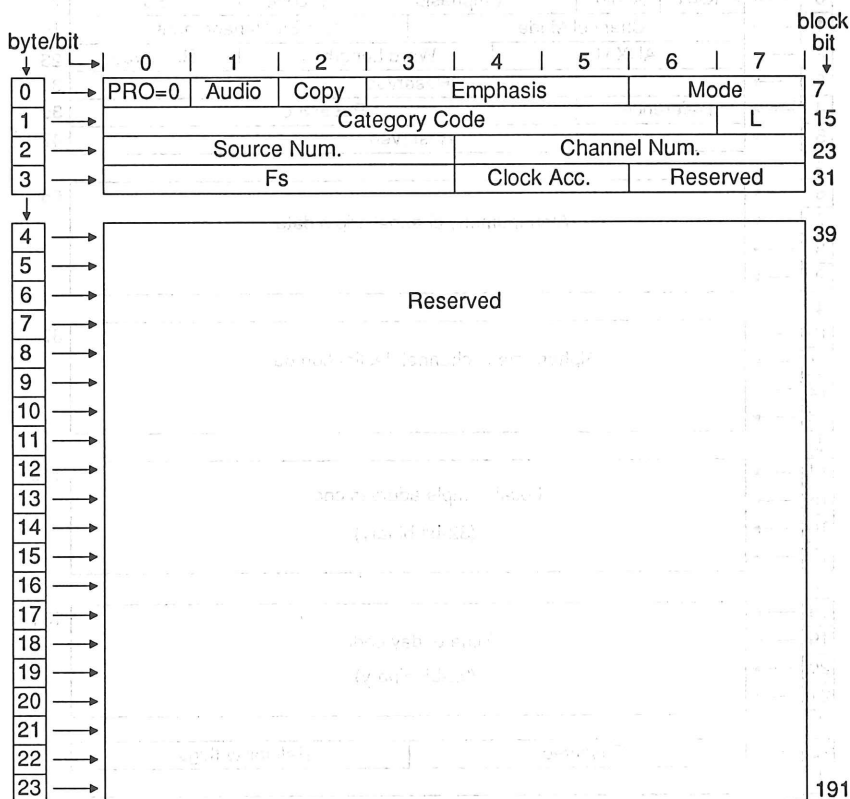
Setting the first bit of channel status low designates the consumer format. The channel status block structure for the consumer format is illustrated in Figure 6 with the bit descriptions in Tables 4 and 5. All areas listed as "reserved" must be transmitted as a 0. The data for this format was obtained from the EIAJ CP-340 and the IEC 958 with some information from TC84 which is a proposed amendment to IEC 958 and has not received approval yet. As with the professional format, since this format is currently changing, the accuracy of the data listed cannot be guaranteed.

In the consumer format, bit 0 must be 0. If bit 1 is set to 1 defining the data as non-audio, then

bits 3-5 are redefined (see Table 4, byte 0). Bits 6 and 7 of byte 0 define the mode, and only one mode is presently defined, mode = 00. This mode defines the next three bytes as listed in Figure 6. Most of byte 1 defines the category code. The first 3 to 5 bits define the general category. Under the laser-optical category is compact disk (cat. code 1000000). This format defines some of the U channel bits and the CD subcode port. More information can be obtained from the CP-340 or IEC 958 documents.

Currently the standards committees are trying to define a minimum implementation as well as levels of implementation of channel status data.

A scheme for providing copy protection is also currently being developed. It includes knowing



**Figure 6. Consumer Channel Status Block Structure**

BYTE 0	
bit 0	PRO = 0 (consumer)
0	Consumer use of channel status block
1	Professional use of channel status block
bit 1	Audio
0	Digital Audio
1	Non-audio
bit 2	Copy / Copyright
0	Copy inhibited / copyright asserted
1	Copy permitted / copyright not asserted
bits 3 4 5	Pre-emphasis - if bit 1 is 0 (dig. audio)
0 0 0	None - 2 channel audio
1 0 0	50/15 $\mu$ s - 2 channel audio
0 1 0	Reserved - 2 channel audio
1 1 0	Reserved - 2 channel audio
X X 1	Reserved - 4 channel audio
bits 3 4 5	if bit 1 is 1 (non-audio)
0 0 0	Digital data
X X X	All other states of bits 3-5 are reserved
bits 6 7	Mode
0 0	Mode 0 (defines bytes 1-3)
X X	All other states of bits 6-7 are reserved

BYTE 1 - Category Code 001	
bits 3 4 5 6	Broadcast reception of digital audio
* 0 0 0 0	Japan
* 0 0 1 1	United States
* 1 0 0 0	Europe
* 0 0 0 1	Electronic software delivery
X X X X	All other states are reserved

BYTE 1 - Category Code 100	
bits 3 4 5 6	Laser Optical
0 0 0 0	CD - compatible with IEC-908
* 1 0 0 0	CD - not comp. with IEC-908 (magneto-optical)
X X X X	All other states are reserved

BYTE 1	
bits 0 1 2 3	4 5 6 Category Code
0 0 0 0	0 0 0 General
* 0 0 0 1	0 0 1 Experimental
	X X X Reserved
* 0 0 1 0	X X X Solid state memory
* 0 0 1 1	X X X Broadcast recep. of digital audio
0 1 0 X	X X X Digital/digital converters
* 0 1 1 0	0 X X A/D converters w/o copyright
* 0 1 1 1	1 X X A/D converters w/ copyright (using Copy and L bits)
* 0 1 1 1	X X X Broadcast recep. of digital audio
1 0 0 X	X X X Laser-optical
* 1 0 1 X	X X X Musical Instruments, mics, etc.
1 1 0 X	X X X Magnetic tape or disk
1 1 1 X	X X X Reserved
bit 7	L: Generation Status.
	Only category codes: 001XXXX, 0111XXX, 100XXXX
* 0	Original/Commercially pre-recorded data
* 1	No indication or 1st generation or higher
	All other category codes
* 0	No indication or 1st generation or higher
* 1	Original/Commercially pre-recorded data

The subgroups under the category code groups listed above are described in tables below. Those not listed are reserved.

The Copy and L bits form a copy protection scheme for original works. Further explanations can be found in the proposed amendment (TC84) to IEC-958.

BYTE 1 - Category Code 010	
bits 3 4 5 6	Digital/digital conv. & signal processing
0 0 0 0	PCM encoder/decoder
* 0 0 1 0	Digital sound sampler
* 0 1 0 0	Digital signal mixer
* 1 1 0 0	Sample-rate converter
X X X X	All other states are reserved

Table 4. Consumer Channel Status Bytes 0 and 1

BYTE 1 - Category Code 101					
bits	3	4	5	6	Musical Instruments, mics, etc.
*	0	0	0	0	Synthesizer
*	1	0	0	0	Microphone
	X	X	X	X	All other states are reserved

BYTE 1 - Category Code 110					
bits	3	4	5	6	Magnetic tape or disk
	0	0	0	0	DAT
*	1	0	0	0	Digital audio sound VCR
	X	X	X	X	All other states are reserved

BYTE 2					
bit	0	1	2	3	Source Number
	0	0	0	0	Unspecified
	1	0	0	0	1
	0	1	0	0	2
	1	1	0	0	3
	0	0	1	0	4 to
	0	1	1	1	14 (binary - 0 is LSB, 3 is MSB)
	1	1	1	1	15
bit	4	5	6	7	Channel Number
	0	0	0	0	Unspecified
	1	0	0	0	A (Left in 2 channel format)
	0	1	0	0	B (Right in 2 channel format)
	1	1	0	0	C to
	0	1	1	1	N (binary - 4 is LSB, 7 is MSB)
	1	1	1	1	O

BYTE 3					
bits	0	1	2	3	Fs: Sample Frequency
	0	0	0	0	44.1 kHz
	0	1	0	0	48 kHz
	1	1	0	0	32 kHz
	X	X	X	X	All other states of bits 0-3 are reserved
bits	4	5	Clock Accuracy		
	0	0	Level II, $\pm 1000$ ppm (default)		
	0	1	Level III, variable pitch		
	1	0	Level I, $\pm 50$ ppm - high accuracy		
	1	1	Reserved		
bits	6	7			
	X	X	Reserved		

BYTES 4 - 23					
Reserved					

\* - Data from draft of IEC 958 proposed amendment (from TC84). Has not received approval yet.

Table 5. Consumer Channel Status Bytes 1-23

the category code and then utilizing the Copy and L bits to determine if a copy should be allowed. Digital processing of data should pass through the copy and L bits as defined by their particular category code. If mixing inputs, the highest level of protection of any one of the sources should be passed through. If the copy bit indicates no copy protection (copy = 1), then multiple copies can be made. If recording audio data to tape or disk, and any source has copy protection asserted, then the L bit must be used to determine whether the data can be recorded.

The L bit determines whether the source is an original (or prerecorded) work, or is a copy of an original work (first generation or higher). The actual meaning of the L bit can only be determined by looking at the category code since certain category codes reverse the meaning.

If the category code is CD (1000000) and the copy bit alternates at a 4 to 10 Hz rate, the CD is a copy of an original work that has copy protection asserted and no recording is permitted.

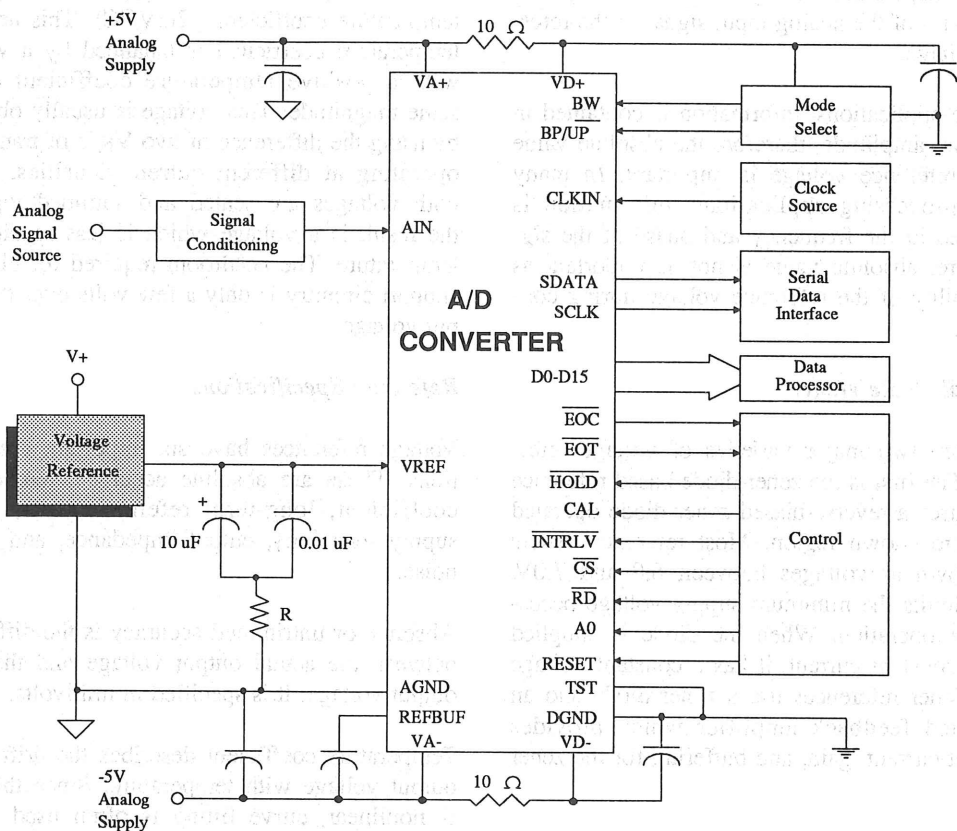


## Application Note

### Voltage References for the CS5012 / CS5014 / CS5016 / CS5101/ CS5102 / CS5126 Series of A/D converters

by

Bruce Del Signore & Steven Harris





## INTRODUCTION

This application note discusses voltage references for use with Crystal Semiconductor's successive approximation series of A/D converters. Reference design considerations, a design example and suggested reference circuits are explained in detail.

Voltage references provide accurate voltages for use in data acquisition systems in order to establish a basis for conversion. In a data acquisition system, the value of the reference sets the gain of the A/D stage since the digital output corresponds to the ratio of the analog input signal to the reference voltage.

In static applications, information is contained in the signal amplitude, therefore the absolute value of the reference voltage is important. In many signal processing applications, information is contained in the frequency and phase of the signal. Here, absolute value is not as important as the stability of the reference voltage during conversion.

### *Zener-diode Reference*

There are two major varieties of voltage references. The first is the zener-diode based reference which uses a reverse-biased zener diode operated in its breakdown region. Most reference zeners breakdown at voltages between 6.0 and 7.0V, which limits the minimum supply voltage necessary for operation. When the diode is supplied with a constant current, it has a constant voltage drop. Zener references use a zener diode and an integrated feedback amplifier which provides constant current, gain, and buffering for the zener diode.

Zener diodes exhibit two types of breakdown. The first is zener breakdown which has a negative temperature coefficient and is dominant at low current levels. The second, avalanche breakdown, occurs at higher current levels and has a

positive temperature coefficient. At some specific current level, these two effects cancel each other and the temperature coefficient of the zener breakdown voltage is zero. As the ambient temperature changes, one of the breakdown mechanisms becomes dominant and the the reverse-biased diode voltage will exhibit a temperature coefficient.

### *Bandgap Reference*

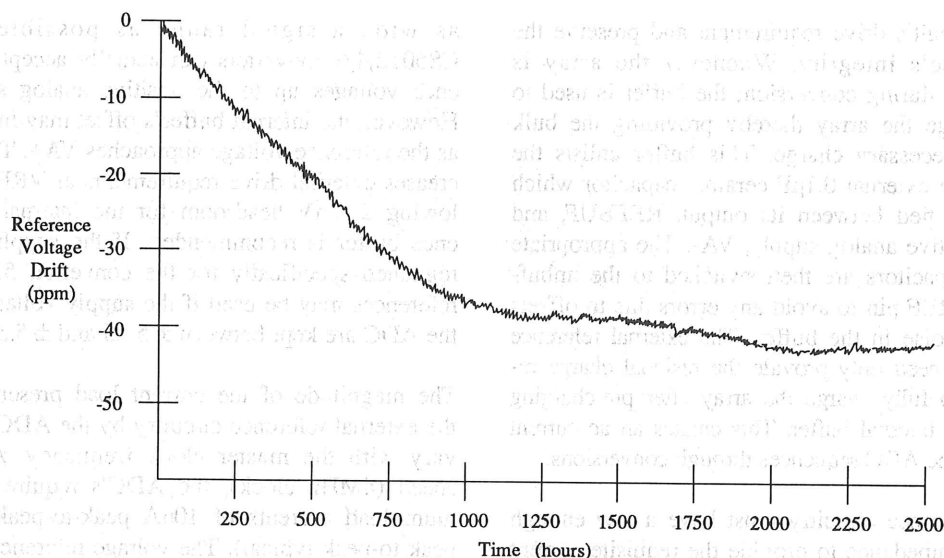
The second major type of reference is the bandgap reference. This reference uses the base-emitter voltage ( $V_{be}$ ) of a bipolar transistor as a basis for operation. The  $V_{be}$  has a negative temperature coefficient ( $-2\text{mV}/^\circ\text{C}$ ). This negative temperature coefficient is balanced by a voltage with a positive temperature coefficient of the same magnitude. This voltage is usually obtained by using the difference of two  $V_{be}$ 's of transistors operating at different current densities. When both voltages are scaled and summed together, the result is a voltage which is less sensitive to temperature. The headroom required for bias and support circuitry is only a few volts over the output voltage.

### *Reference Specifications*

Voltage references have six important specifications. These are absolute accuracy, temperature coefficient, long-term reference drift, power supply sensitivity, output impedance, and output noise.

Absolute or untrimmed accuracy is the difference between the actual output voltage and the ideal output voltage. It is specified in millivolts.

Temperature coefficient describes the drift in the output voltage with temperature. Since this drift is nonlinear, curve fitting is often used for all temperatures between those actually tested. Voltage references are available with temperature coefficients as low as  $1\text{ ppm}/^\circ\text{C}$ . Inexpensive references are available with 10 to  $50\text{ ppm}/^\circ\text{C}$  drift which is comparable to on-chip references of



**Figure 1. - Long Term Stability of a Typical Zener Reference**

bipolar A/D converters. Temperature coefficient is specified in ppm/°C.

Long term stability is the drift in the reference voltage over time. Most references show minor deviations in voltage due to 1/f noise in circuit components. These deviations are usually small and are superimposed on a larger drift characteristic which is due to device aging. An example of this is seen in Figure 1. Long term drift is specified in ppm/1000 hrs.

Power supply sensitivity (line regulation) is the change in output voltage due to a change in power supply. Most references have good power supply rejection at dc, but ac power supply rejection is also important when power supplies are subject to high frequency coupling or noise spikes. PSRR (Power Supply Rejection Ratio) is the ratio of the change in power supply to the change in output voltage. It is specified in dB.

Output impedance is important because of the dynamic loads generated by successive-approximation A/D converters. When the reference is sourcing or sinking current, its output voltage

will change due to non-zero output impedance. This impedance must be low enough at all frequencies of interest so the deviation in reference voltage when sourcing current is negligible. Output impedance is specified in ohms.

Output noise can lead to comparison errors in the A/D converter, and subsequently conversion errors. Reference noise is more evident with full scale inputs. It is specified in  $\mu\text{V}$  peak-to-peak.

### Design Considerations

When interfacing a voltage reference to an A/D converter, the specifications should be robust enough so that the reference does not become a source of conversion error. During conversion, each capacitor of the calibrated capacitor array in the ADC is switched between VREF and AGND in a manner determined by the successive approximation algorithm. The charging and discharging of the array results in a current load at the reference. The ADC's include an internal buffer amplifier to minimize the external refer-

ence circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. This buffer enlists the aid of an external 0.1 $\mu$ F ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer. The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the internal buffer. This creates an ac current load as the ADC sequences through conversions.

The reference circuitry must have a low enough output impedance to provide the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Also with CS5012,4,6 converters, bits are converted at a 1MHz rate with a full speed (4MHz) clock. The reference must settle within one microsecond so that it will be accurate before the next bit is converted. Signal amplitude dependent loading and conversion settling time require the output impedance of the reference to remain low from dc to at least 1MHz in order to ensure good converter performance.

The CS5012,4,6 series of converters can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using

as wide a signal range as possible. All CS5012,4,6 converters can actually accept reference voltages up to the positive analog supply. However, the internal buffer's offset may increase as the reference voltage approaches VA+. This increases external drive requirements at VREF. Allowing 250mV headroom for the internal reference buffer is recommended. If the supplies are regulated specifically for the converter, 5.0 volt references may be used if the supply voltages for the ADC are kept between  $\pm 5.25$  and  $\pm 5.5$  volts.

The magnitude of the current load presented to the external reference circuitry by the ADC's will vary with the master clock frequency. At full speed (4MHz clock), the ADC's require maximum load currents of 10 $\mu$ A peak-to-peak (1 $\mu$ A peak-to-peak typical). The voltage reference must supply this current and maintain adequate voltage regulation. The load currents scale proportionately with the master clock frequency. Slower clocks can be used to relax maximum output impedance specification of the reference.

When driving multiple A/D converters from the same reference circuit, load currents will scale proportionally to the number of converters. Distribute the required decoupling components such that each ADC is locally decoupled.

A reference with a maximum output impedance of 2  $\Omega$  will yield a maximum error of 20 $\mu$ V. This reference could drive a CS5016 (LSB=69 $\mu$ V with a 4.5V reference) and maintain approximately

Part # \ f <sub>clk</sub>	4MHz	2MHz	1MHz	500kHz
CS5012 (Vref=4.5V)	27	54	108	216
CS5012 (Vref=2.5V)	15	30	60	120
CS5014 (Vref=4.5V)	7	14	28	56
CS5016 (Vref=4.5V)	2	4	8	16

All units  
in ohms

Table 1. - Maximum Output Impedance for  $\approx 1/4$  LSB Reference Deviation

1/4 LSB deviation during conversion. Similarly for the CS5014 (LSB=276 $\mu$ V with a 4.5V reference), and CS5012 (LSB=613 $\mu$ V with a 2.5V reference), maximum impedances of 7 and 15  $\Omega$  respectively will maintain adequate regulation. Table 1 defines maximum reference impedances allowed for each of the Crystal A/D's operating at different master clock frequencies in order to keep reference deviation approximately equal to 1/4 LSB.

All precision references exhibit extremely low output impedance at dc. However, as frequency increases the impedance also increases. A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum where the reference impedance is too high.

For example, the impedance of an ideal 10 $\mu$ F capacitor drops below 1  $\Omega$  at frequencies greater than 16kHz. However, actual capacitors behave differently due to their physical structure. Tantalum-foil electrolytic capacitors begin to appear inductive at frequencies around 100kHz and as a result their impedance begins to rise at frequencies above this. Aluminum electrolytic capacitors appear inductive at frequencies around 10kHz. Ceramic-disk capacitors behave much closer to ideal and begin to appear inductive at frequencies around 5MHz, but 10 $\mu$ F ceramic-disk capacitors are quite rare. Therefore, a high-quality tantalum capacitor (10 $\mu$ F) in parallel with a smaller

(0.1 $\mu$ F) ceramic capacitor is recommended. This combination yields low impedance up to frequencies around 50MHz.

### Peaking

The presence of large capacitors on the output of some voltage references may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to reduce it.

Most commercially available references use an integrated op-amp to buffer the actual reference generator. External capacitive loading will degrade performance of this op-amp. This degradation can be analyzed using classical analysis techniques. The open loop gain of an ideal op-amp is primarily determined by the internal compensation capacitor which generates a left-half-plane-pole (LHPP) at a very low frequency. The effect of this pole is to reduce the open loop gain by 20dB per decade and to add a -90 degree phase shift to the open loop transfer characteristic. Adding a capacitive load to the output of the op-amp generates another LHPP at a frequency inversely proportional to the capacitor's value. An additional 20dB per decade reduction in gain and -90 degree phase shift result from the second LHPP.

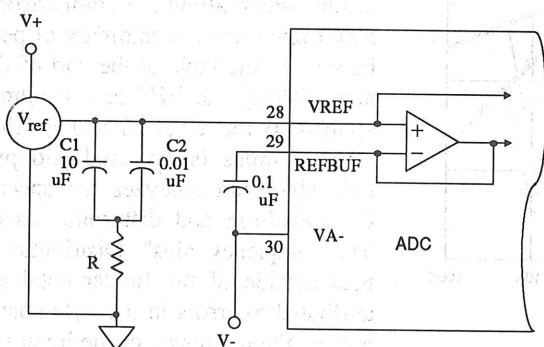


Figure 2. - Reference Connections

$$R = \frac{1}{2\pi(C_1 + C_2)f_{peak}}$$

The unity gain bandwidth of an op-amp ( $f_0$ ), is the frequency at which the open loop gain goes to unity. If the total phase shift reaches  $-180$  degrees before  $f_0$  is reached the op-amp will become unstable. The closed loop frequency response peaks at  $f_0$ . As the total open loop phase shift at  $f_0$  approaches  $-180$  degrees, the closed loop peak at  $f_0$  approaches infinity. The point of critical damping is the point where the peaking is precisely zero. Any phase shift less than this results in no peaking, and phase shift greater than this results in increased peaking.

Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 2). This resistor adds a left-half-plane-zero (LHPZ) to the open loop characteristic of the op-amp. This zero increases the gain by 20dB per decade, and adds a  $+90$  degree phase shift. The resulting reduction in total phase shift at  $f_0$  reduces peaking in the closed loop characteristic. The equation in Figure 2 can be used to help calculate the optimum value of R for a particular reference. The term " $f_{\text{peak}}$ " is the frequency of the peak in the output impedance of the reference before the resistor is added.

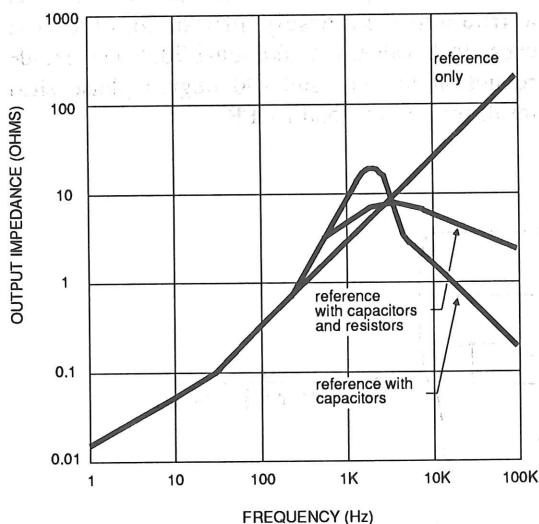


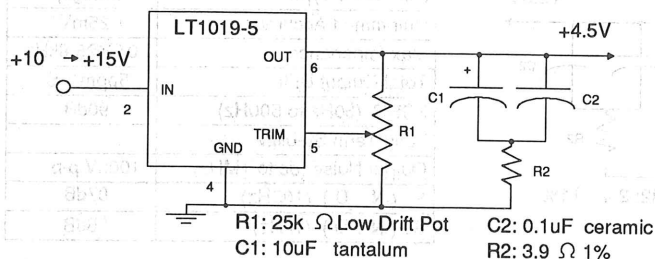
Figure 3. - Output Impedance Curves for LT1019-5

### Design Example

Figure 3 shows the output impedance characteristic of an LT1019-5 reference trimmed to 4.5V. The three curves represent impedances of the stand-alone reference, the reference with a  $10\mu\text{F}$  tantalum and a  $0.1\mu\text{F}$  ceramic capacitor added in parallel to the output, and the reference with the capacitors and a  $2.2\Omega$  resistor in series with them (See Figure 2). Without loading, the reference impedance rises above  $100\Omega$  at 50kHz. Adding the capacitors, peaking can be seen, but the maximum impedance is about  $13\Omega$  at 4kHz. As shown in Table 1,  $13\Omega$  is sufficient for use with the 12-bit converters and for the 14 and 16-bit converters with slow master clocks. With the addition of the  $2.2\Omega$  resistor, the peak is reduced to  $6\Omega$  and the impedance approaches  $2.2\Omega$  at high frequencies.

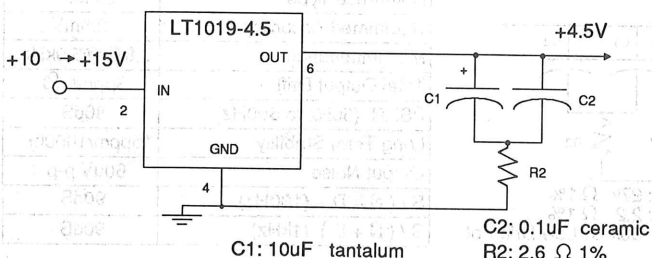
### Suggested Voltage Reference Circuits

Nine reference circuits were characterized for use with the CS5012, CS5014, CS5016, CS5101, CS5102, CS5126 family of successive-approximation A/D converters. Important reference specifications such as output impedance and drift were measured for all references using standard test techniques. In addition, a Fast-Fourier Transform (FFT) test was performed to characterize the total dynamic performance of each reference circuit while driving a CS5016 converter. The same CS5016 was used for all tests yielding results which allow the comparison between different references. A summary of performance can be seen in the table at the end of this application note. During the FFT test, a pure sine wave is applied to the CS5016 and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the waveform and distributes its energy among 512 "frequency bins". Distribution of energy in bins outside of the fundamental and dc can be attributed to errors in the A/D converter's performance, the reference, or the input sine wave.



Reference Type	Bandgap
Untrimmed Accuracy	2.5mV
Max Impedance	6.5 $\Omega$ @3.2kHz
Total Output Drift	5ppm/ $^{\circ}$ C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	250uV p-p
S / ( N + D ) (100Hz)	89dB
S / ( N + D ) (1kHz)	89dB

Figure 4. LT1019-5 Reference Trimmable to 4.5V



Reference Type	Bandgap
Untrimmed Accuracy	3.0mV
Max Impedance	3.1 $\Omega$ @6.1kHz
Total Output Drift	5ppm/ $^{\circ}$ C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	150uV p-p
S / ( N + D ) (100Hz)	91dB
S / ( N + D ) (1kHz)	90dB

Figure 5. LT1019-4.5 Reference

The result of the FFT test is the ratio of input signal amplitude to the combination of harmonic distortion and total integrated noise. It is referred to as  $S/(N+D)$  in all of the performance charts in Figures 4 to 10. This ratio is expressed in dB. If input sine wave distortion and the actual A/D converter's distortion and noise are assumed to be negligible, the  $S/(N+D)$  is due to the reference only. In reality, this assumption can not be made. In the case of the Great Reference (See Figure 11), performance matches or exceeds the capability of the test setup.  $S/(N+D)$  ratios of 72 and 82 dB are sufficient for the 12-bit and 14-bit converters. For the 16-bit converters, 88 to 94 dB is necessary.

FFT tests were performed at 100Hz and 1kHz. The 100Hz test checks the output impedance of the reference chip itself which dominates at low frequencies. The 1kHz FFT test checks the output impedance at intermediate frequencies in the kHz range. The highest output impedance was seen in all references at these intermediate frequencies.

Since the reference capacitors dominate the impedance at high frequencies, high frequency FFT tests were not necessary. Although not tested, the best reference is likely to yield the best DNL performance.

The least complicated reference circuit is the stand-alone reference chip with a passive compensation network. Its temperature drift and noise performance is equal to the reference chip itself since the compensation network does not change the dc output voltage. Keeping the output impedance low from dc to 1MHz is not trivial however, since there is no additional active circuitry added to perform this task. Five references were tested in the stand-alone configuration. Figures 4, 5, 6, 7, and 8 illustrate schematics and measured specifications for these references. All references are monolithic with the exception of the CS3902 reference which is a hybrid. Notice that the CS3902 and the LT1019-4.5 require no trimming for 4.5V operation. The calculated value of R2 in each of the references above will change slightly



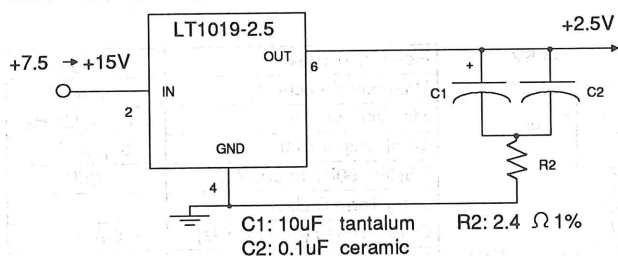


Figure 6. LT1019-2.5 Reference

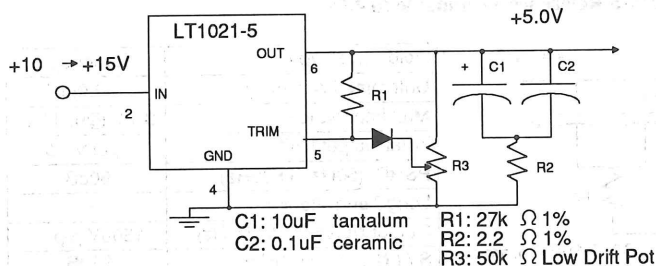


Figure 7. LT1021 Reference

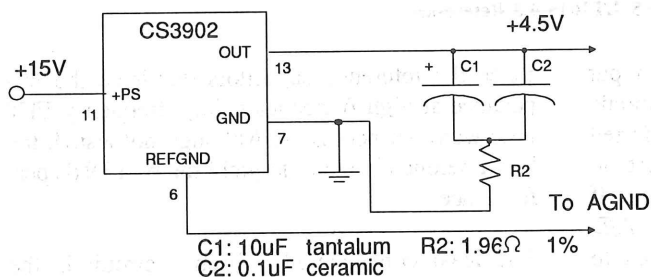


Figure 8. CS3902 Reference

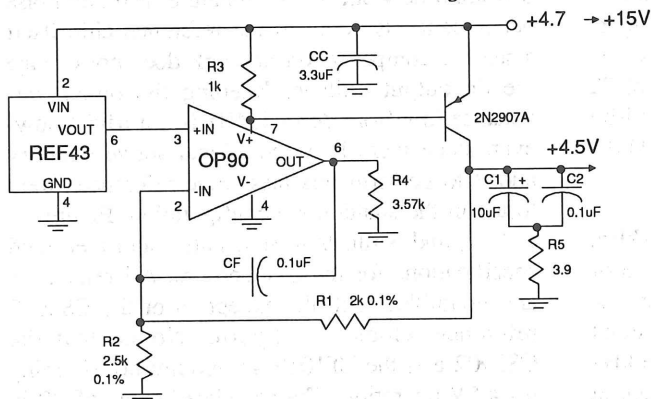


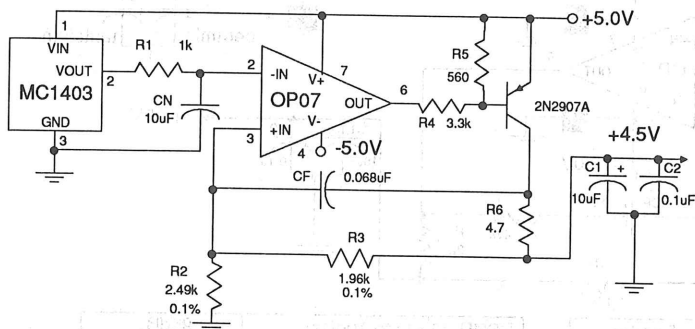
Figure 9. Low Power Supply Reference

Reference Type	Bandgap
Untrimmed Accuracy	1.25mV
Max Impedance	4.0 $\Omega$ @5.8kHz
Total Output Drift	5ppm/ $^{\circ}$ C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	100uV p-p
S / ( N + D ) (100Hz)	87dB
S / ( N + D ) (1kHz)	86dB

Reference Type	Zener
Untrimmed Accuracy	2.5mV
Max Impedance	3.8 $\Omega$ @5.0kHz
Total Output Drift	3ppm/ $^{\circ}$ C
PSRR (50Hz to 500Hz)	86dB
Long Term Stability	15ppm/1000hr
Output Noise	60uV p-p
S / ( N + D ) (100Hz)	90dB
S / ( N + D ) (1kHz)	90dB

Reference Type	Zener
Untrimmed Accuracy	500uV
Max Impedance	2.5 $\Omega$ @20kHz
Total Output Drift	0.5ppm/ $^{\circ}$ C
PSRR (50Hz to 500Hz)	100dB
Long Term Stability	6ppm/1000hr
Total Output Noise	80uV p-p
S / ( N + D ) (100Hz)	90dB
S / ( N + D ) (1kHz)	90dB

Reference Type	Bandgap
Untrimmed Accuracy	1.5mV
Max Impedance	4.4 $\Omega$ @1kHz
Total Output Drift	8.0ppm/ $^{\circ}$ C
PSRR (50Hz to 100Hz)	60dB
Long Term Stability	-
Output Noise (dc to 1MHz)	400uV p-p
S / ( N + D ) (100Hz)	88dB
S / ( N + D ) (1kHz)	88dB



Reference Type	Bandgap
Untrimmed Accuracy	50mV
Max Impedance	6.9Ω @ 2kHz
Total Output Drift	25ppm/°C
PSRR (50Hz to 100Hz)	80dB
Long Term Stability	-
Output Noise (dc to 1MHz)	30uV p-p
S / (N + D) (100Hz)	90dB
S / (N + D) (1kHz)	90dB

**Figure 10. Low Headroom Reference**

between units. Since the actual variation is small, picking the closest 1% tolerance resistor to the calculated value should give similar performance for all references of a particular manufacturer's model.

Other stand-alone voltage references with similar specifications include the AD584, REF02, REF03, REF10, and REF43. When designing with these references, the equation shown in Figure 2 should be used to calculate the appropriate value of R2 for each type of reference.

For applications which use  $\pm 5.0$  volt supplies, the reference in Figure 9 can be used. This reference circuit, designed by PMI, takes advantage of their new low power op-amp in a novel feedback configuration to achieve a 4.5 volt reference which operates from 4.7 to 15 volt supplies.

Since only a few microamps of quiescent current flows in the op-amp, it can be assumed that the only current flowing in R3 is the same as that flowing in R4. It can be shown that  $V_6 = 3.57(V_{in} - V_7)$ . For an output of 4.5 volts, and a supply of 4.7 volts, the op-amp has a supply of approximately 4.0 volts and an output voltage of 2.14 volts. This output voltage is well within the maximum specification of the OP-90 op-amp. Other references can be substituted for the

REF43 if different drift or noise specifications are required.

The reference shown in Figure 10 is a low noise reference with less than 30μV peak-to-peak of noise from dc to 1MHz. It uses a discrete output stage allowing Vref to come within 300mV of the positive supply. The filtering network R1,CN reduces the bandwidth of the reference and therefore reduces the total output noise. The OP-07 is a low noise op-amp which buffers the filtered reference. This op-amp contributes very little noise to the entire reference circuitry.

The temperature coefficient of this reference is primarily due to the matching of the gain resistors R2 and R3, so low temperature drift resistors should be used. Long term drift is dominated by the MC1403's drift. Other 2.5 volt references can be used to improve this specification. The output voltage can be changed by adjusting R2 and R3 according to the following equation:  $V_{ref} = V_{out} \cdot ((R_2 + R_3) / R_2)$ . Resistors with 0.1% tolerance for R2 and R3 limit the reference's untrimmed accuracy only. Resistors with 1% or 5% tolerance can be used if untrimmed accuracy less than 50mV is not necessary. The supplies of the OP-07 should be bypassed with 0.1μF capacitors to ground.

The reference in Figure 11 exhibits very good noise, output impedance, and long term drift per-



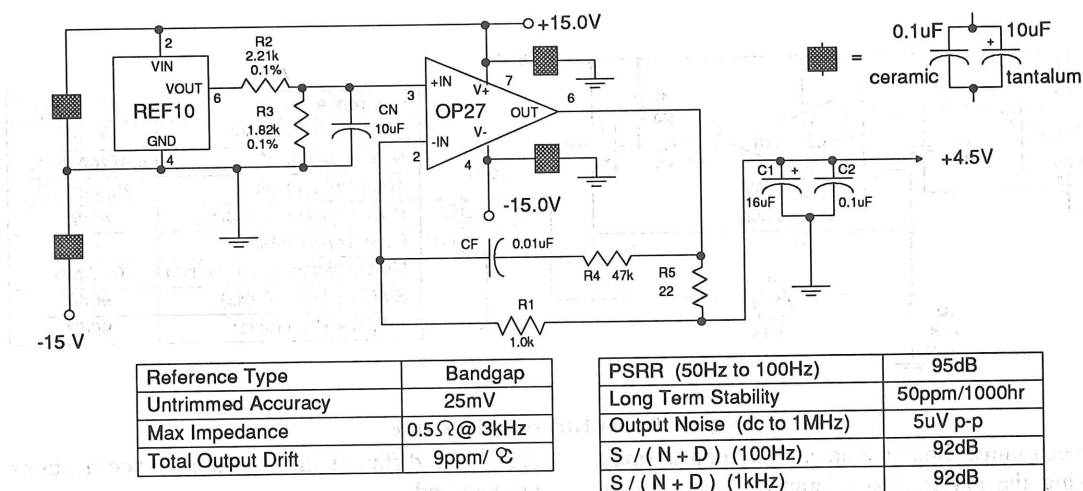


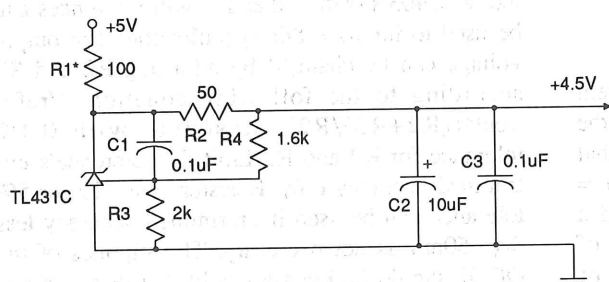
Figure 11. - Great Reference

formance. It can be used in applications which have  $\pm 15$  volt supplies available. The reference has noise less than  $10\mu\text{V}$  peak-to-peak from dc to 1MHz. The filtering network R2, R3, and CN filters noise components greater than 10Hz from the output of the REF10 reference. The OP-27 is a very low noise op-amp with excellent input offset drift over time and temperature.

The temperature coefficient of this reference is primarily due to the matching of the voltage

divider R2 and R3, assuming that an appropriate low leakage capacitor is chosen for CN. Matched, low temperature drift resistors should be used when absolute accuracy is required. Temperature drift of the reference chip plus input offset drift of the op-amp is about  $9\text{ppm}/^\circ\text{C}$ . Other 10 volt references can be used in place of the REF10.

The reference voltage can be changed by adjusting R2 and R3 according to the following equation.  $V_{\text{ref}} = V_{\text{out}} \cdot (R3 / (R2 + R3))$ .



\* Can be operated from +12 or +15 volts if R1 is changed to 2K.

Reference Type	Bandgap
Untrimmed Accuracy	30mV
Max Impedance	50 Ω @ 600Hz
Total Output Drift	30ppm/ °C
PSRR (50Hz to 500Hz)	85dB
Long Term Stability	-
Output Noise (dc to 1MHz)	100uV p-p
S / (N + D) (100Hz)	92dB
S / (N + D) (1kHz)	91dB

Figure 12. -TL431 Shunt Reference

This circuit has no protection against accidentally applying  $\pm 15\text{V}$  to the VREF pin. This could occur if the OP27 fails.

For applications where good dynamic performance is required, but only moderate dc accuracy, the TL431 shunt reference is an inexpensive solution. Figure 12 shows an example circuit, along with the excellent dynamic performance numbers.

### Miscellaneous Applications Information

Noise from the voltage reference element may reduce system performance. Bandgap references tend to generate much more noise than zener diodes. To obtain the best noise performance from the reference element, it should be band-limited. Note the broadband noise for the LT1019-5 circuit (Figure 4,  $250\mu\text{V}$ ) versus the noise of a similar bandgap reference with additional circuitry to band-limit the noise as in the Great Reference (Figure 11,  $10\mu\text{V}$ ).

Thermal temperature gradients due to power dissipation on the voltage reference die can create output voltage shifts. Keeping the entire chip on an isothermal plane is helpful. Reference load conditions should be kept very close to those specified, or degraded temperature performance will result. Some references specify a thermal regulation in ppm/mW. This can be used to calculate voltage drift for a specific power dissipation due to loading.

Overall die temperature change can cause thermally induced output voltage variations which can exceed electrical effects. Shifts in power dissipation on the board level are the major contributor to this error. In critical applications, using a heat-sink is recommended to keep the reference temperature deviations small.

Thermocouple effects between package leads can also cause excessive output voltage drift and noise. Differences between materials in IC leads

and PC-board traces can cause thermoelectric effects. Ambient air turbulence around the leads causes mismatches in the temperature between the package leads. The resulting thermoelectric voltage contributes to noise. Using dual in-line packages (DIPs) is recommended over using TO-5 type packages. The copper or Alloy 42 lead frames on DIPs are much less sensitive to thermocouple effects than the Kovar leads of the TO-5 packages. Using an enclosure such as a polysulfone shield which blocks the air flow over the reference package will also reduce the problem by reducing air movement around the package leads.

In reference circuits which have external gain setting resistors, tracking of the temperature coefficients of these resistors is vital. Wirewound resistors made of Evenohm or Mangamin have the lowest temperature coefficients. Ceramic film resistors such as Vishay are also good. Matching in resistor temperature coefficients as good as  $0.4\text{ ppm}/^\circ\text{C}$  can be achieved. Arranging these resistors in close proximity to one another also helps matching. SIP or DIP resistors by Beckman and Vishay exhibit the best matching since all resistors are processed on the same substrate.

Part #	Manufacturer	Telephone Number
CS3902	Crystal Semiconductor	(512) 445-7222
LT1019-5	Linear Technology	(408) 432-1900
LT1019-4.5		
LT1019-2.5		
LT1021-5		
OP07	Precision Monolithics Inc.	(408) 727-9222
OP90		
REF02		
REF03		
REF43		
OP27		
REF10		
TL431	Texas Instruments	
TL431		
MC1403		
	Motorola	

### List of Manufacturers

Reference	Type	Untrimmed Accuracy	Maximum Impedance	Output Drift	PSRR (50Hz to 100Hz)
LT1019-5	Bandgap	2.5mV	6.5Ω @ 3.2kHz	5ppm/ °C	90dB
LT1019-4.5	Bandgap	3.0mV	3.1Ω @ 6.1kHz	5ppm/ °C	90dB
LT1019-2.5	Bandgap	1.25mV	4.0Ω @ 5.8kHz	5ppm/ °C	90dB
LT1021-5	Zener	2.5mV	3.8Ω @ 5.0kHz	3ppm/ °C	86dB
CS3902	Zener	500uV	2.5Ω @ 20kHz	0.5ppm/ °C	100dB
Low Supply	Bandgap	1.5mV	4.4Ω @ 1kHz	8ppm/ °C	60dB
Low Headroom	Bandgap	50mV	6.9Ω @ 2kHz	25ppm/ °C	80dB
Great	Bandgap	25mV	0.5Ω @ 3kHz	9ppm/ °C	95dB
TL431 Shunt	Bandgap	30mV	50Ω @ 600Hz	30ppm/ °C	85dB

Reference	Long Term Stability *	Output Noise (dc to 1MHz)	S/(N+D) (100Hz)	S/(N+D) (1kHz)
LT1019-5	-	250uV p-p	89dB	89dB
LT1019-4.5	-	150uV p-p	91dB	90dB
LT1019-2.5	-	100uV p-p	87dB	86dB
LT1021-5	15ppm/1000hr	60uV p-p	90dB	90dB
CS3902	6ppm/1000hr	80uV p-p	90dB	90dB
Low Supply	-	400uV p-p	88dB	88dB
Low Headroom	-	30uV p-p	90dB	90dB
Great	50ppm/1000hr	10uV p-p	92dB	92dB
TL431 Shunt	-	100uV p-p	92dB	91dB

### Performance Comparison Table

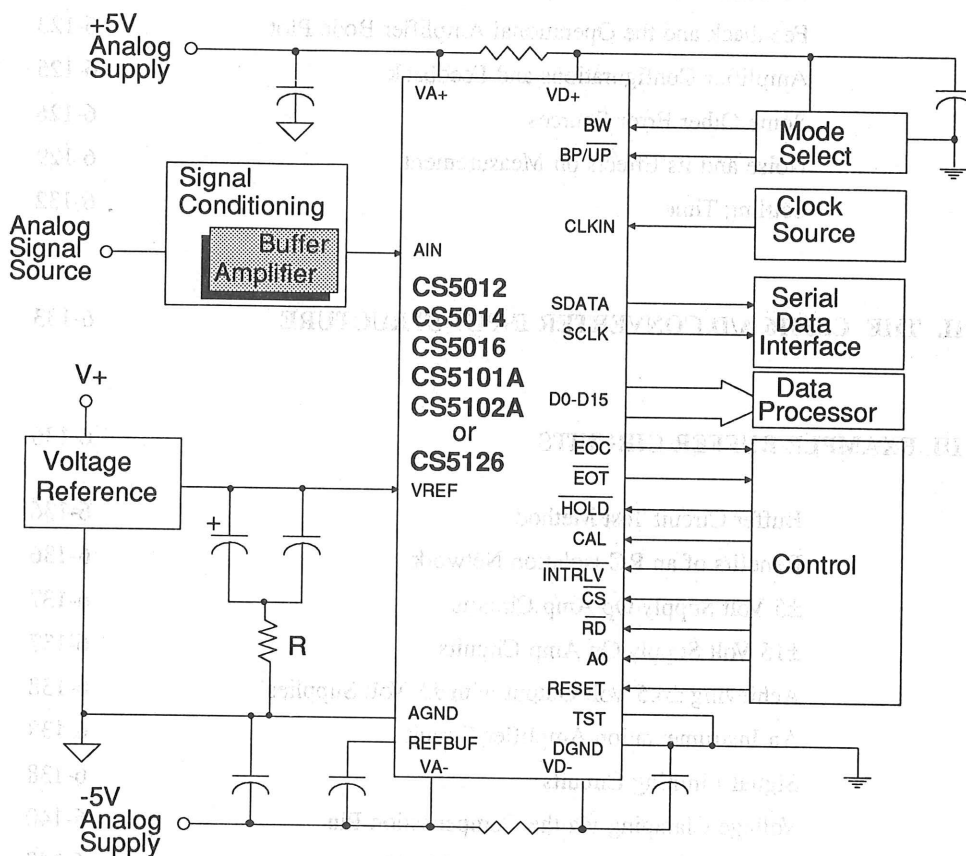
\* Taken from reference data sheets. All other parameters were measured.

## Application Note

### Buffer Amplifiers for the CS5012/CS5014/CS5016/ CS5101/CS5102/CS5126 Series of A/D Converters

by

Jerome Johnston



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### Introduction

This application note discusses buffer amplifiers for use with Crystal Semiconductor's CS5012, CS5014, CS5016, CS5101A, CS5102A or CS5126 A/D converters. Amplifier design considerations are discussed and several circuits are proposed.

### Signal Requirements for Analog to Digital Converters

Crystal Semiconductor is a source for a variety of monolithic A/D Converters. While the type of design configuration of the converters may differ, their uses could be classified into two general categories: those which require specifications in static measurement applications; and those which require specifications for signal processing or dynamic signal measurement applications.

The capability of a converter to achieve a stated static measurement requirement is generally defined by its linearity error specifications, both integral and differential, and by its offset error and gain error specifications. To assess the total error in a static measurement, the effects of temperature on the offset, gain, and linearity errors must also be investigated. In static measurement systems, these same error sources need to be scrutinized in the signal conditioning circuitry as well.

When a converter is used in dynamic signal measurement applications (generically known as "signal processing"), its signal measurement capability is indicated by specifications such as total harmonic distortion, signal to noise ratio, and signal to peak harmonic or spurious noise. Signal processing designers generally evaluate the error contribution of the signal conditioning circuitry in terms of these same parameters.

Signal conditioning circuitry generally includes all circuitry from the transducer or the signal

source up to the A/D converter. This application note will concern itself primarily with the requirements of the amplifier which immediately precedes the A/D converter. This amplifier will be called a buffer amplifier.

In the design of an A/D converter system, the buffer amplifier can be a source of significant errors. The significance of these errors can only be assessed if the circuit configuration is thoroughly analyzed for its total error contribution. A thorough analysis requires a good understanding of amplifier specifications, of the limitations of the different circuit configurations, and of the benefits and limitations of feedback. A good place to begin is with a review of feedback theory.

### I. OPERATIONAL AMPLIFIERS: Review Of Theory

#### Feedback Control Theory

The goal in using feedback is to establish a closed-loop system whose operating characteristics are primarily determined by the choice of the feedback elements. The extent to which this goal can be accomplished is explained by feedback control theory. Figure 1 illustrates the classical feedback control loop. The equations

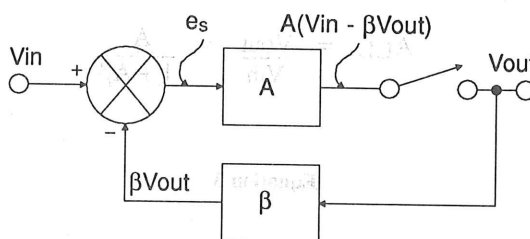


Figure 1. The Classic Feedback Control Loop

which describe this control loop are directly applicable to the noninverting operational amplifier circuit.

The control loop consist of an input voltage differencing section whose output is amplified by a positive gain section. A fractional part of the signal output is then returned to the negative terminal of the differencing section though the feedback network. The input differencing section, indicated by the circle with the X in it, determines the difference in the signals at the (+) and (-) inputs. The difference is indicated by an error signal of the quantity:

$$e_s = (V_{in} - \beta V_{out})$$

Equation 1

which is then amplified by the open-loop voltage gain of the amplifier:

$$A (V_{in} - \beta V_{out}) = V_{out}$$

Equation 2

The amplifier open-loop gain is represented in Figure 1 by the box with the A in it. The feedback portion of the loop is represented by the box with the  $\beta$  in it.  $\beta$  is defined as the feedback attenuation factor and its value is that fractional part of the output voltage which is fed back to the input. Equation 2 can be manipulated to give:

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{A}{1 + A\beta}$$

Equation 3

This is the key equation in the feedback system. Equation 3 indicates that the closed-loop gain is dependent upon both the open-loop gain and the

feedback factor,  $\beta$ . The product,  $A\beta$ , in the denominator is called the loop gain. Its name comes from the gain seen by a signal propagating around the loop through both the A and  $\beta$  networks.

Equation 3 can be manipulated to give:

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{1}{\beta} \left[ \frac{1}{1 + \frac{1}{A\beta}} \right]$$

Ideal Term
Error Multiplier

Equation 4

In equation 4 the ideal term,  $1/\beta$ , determines the ideal closed-loop gain of the system. The value of  $1/\beta$  is determined by the elements chosen for the feedback path. The intent is for these elements to determine the closed-loop characteristics of the feedback system. To the extent that this is accomplished is dependent upon the magnitude of the loop gain  $A\beta$ . The greater the magnitude of  $A\beta$ , the more closely the error multiplier term approaches unity, therefore allowing the ideal term  $1/\beta$  to determine the closed-loop gain of the system. Said another way, the magnitude of the loop gain  $A\beta$  is the primary factor which determines how closely the closed-loop performance of a feedback system is determined by the feedback elements. The term  $1/\beta$  is known as the noise gain and also determines the gain seen by amplifier input referred noise and other input referred errors (such as offsets and drift parameters). The noise gain of the system is used to determine closed loop amplifier performance with respect to these error parameters, not the signal gain. The noise gain of the two basic op amp configurations will be discussed later in this application note.

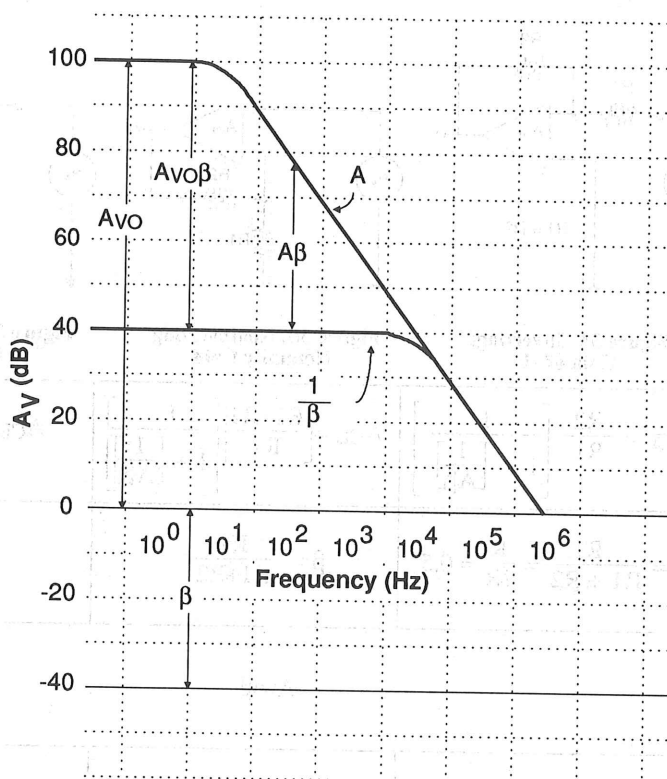


Figure 2. Bode plot illustrating the relationship of  $A_{vo}$ ,  $\beta$ ,  $1/\beta$ , and  $A_{vo}\beta$

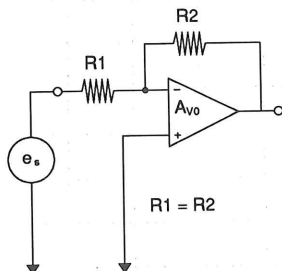
### Feedback and the Operational Amplifier Bode Plot

The feedback parameters which have been discussed can be depicted graphically on a Bode plot. Figure 2 depicts the relationship between open-loop gain, the feedback attenuation factor, noise gain, and loop gain as a function of frequency for the noninverting circuit.

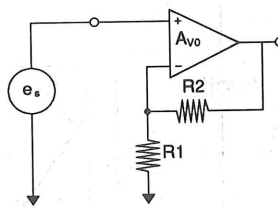
The Bode diagram shows a typical plot of the open-loop gain characteristic of an operational amplifier. At very low frequencies a typical operational amplifier may have a dc open-loop gain, ( $A_{vo}$ ) near 100 dB. A large number of amplifiers use dominant pole frequency compensation which simplifies the compensation

requirements for the user. The dominant pole, located between 0.1 and 100 Hz on various amplifiers, causes the open-loop gain characteristic ( $A$ ) to decrease in magnitude at a 20 dB/decade rate as the frequency is increased. In Figure 2 the logarithm of the feedback attenuation factor ( $\beta$ ) is shown to be negative as it is a reduction in signal amplitude. The loop gain, the product of  $A\beta$ , (or  $A_{vo}\beta$  at dc), is depicted in the figure as the sum (+100 dB plus -40 dB = 60 dB at very low frequency) of the open-loop gain and the feedback attenuation factor, or the difference (+100 dB - (+40 dB) = 60 dB) between the open-loop gain and the noise gain ( $1/\beta$ ). From the figure, one can observe that as frequency increases, the loop gain ( $A\beta$ ) decreases for a set value of  $\beta$ . To obtain a greater amount of loop gain at higher frequencies a designer must

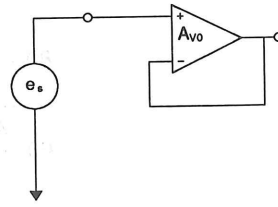




**Figure 3A. Inverting:  
Gain of -1**



**Figure 3B. Noninverting:  
Nonunity Gain**



**Figure 3C. Noninverting:  
Gain of +1**

Closed Loop Signal Gain	$A_{CL} = \frac{-R2}{R1} \left[ \frac{1}{1 + \left[ \frac{1}{A\beta} \right]} \right]$	$A_{CL} = \left[ \frac{R1+R2}{R1} \right] \left[ \frac{1}{1 + \left[ \frac{1}{A\beta} \right]} \right]$	$A_{CL} = 1 \left[ \frac{1}{1 + \left[ \frac{1}{A\beta} \right]} \right]$
Feedback Attenuation Factor	$\beta = \frac{R1}{R1 + R2} = \frac{R}{2R} = 0.5$	$\beta = \frac{R1}{R1+R2}$	$\beta = 1$
Loop Gain	$A_{vo}\beta$		
Noise Gain	$\frac{1}{\beta} = \frac{1}{0.5} = 2$	$\frac{1}{\beta}$	$\frac{1}{\beta} = 1$
Closed Loop Corner Frequency	$f_c = \frac{f_u}{ A_{CL}  + 1}$ note: $ A_{CL}  = \frac{1}{\beta} - 1$	$\frac{f_u}{\left[ \frac{1}{\beta} \right]}$	$f_c = f_u$
Closed Loop Gain Stability	$\frac{\Delta A_{CL}}{A_{CL}} = \frac{\Delta A_{OL}}{A_{OL}} \left[ \frac{1}{1+A\beta} \right]$		
Closed Loop Distortion and Nonlinearity	$THD_{CL} = THD_{OL} \left[ \frac{1}{1+A\beta} \right]$		
Closed Loop Output Impedance	$Z_{CL} = Z_{OL} \left[ \frac{1}{1+A\beta} \right]$		

**Figure 3. Basic Circuit Configurations**

either increase the open-loop gain of the amplifier or increase the feedback factor,  $\beta$  (decrease the noise gain). Remember that both the open-loop gain and the feedback attenuation factor are not constant, but instead are functions of frequency. Therefore the value of the loop gain is a function of frequency as well. The quantity of loop gain at the operating frequency is the key measure of how closely an amplifier configuration approaches the ideal.

### Amplifier Configurations and Feedback

Figure 3 provides an overview of the inverting and noninverting voltage amplifier configurations. General equations for various parameters of the configurations are given with special emphasis on the unity gain configuration. Signal gain is set by the choice of resistors, but the gain error (assuming perfectly accurate resistors) is a function of the loop gain in the error multiplier term as previously stated in our discussion on feedback. The unity gain noninverting amplifier is just a special case of choosing the value of resistor  $R1$  as being infinite and  $R2$  being zero. Notice that the feedback attenuation factor,  $\beta$ , as derived for both circuits yields the same equation:

$$\beta = \frac{R1}{R1+R2}$$

Equation 5

but for the unity gain inverting amplifier this results in a value of 0.5 whereas the unity gain noninverting amplifier results in a  $\beta$  of 1. These unequal values of  $\beta$  between the two unity-gain configurations yield further differences between the inverting and noninverting circuits. Loop gain for the unity-gain inverting circuit is half that of the noninverting unity-gain circuit. This results in the inverting circuit being more easily compensated for stability, but also yields greater errors in those parameters where loop gain is a

factor. More will be said about these parameters later.

Reduced  $\beta$  for the inverting configuration results in greater noise gain ( $1/\beta$ ). Error sources such as offset and noise are amplified by the noise gain and therefore the unity-gain inverting amplifier is more adversely affected by these error sources. Another negative factor of the unity-gain inverting stage is that its signal bandwidth is half that of the noninverting circuit with identical amplifiers. This bandwidth reduction is because bandwidth is a function of the noise gain, not the signal gain. Be aware of this fact when using low gain inverting stages.

The magnitude of the loop gain in a circuit affects many parameters in both the inverting and noninverting configurations. Closed loop gain stability is improved by increased loop gain as indicated in the equation:

$$\frac{\Delta A_{CL}}{A_{CL}} = \frac{\Delta A_{OL}}{A_{OL}} \left[ \frac{1}{1+A\beta} \right]$$

Equation 6

The effects of changes in the open-loop gain (such as a reduction due to increased temperature) are reduced proportionally to the amount of loop gain. Open loop distortion and nonlinearity are reduced by increased loop gain. This reduction in total harmonic distortion as indicated in the equation:

$$THD_{CL} = THD_{OL} \left[ \frac{1}{1+A\beta} \right]$$

Equation 7

The output impedance of a voltage amplifier is reduced with feedback as indicated in the equation:

$$Z_{CL} = Z_{OL} \left[ \frac{1}{1+A\beta} \right]$$

**Equation 8**

The input impedance of both amplifier configurations benefit from increased loop gain. Although increased loop gain is desirable in both circuit configurations the effect of feedback on the two configurations is different.

The noninverting amplifier utilizes voltage ratio feedback which increases the differential input impedance seen by the input signal. But the differential input impedance of the amplifier is shunted by the common mode input impedance of the amplifier. Because the common mode impedance cannot be increased by the use of feedback it is usually the limiting factor in increasing the input impedance.

The inverting amplifier configuration uses transadmittance feedback which decreases the impedance at the summing node of the input and feedback resistors. This decrease in impedance improves the virtual ground characteristic of the amplifier. In the inverting configuration the effect of a good virtual ground enables the effective value of the input impedance seen by the signal source to be set by the input resistor.

In both configurations the improvements to the respective impedances depend on the magnitude of loop gain. As the magnitude of loop gain generally decreases with increased frequency, all of the parameters normally improved by loop gain tend to degrade as the signal frequency increases. All real-world amplifiers have finite open loop gain and finite bandwidth, both of which affect the amount of loop gain available to a designer. A designer must make a prudent choice

of amplifier and of the circuit configuration to minimize the errors due to loop gain limitations.

### Some Other Error Sources

There are many sources of error in a given amplifier configuration. As already discussed, limited loop gain is a source of gain error which can affect DC accuracy. In addition to the DC gain error, there are the various offset errors which are contributed dependent upon the characteristics of the chosen amplifier. Sources of offset errors are the input offset voltage of the amplifier, the input bias and the input offset currents of the amplifier, limited power supply rejection and limited common-mode rejection.

Which of these errors is dominant will depend upon the choice of amplifier and its application configuration. It is a routine procedure to calculate the contribution of each source of error and this should be done as a matter of course. A few comments on each of these sources of error is appropriate.

All amplifiers have input offset voltage and input bias currents which result in errors in signal measurement. The input bias currents flow through the resistances on the (+) and (-) leads of the amplifier and produce an offset voltage error at each input. These offset voltages, and the voltage offset of the amplifier itself, are then amplified by the circuit to produce an error in the output signal. To reduce the errors due to the bias currents the standard practice has been to balance the value of resistance at the inverting and noninverting inputs to an amplifier. The purpose of making these two resistances equal has been to enable the bias currents at both inputs to produce equivalent values of offset voltage which could then be rejected by the common mode capability of the amplifier. This practice is an acceptable method of reducing error due to the bias currents and is recommended except with modern

amplifier designs which have internal bias current compensation circuitry. The bias current compensation circuitry tends to reduce the bias currents an order of magnitude or more, to the extent that they are reduced to the same order of magnitude as the amplifier's input offset currents. Adding a resistor to one input to achieve equal resistances at the two inputs of these types of amplifiers is not recommended. The added resistance is not effective in reducing the error due to the bias currents, but it will add another source of thermal noise.

Initial offset errors as well as gain errors generally can be reduced to zero with initial system calibration adjustments at room temperature. The effects of temperature-induced offset drift and gain drift remain unless a method of ongoing correction or recalibration is used to remove these effects. This correction may be accomplished with a computer after the analog signals are digitized and is recommended when maximum accuracy of measurement is demanded.

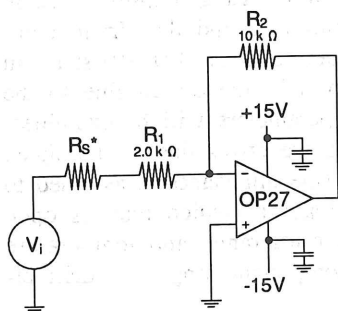
Even if the effects of temperature-induced offset errors are removed from the final data by software, it remains desirable to examine the total errors at each gain stage throughout the system. Voltage offsets due to temperature drift can be removed in software, but may still consume a significant portion of the dynamic range available to the signal. This is especially true in 16-bit converter systems with wide temperature range requirements such as required by some military specifications (-55 to +125 ° C).

Limited power supply rejection and limited common mode rejection are two more sources of errors. Most commercially-available amplifiers are designed such that the offset voltages induced by power supply variations or common-mode signals are very small; but these errors can be significant when amplifying very low level signals with high gain. It is therefore recommended to examine the error contribution of each of these sources.

Figure 4a shows an inverting amplifier circuit. The operational amplifier and the circuit components have been chosen for illustration purposes. The errors in the circuit due to the various amplifier parameters will be examined. Not included are those errors due to the signal source impedance (the impedance is assumed to be zero), output loading (which reduces open loop gain), resistor tolerance and temperature coefficient, and component long term drift effects.

A table in Figure 4a contains a selected subset of specifications for a "generic" OP-27C. No specific manufacturer is implied. The subset of data is for the total error band of the stated parameters over the -55° to +125°C temperature range. Manufacturers do not always specify temperature drift coefficients in their component data sheets. Instead, the specification sheets contain a table of data for the amplifier at room temperature (25° C) along with a table showing the total error band of the various parameters over a stated temperature span (say 55° to 125° C). Usually the specification data tables are supplemented by supporting graphs which indicate typical drift characteristics for the various parameters. These graphs can be very informative. For example, graphs in the manufacturer's data sheets (see the Precision Monolithics or the Linear Technology data book) for the OP-27 indicate that input bias currents and input offset currents show much more drift at temperatures approaching -55° C than at temperatures above 25° C. Another graph indicates that the direction of the input offset voltage drift in the OP-27 is unpredictable.

The normal procedure to calculate the error contribution of each of the operational amplifier drift parameters is to multiply the rate of drift times the temperature span over which the circuit is to be subjected. These errors due to drift are then added to the initial errors of each of the parameters at the ambient operating temperature. Because amplifier manufacturers specify total



\* Assumed to be zero.

$$R_e = \frac{R_2 R_1}{R_1 + R_2} = 1.667 \text{ k}\Omega$$

$$\text{Ideal Signal Gain} = \frac{-R_2}{R_1} = -5$$

$$\text{Feedback Attenuation Factor } \beta = \frac{R_1}{R_1 + R_2} = \frac{1}{6}$$

$$\text{Noise Gain} = \frac{1}{\beta} = 6$$

$$\text{Closed Loop Bandwidth } f_c = \frac{f_u}{|A_{CL}| + 1} \left[ \frac{8 \times 10^6}{6} \right] = 1.33 \text{ MHz}$$

### Generic OP-27 Specifications Total Error Band for -55° to +125°C Temperature Span

		Typical	Worst Case
Input Offset Voltage	$V_{IO\Delta t}$	70 $\mu$ V	300 $\mu$ V
Input Bias Current†	$I_{B\Delta t}$	$\pm 35$ nA	$\pm 150$ nA
Large Signal Open Loop Gain	$A_0$	$800 \times 10^3$ V/V	$300 \times 10^3$ V/V
Power Supply Rejection Ratio	P.S.R.R.	$4 \times 10^{-6}$ V/V (108 dB)	$51 \times 10^{-6}$ V/V (86 dB)
Common Mode Rejection Ratio	C.M.R.R.	$1.6 \times 10^{-6}$ V/V (116 dB)	$20 \times 10^{-6}$ V/V (94 dB)

† Bias currents are usually of one polarity. Bias currents of both polarities indicate the use of bias current cancellation circuitry in the input stage.

Figure 4a. OP-27 Circuit and Total Error Band Specifications

Errors: -55°C to 125°C ( $\Delta t$ )

Gain	Input Offset Voltage	Input Bias Current	P.S.R.	C.M.R.	Noise
$V_o = -V_i \left[ \frac{R_2}{R_1} \right] \left[ \frac{1}{1 + \frac{1}{A_0 \beta}} \right] + V_{IO\Delta t} \left[ \frac{1}{\beta} \right] + I_{B\Delta t} R_1 \left[ \frac{R_2}{R_1} \right] + \frac{2\Delta V_{IO}}{\Delta V_{SUP}} \left[ \frac{1}{\beta} \right] + \frac{\Delta V_{IO}}{\Delta V_{CM}} \left[ \frac{1}{\beta} \right] + \text{Noise}$					
$V_o = -V_i \left[ \frac{R_2}{R_1} \right] \left[ 1 + \frac{1}{(300 \times 10^3) \frac{1}{6}} \right] + (\pm 300 \times 10^{-6})(6) + (\pm 150 \times 10^{-9})(2 \times 10^3)(5) + (2)(51 \times 10^{-6})(100 \times 10^{-3})(6) + \approx 0 + \text{Noise}$					
$V_o = -0.99998 V_i$	$\pm 1.8 \times 10^{-3} \text{ V}$	$\pm 1.5 \times 10^{-3} \text{ V}$	$\pm 61.2 \times 10^{-6} \text{ V}$	$\pm \approx 0$	+ Noise
<b>Worst Case Error % Full Scale Output†</b>					
0.002%	+ 0.040%	+ 0.033%	+ 0.00136	+ $\approx 0\%$	+ Noise

† Based upon: 4.5 V FSO; 100 mV power supply change on each supply.

Figure 4b. Total Error Band Calculations

error band rather than drift rates, the method of computing the error contribution of each parameter must be modified. The equation in Figure 4b illustrates the errors calculated using the total error band specifications on the OP-27C in Figure 4a. The calculations indicate the relative contribution of each source of error in the worst case with the exception of noise, which is yet to be discussed. As can be seen from the numbers, real world amplifiers can contribute significant errors in a high precision data acquisition system due to their non-ideal characteristics.

$$e_r = \frac{4nV}{\sqrt{(Hz)}} \sqrt{\frac{R}{1k\Omega}}$$

Equation 10

This noise value assumes a one Hz bandwidth. The noise within a wider bandwidth can be computed by:

$$e_r = \frac{4nV}{\sqrt{(Hz)}} \sqrt{\frac{R}{1k\Omega}} B$$

Equation 11

### Noise and its Effects on Measurement

Noise can have a significant detrimental effect in high precision data acquisition systems. Although one can encounter many different sources of noise and of interference in system design, only certain noises made by the components themselves will be discussed here. Thermal noise, also called Johnson noise, is fundamental to all components. The thermal noise in a resistor can be calculated by use of the formula:

$$e_n = \sqrt{(4kTBR)}$$

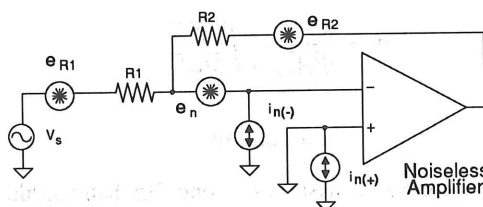
Equation 9

where  $k = 1.38 \times 10^{-23}$  Joules/ degree K (Boltzman's constant),  $T$  = Absolute temperature of the resistor,  $B$  = the effective "brickwall" Bandwidth over which the noise is to be measured, in Hz,  $R$  = Resistance value.

The amount of noise generated by a resistor can be made easier to calculate by remembering that the amount of noise generated by a 1 k $\Omega$  resistor in a 1 Hz bandwidth is 4 nV rms. The amount of noise per  $\sqrt{Hz}$  generated by any other valued resistor can be computed from this normalized value:

Components other than resistors generate thermal noise. The OP-27 monolithic amplifier is classified by its manufacturers as a low noise amplifier. It is optimized for low voltage noise and requires low source impedances to achieve good noise performance. A plot of the OP-27 noise voltage and noise current characteristics is given in the manufacturer's data sheet. The amplifier's noise is uniform across the higher frequencies, but increases at frequencies approaching DC. This increase is called flicker noise, or 1/f noise.

A thermal noise model of the circuit of Figure 4a is shown in Figure 5. Five noise sources are shown in the model. The amplifier has a voltage noise source  $e_n$  and two current noise sources; one associated with each input of the amplifier. Each of the amplifier current noise sources will generate a corresponding noise voltage which is a function of the impedance seen by the current noise source. In addition to the voltage and current noise sources, each of the resistors has a noise voltage source associated with it. The amount of noise contributed at the input of the amplifier by the each of the resistor noise sources is reduced by the loading of the other resistor. For example, consider noise source  $e_{R2}$  as having resistor  $R2$  as its source impedance with resistor  $R1$  acting as the load. The noise seen at the



Noise Model of Amplifier in Figure 4a.

## Effective Amplifier Bandwidth

OP-27 typical unity gain frequency = 8 MHz

$$\text{circuit bandwidth} = \frac{f_u}{|A_{CL}| + 1} = \frac{8 \times 10^6}{5 + 1} = 1.33 \text{ MHz}$$

$$\text{effective noise bandwidth} \\ B = (1.33 \times 10^6)(1.57)^{\dagger} = 2.1 \text{ MHz}$$

<sup>†</sup> The effective noise bandwidth of a single pole, lowpass filter is 1.57 times greater than the 3 dB corner frequency.

## Noise Sources of the Model

Amplifier Noise Voltage	$e_n \text{ max } (f_0 = 1 \text{ kHz}) 25^\circ\text{C} = 4.5 \text{ nV}/\sqrt{\text{Hz}}$	} From data sheet specifications
Amplifier Noise Current	$i_n \text{ max } (f_0 = 1 \text{ kHz}) 25^\circ\text{C} = 0.6 \text{ pA}/\sqrt{\text{Hz}}$	

$$e_{R1} = \frac{4.5 \text{ nV}}{\sqrt{\text{Hz}}} \sqrt{\frac{2 \text{ k}}{1 \text{ k}}} = \frac{5.65 \text{ nV}}{\sqrt{\text{Hz}}}$$

$$e_{R2} = \frac{4.5 \text{ nV}}{\sqrt{\text{Hz}}} \sqrt{\frac{10 \text{ k}}{1 \text{ k}}} = \frac{12.6 \text{ nV}}{\sqrt{\text{Hz}}}$$

## Equivalent Input Referred Noise (Thermal)

$$e_t = \sqrt{(e_n)^2 + \left[ i_n(-) \left[ \frac{R_1 R_2}{R_1 + R_2} \right] \right]^2 + \left[ i_n(+)(0) \right]^2 + \left[ e_{R1} \left[ \frac{R_2}{R_1 + R_2} \right] \right]^2 + \left[ e_{R2} \left[ \frac{R_1}{R_1 + R_2} \right] \right]^2}$$

$$e_t = \frac{6.8 \text{ nV}}{\sqrt{\text{Hz}}}$$

## Total Output Noise (Thermal)

$$E_T = e_t \sqrt{B} \frac{1}{\beta} = \frac{6.8 \text{ nV}}{\sqrt{\text{Hz}}} \sqrt{2.1 \times 10^6} \frac{1}{1/6} = 59 \text{ } \mu\text{Vrms}$$

Peak Noise will be much greater.

Figure 5. Noise Calculations



input of the amplifier from source  $e_{R2}$  will be only that portion of its output which is developed across resistor  $R1$  (assuming the input impedance of the op amp is very high). The noise generated by  $e_{R1}$  is reduced by the loading of resistor  $R2$ . The amount of noise generated at the input of the amplifier by each of the sources is tabulated in Figure 5. The two current sources each have the same value of current noise. Using the values of the noise sources, the effective input-referred voltage noise of the circuit has been calculated. It must be remembered that the noise sources are uncorrelated and therefore add in root-mean-square fashion. This equivalent noise source then represents the total input referred thermal noise. To obtain the value of the noise at the output of the amplifier which will be input to the A/D converter, the input referred noise is amplified by the noise gain of the amplifier while at the same time taking into consideration the effective noise bandwidth of the circuit.

Arriving at a value for the noise bandwidth of the OP-27 circuit is not as obvious as it might seem. If the noise gain of the circuit in Figure 4a is used to compute the 3 dB signal bandwidth the result will be 1.33 MHz. The effective noise bandwidth of a single pole filter is actually 1.57 times greater than the 3 dB corner frequency. But, above 1.33 MHz the OP-27 gain-phase characteristics are not those of a single pole system, but are more complex. The internal gain-phase compensation of the OP-27 will actually cause gain peaking in the circuit of Figure 4a. The gain peaking will occur at the point where the closed loop gain and open loop gain crossover. Also, at frequencies approaching the unity-gain-crossover of the OP-27, the amplifier gain will differ from the roll off of a single pole filter. The effects of the gain peaking and the complex gain-phase characteristics of the OP-27 above the 3 dB corner frequency make an accurate estimate of the resultant noise difficult. One can use the single pole filter characteristics and can approximate the noise bandwidth of the circuit as being 1.57 times the 1.33 MHz corner frequency

(2.1 MHz), but the resultant noise calculation using this bandwidth will yield only a coarse approximation of the actual noise.

Using the assumption that the approximation is adequate, the noise at the output of amplifier has been calculated as shown in Figure 5. The calculated value is the amount of thermal noise in rms volts.

Thermal noise is both white and Gaussian. "White" describes the noise as having equal spectral density at all frequencies. "Gaussian" defines the probability density function which describes the amplitude characteristics of the noise. Gaussian noise follows the Normal Distribution. Therefore, once the rms value of the noise has been determined, the probability of occurrence of any value greater than a particular amplitude can be determined. The peak (+ and -) noise associated with a stated probability of occurrence is indicated in the following table:

Probability of Having a higher Amplitude Occurrence	Peak to Peak Amplitude
10 %	3.29 x RMS
1 %	5.15 x RMS
0.1 %	6.58 x RMS
.001 %	7.78 x RMS

Since the peak noise can adversely affect A/D measurements it should be investigated by both analysis and measurement. Minimization of thermal noise in system design is accomplished with the application of three design principles. First, it is good practice to use the lowest resistor values possible (this assumes a voltage amplifier system) limited only by the constraints necessary to meet other system requirements. Second, choose an appropriate amplifier. Some amplifiers, such as the ubiquitous LM324, do not include noise



specifications in their data sheet. If low noise is a system requirement, amplifiers which have no noise specifications are not likely to be an appropriate choice. Also, choose an amplifier which is optimized to work with the source impedance requirements of the system. Bipolar-input amplifiers are generally optimized to work with low impedances as they have lower voltage noise than current noise while FET-input amplifiers are generally optimized for high impedances due to their lower current noise. The optimum choice of amplifier will depend not only on the amplifier, but its associated gain elements and circuit configuration. Analysis of the various possible configurations is necessary to disclose which will be optimum to meet design requirements. Third, one of the easiest ways to reduce the effects of noise is to restrict the bandwidth. System bandwidth should be restricted to only that amount necessary to meet system requirements. This should be done as a matter of good practice.

While only the effects of thermal noise have been discussed be aware of other noise sources (see the reference material at the end of this application note). Note that in the circuit of Figure 4a the effects of the 1/f noise were not investigated. If the system requirements demand the lowest noise possible the effects of the 1/f noise needs to be examined.

The example calculations on thermal noise were done at room temperature. An increase in temperature to 125° C will result in about 1.3 dB greater noise. Last of all, the calculated answers are only theoretical estimates. The calculations provide a theoretical minimum value but the final determinant of design should be in the evaluation of total system function and/or measurement of the actual amount of noise in the system. Remember that the value of the noise calculated provides only a reference point for the minimum amount of noise in the circuit; the actual amount present will never be less than the theoretical amount calculated, but can be more, due to other

noise sources which have not been accounted for. For a more thorough discussion of noise as it applies to amplifier design see references 2 through 6 listed at the end of this application note.

### Settling Time

Amplifier circuits have limitations which restrict just how quickly they can produce an accurate output signal at the application of a step change of the input signal. For small changes in signal amplitude, the ability of the amplifier to respond is dependent upon its 3 dB upper corner frequency. If the amplifier gain-phase characteristics approximate a single pole response above the 3 dB frequency the output signal will asymptotically approach a steady state output value  $V_s$  as defined by the equation:

$$V_o(t) = V_s \left[ 1 - e^{\left(\frac{-t}{\tau_c}\right)} \right]$$

Equation 12

Where the time constant,  $\tau_c$ , is given as a function of the corner frequency:

$$\tau_c = \frac{1}{2\pi f_c}$$

Equation 13

Settling time is defined as the elapsed time from when the input step voltage is applied until the output signal reaches and stays within a given error band of a steady state value.

If the input step change is large, the slew rate limit of the amplifier will restrict the speed at which its output can change. The limit at which an amplifier can slew is a function of how fast it can charge or discharge its compensation capacitor. The maximum frequency of a given

amplitude that can be faithfully reproduced by an amplifier with a stated slew rate is defined by the equation:

$$f_{\max} = \frac{SR}{2\pi V_p}$$

Equation 14

where  $V_p$  is the peak output voltage.

When large changes of signal at the input occur, the settling time of the amplifier will be a combination of initial delay, slew rate limited excursion, and small signal settling time as indicated in Figure 6. Note that the small signal settling illustrated in Figure 6 is not that of a single pole system, but is instead representative of an actual wideband amplifier.

A first order approximation of settling time can be estimated for a circuit under the following conditions. First, the signal must not cause the amplifier to enter slew rate limiting. Second, the 3 dB corner frequency of the amplifier must be known and its roll-off must be at 20dB/decade for at least a decade of frequency above the 3 dB corner frequency. Under these conditions the following equation yields a good approximation to the settling time:

$$t = -\frac{1}{2\pi f} \ln \left| \frac{V_o}{V_s} - 1 \right|$$

Equation 15

where  $f$  is the 3dB frequency. To settle to 1/2 LSB at  $N$  bits ( $N = 16$  in a 16-bit A/D) the equation can be written as:

$$t = -\frac{1}{2\pi f} \ln \left| \frac{2^N - 0.5}{2^N} - 1 \right|$$

Equation 16

Which can be simplified to the following:

$$t = \frac{(1 + N)(0.11)}{f}$$

Equation 17

Settling time is not readily predicted in other circumstances. It varies with signal amplitude and is as much dependent upon the circuit configuration and circuit components (including things like stray capacitance) as it is upon the amplifier characteristics. An assessment of circuit settling time is often best be obtained from observation of the circuit under applicable conditions.

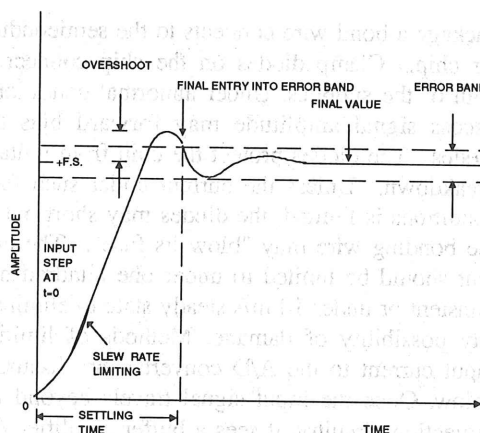


Figure 6.

## II. THE CS5016 FAMILY A/D CONVERTER INPUT STRUCTURE

The analog input pin (AIN) of the CS5016 series converter acts as a load to the buffer amplifier output. A good understanding of the internal workings of this pin on the converter will help in the design of an appropriate buffer amplifier.

Figure 7a depicts a simplified circuit diagram of the circuitry internal to the A/D converter as seen from the AIN pin. From the metal pin of the

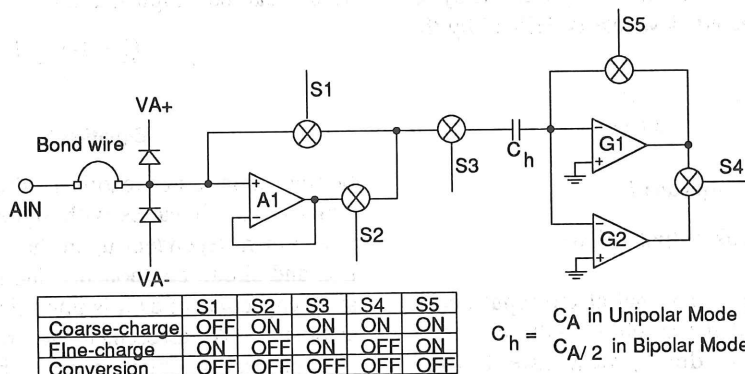


Figure 7a CS5016 Family Analog Signal Input Model

package a bond wire connects to the semiconductor chip. Clamp diodes on the chip connect to both of the supplies. Under abnormal conditions, excess signal amplitude may forward bias the diodes. The diodes protect the chip from voltage breakdown. Unless the current under such fault conditions is limited, the diodes may short out or the bonding wire may "blow its fuse". The current should be limited to under one hundred mA transient or under 10 mA steady state to eliminate any possibility of damage. Methods of limiting input current to the A/D converter are discussed below. Once the input signal travels beyond the protection circuitry, it sees a buffer amplifier A1, CMOS switches S1, S2, and S3, a hold capacitor  $C_h$ , and transconductance amplifiers G1 and G2. To accomplish a complete conversion cycle, the states of the CMOS switches are altered. These state changes cause the effective load at the AIN pin to change dynamically during the three different phases of the conversion cycle. These three phases are called coarse-charge, fine-charge and conversion. An understanding of the function of each of these three phases will explain the reasons for the dynamic change in loading. The conversion phase begins with the activation of the hold command ( $\overline{\text{HOLD}}$  goes low).

When hold is activated, the "sample capacitor" of the track-and-hold section of the converter imme-

diately traps a charge on the sample capacitor which is representative of the input signal. The binary representation of the value of the charge is then determined. The number of master clock cycles necessary for this determination to occur is a function of the number of bits of the converter and the particular mode of operation (loopback or asynchronous). The occurrence of the  $\overline{\text{EOC}}$  (end of conversion) signal indicates that the conversion time is complete. The converter must then acquire a new sample of the input signal for the next conversion. The coarse-charge and fine-charge times accomplish this. First to occur is the coarse-charge phase. A buffered version of the analog input signal is first connected to the sample capacitor. The input impedance of the buffer is very high and therefore does not load the input signal source. The output of the buffer is connected via switches S2 and S3 to the sample capacitor (switch S1 is open). The buffer (Figure 7a, A1) furnishes the majority of the current necessary to charge the capacitor toward the new voltage value. The buffer therefore reduces the transient current demand from the signal source if the input signal has changed from the value previously stored on the sample capacitor. The sample capacitor is connected to the output of the buffer for six cycles of the master clock (CLKIN)

frequency. At the end of the six cycles the coarse-charge phase is complete. The sample capacitor is then directly connected to the analog input signal for the fine-charge phase (Switches S1 and S3 are closed, S2 is opened). Immediately before being connected for the fine-charge phase, the voltage on the sample capacitor may still differ slightly from the analog input value. This is due to the offset voltage of the buffer amplifier (A1). This offset voltage is typically 50 mV but may be up to 150 mV in the worst case. At the beginning of the fine-charge phase a small transient demand of current from the external signal source may occur as the capacitor charges to its final value. The fine-charge phase will last until the hold command becomes active again. In loop-back mode the fine-charge phase lasts nine master clock cycles until the end of track (EOT) signal reactivates the hold command. When the hold command is activated asynchronously, the fine-charge phase should last a minimum of nine master clock cycles and may continue indefinitely until the hold command is activated.

Simplified models of the impedances seen by the analog input signal are depicted in Figures 7b and 7c. For the conversion and coarse-charge phases, the impedance seen at the AIN pin is the input impedance of the buffer A1. This impedance is approximately 100 M $\Omega$  shunted by 15

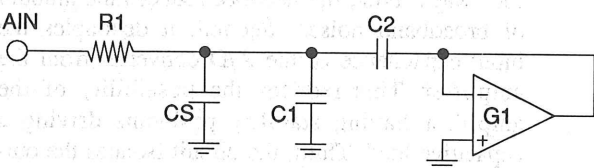


Figure 7c Simplified Input Model During Fine-charge.

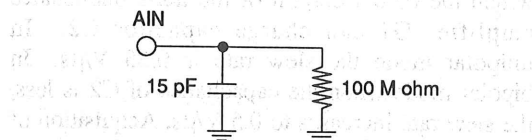
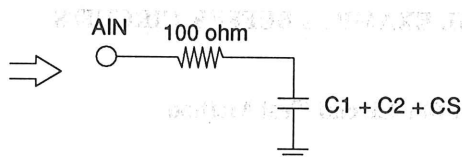


Figure 7b. Simplified Input Model During Coarse-charge / Conversion

pF. When in the coarse-charge phase the sample capacitor is charged by the buffer (A1) output. The speed at which the voltage on the sample capacitor can track the input signal is limited to the rate at which the buffer output current can charge the capacitor. The slew rate of the buffer is 5 V/ $\mu$ s when the converter is in unipolar mode and 10 V/ $\mu$ s when in the bipolar mode. The reason for the difference is that the sample capacitor in bipolar mode is only half the value of that in unipolar mode.

The simplified model of the impedance seen in fine-charge is that of Figure 7c. Resistor R1 is the effective resistances of the S1 and S3 CMOS analog switches of Figure 7a. The sample capacitor consists of C2, whereas capacitor C1 and CS are stray capacitance. G1 is a transconductance amplifier with an effective input resistance of about 35  $\Omega$  at DC. The slew rate in the fine-charge mode is limited to the rate at



	C1	C2	CS	R1	Gin
Unipolar	170 pF	170 pF	20 pF	100 ohm	35 ohm
Bipolar	85 pF	85 pF	30 pF	100 ohm	35 ohm

which the output current of the transconductance amplifier G1 can charge capacitor C2. In unipolar mode the slew rate is 0.25 V/ $\mu$ s. In bipolar mode when the capacitance of C2 is less, the slew rate increases to 0.5 V/ $\mu$ s. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during the conversion cycle or during the coarse-charge cycle since at these times the slew rate of the converter input is faster. It should be noted that in fine-charge, any external impedance on the AIN pin becomes part of the total network and will contribute to the settling time response characteristics.

Also, Figure 7a shows that when switches S1 and S3 are turned on (S2 is off) in the fine-charge phase, the source impedance of the external circuitry connected to the AIN pin actually becomes part of the feedback network of amplifier G1. The external circuitry should offer an impedance less than 400  $\Omega$  at frequencies greater than 2 MHz or amplifier G1 may oscillate.

The input circuitry of the analog front end of the A/D converter uses CMOS analog switches which are similar to analog switches available in individual integrated circuits. The resistances of the CMOS switches, such as shown in Figure 7c, exhibit non-linear effects with changes in signal amplitude and frequency. These dynamic changes in switch characteristics are a source of distortion at high frequencies.

### III. EXAMPLE BUFFER CIRCUITS

#### Buffer Circuit Test Method

Several example buffer circuits have been constructed and tested. Evaluation was restricted to dynamic testing at room temperature (25° C). The testing was performed using a CDB5016 evaluation board connected to an IBM compatible computer via a 16-bit parallel I/O card. Signal processing software developed at Crystal

was used to evaluate the data. The signal source was a Khron-Hite 4400A Low Distortion Oscillator modified to produce low broadband noise per the article in Reference 1 (Reprints available from Crystal upon request). The oscillator was adjusted to the appropriate full-scale value for each circuit. A frequency of 1.5 kHz was chosen as the test frequency.

The output data from the A/D converter was processed to yield three indicators of dynamic performance. These are:

- 1) S/(N+D): The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (except DC), including distortion components.
- 2) S/D: The ratio of the rms signal value to the ratio of the rms sum of all harmonics.
- 3) S/PN: The ratio of the rms signal value to the rms value of the next largest spectral component below the Nyquist rate (except DC).

#### Benefits of an RC Isolation Network

All of the example circuits show an RC network coupling the output of the buffer to the input of the A/D converter. The 200  $\Omega$  resistor and 1 nF capacitor network enhance circuit operation in four ways. First, the network reduces the amount of broadband noise. Second, it decouples the input capacitance of the A/D converter from the amplifier. This reduces the possibility of the amplifier having stability problems driving a capacitive load. Third, the circuit isolates the output of the amplifier from the high frequency pulsed charge effects of the sampling front end of the A/D converter. And finally, the passive network offers a well-behaved low source impedance to the internal transconductance amplifier, satisfying its stability needs. The component values are chosen to have a time constant

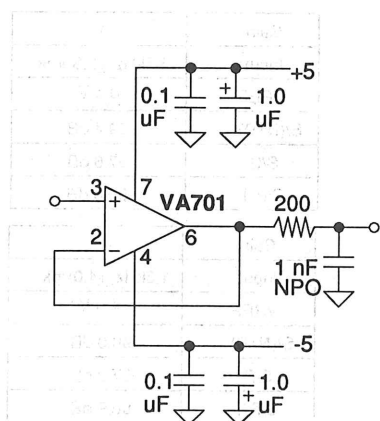


Figure 8 : VA701 Noninverting Amplifier

Gain	1
Input	1.5kHz, $\pm 3.5$ Vpk
VREF	3.5 V
S(N+D)	90.7 dB
S/D	100.0 dB
S/PN	103.0 dB

of 200 ns to provide appropriate settling time when the converter (16 bits) is sampling at 50 kHz. The NPO dielectric characteristic minimizes the effect of voltage coefficient of capacitance which can adversely affect performance at the 16-bit level. Other dielectrics may be adequate while some may result in non-linear capacitance with signal level and therefore introduce distortion. Empirical testing may be necessary to insure whether a given dielectric is adequate for a particular application.

### $\pm 5$ Volt Supply Op Amp Circuits

The first example circuit is a unity gain buffer circuit shown in Figure 8. The VA701 op amp (from VTC, Inc.) is designed for operation from  $\pm 5$  V power supplies. The input common mode range of the amplifier is specified as  $\pm 3.5$  V, therefore the reference voltage for the A/D converter was set to use +3.5 V as its full scale reference value. The circuit yields quite good results when the reduced signal level is considered.

The second circuit, Figure 9, configures the VA701 in the inverting mode. The minimum

output voltage swing for the VA701 is specified as  $\pm 3.5$  V (2 k $\Omega$  load) with a typical range of  $\pm 4.0$  V. The voltage reference for the A/D converter was adjusted accordingly. The difference in the amplifier capability between the two signal levels was not very significant. The lower amplitude signal had more noise while the higher level signal had slightly more distortion.

### $\pm 15$ Volt Supply Op Amp Circuits

Most precision operational amplifiers are specified for operation from  $\pm 15$  V supplies. Figure 10 shows an OP-27 used to reduce signal levels of  $\pm 10$  V to  $\pm 4.5$  V. The performance is excellent. Figure 11 then shows the OP-27 in the non-inverting configuration.

The performance levels being achieved with the OP-27 result from operating the amplifier well within its specifications for input range and output amplitude capability. The Signetics NE5534A worked equally well in both circuit configurations (Figures 10 and 11). Note that low value resistors are used to minimize the component noise in the circuits.



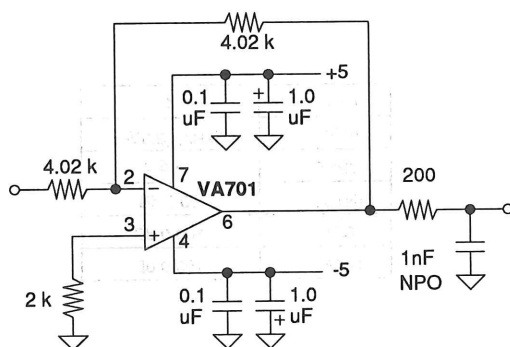


Figure 9. VA701 Inverting Amplifier

If an OP-27 type amplifier is used, the inverting circuit is preferred for signal processing applications. This is because some brands of OP-27 amplifiers exhibit much higher distortion at frequencies above 10 KHz or so when used in the non-inverting configuration. It may be that the internal bias current cancellation circuitry does not track the input stage well when subjected to the rapidly-varying (high frequency) common mode voltages such as those experienced by the positive gain configuration.

### Achieving $\pm 4.5$ Volt Output with $\pm 5$ Volt Supplies

Some amplifier designs may require a minimum number of supplies, yet still want to take advantage of the full dynamic range of the A/D converter when using a 4.5 V reference. The Signetics NE5534A op amp, known to be excellent for audio use, can be combined with a discrete transistor output stage to yield excellent results when using only  $\pm 5$  V supplies. Figure 12 illustrates the NE5534A in the inverting configuration, reducing a  $\pm 10$  V signal to  $\pm 4.5$  V. The OP-27 (without the external compensation capacitor) yielded similar noise and distortion

results but had slightly slower rise time when tested with a transient input.

### An Instrumentation Amplifier Circuit

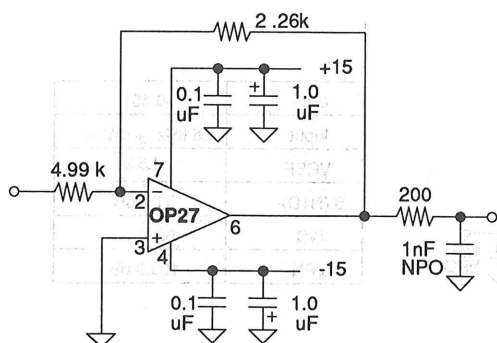
Some systems require an instrumentation amplifier front end. One instrumentation amplifier was tested; the AD625C from Analog Devices. The data sheet specifies a maximum nonlinearity of 0.001%. Although the device may have good static linearity, its dynamic performance was well below 16-bit performance. The AD625C, shown in Figure 13, was tested with two different gains. The instrumentation amplifier was tested with a gain of one, and then with a gain of nine. The gain of nine configuration is with the 5 k resistor connected to pins 2 and 15. The data indicates that the part actually has greater distortion (indicative of greater non-linearity) in the lower gain configuration.

### Signal Limiting Circuits

When utilizing op amps with  $\pm 15$  V supplies to drive A/D converters with  $\pm 5$  V supplies it is possible under certain input conditions for the

Gain	-1
Input	1.5kHz, $\pm 3.5$ Vpk
VREF	3.5 V
S/(N+D)	89.4 dB
S/D	97.6 dB
S/PN	99.6 dB

Gain	-1
Input	1.5kHz, $\pm 4.0$ Vpk
VREF	4.0 V
S/(N+D)	90.0 dB
S/D	97.3 dB
S/PN	98.9 dB



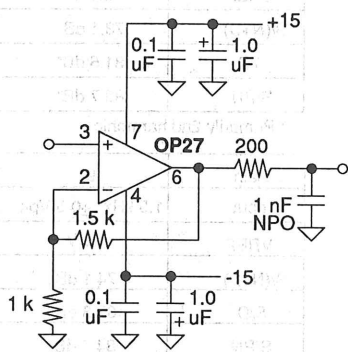
Gain	-0.45
Input	1.5kHz, ±10Vpk
VREF	4.5 V
S(N+D)	91.8 dB
S/D	100.5 dB
S/PN	102.6 dB

Figure 10. OP-27 Inverting Amplifier

amplifier output voltage to attempt to exceed the supply rails of the converter. As described previously, the converter has protection diodes at the analog input and therefore will clamp the voltage whenever the signal forward biases the diodes. If high current amplifiers are used, excess current from the amplifier may damage the converter. If excess current is a possibility, then the voltage swing of the amplifier must be limited so as to not exceed the supplies of the converter; or some means of current-limiting must be used. Many amplifiers have current limiting circuitry as part of their output stage and will limit their output current if a fault condition exists. Even though the amplifier may protect itself in this manner it

may not be desirable from a system performance point-of-view. System measurement accuracy can be degraded due to offset and gain errors which occur as a result of amplifier self-heating.

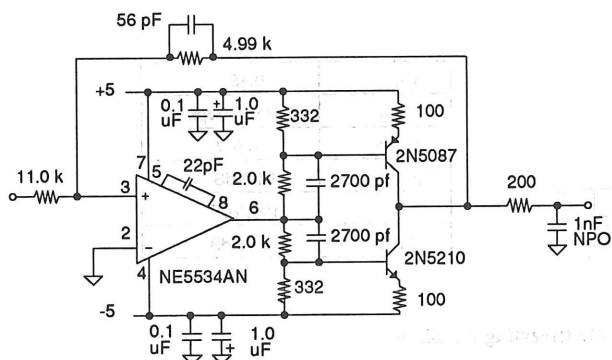
Several approaches to amplifier output limiting can be used. Zener or diode bounding circuits can be used. Some bounding circuits reduce the circuit gain by reducing the effective feedback resistance when an overvoltage signal exists. Others limit the signal by shunting it to ground when it exceeds the desired amplitude. Reference 6 documents some of these circuits and discusses their strengths and weaknesses.



Gain	+2.5
Input	1.5 kHz, ±1.8 Vpk
VREF	4.5 V
S(N+D)	90.7 dB
S/D	98.0 dB
S/PN	102.3 dB

Figure 11. OP27 Noninverting Amplifier





Gain	-0.45
Input	1.5 kHz, $\pm 10$ Vpk
VREF	4.5 V
S (N+D)	91.7 dB
S/D	99.7 dB
S/PN	103.3 dB

Figure 12. Op Amp with Transistor Buffer Stage

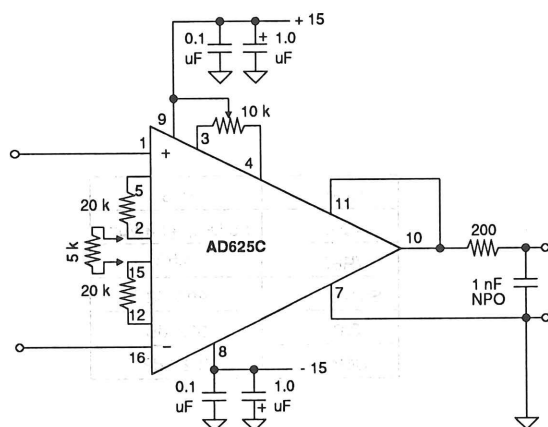
### Voltage Clamping via the Compensation Pin

Figure 14 indicates a simple means of clamping available on some op amps. Illustrated is a Harris HA-2600 with diodes connected to its compensation pin (8). The  $\pm 5$  V supplies of the A/D converter provide the clamp voltage reference values for the diodes. The output stage of the HA-2600 has unity voltage gain but high current gain. The signal on pin 8 of the amplifier is a low current signal of identical amplitude to the output signal. Limiting of the output signal swing

is accomplished by clamping the signal at pin 8 to the desired level. Even if the on voltage of the clamp diodes on the op amp exceed the on voltage of the clamp diodes inside the A/D, the 200  $\Omega$  resistor will limit the current to an acceptable level.

### A Novel Method to Aid Current Limiting

Another method of protecting the A/D converter from excess signal conditions is illustrated in Figures 15 and 16. The circuits make use of addi-



Gain	1
Input	1.5 kHz, $\pm 4.5$ Vpk
VREF	4.5 V
S/(N+D)	73.1 dB
S/D	81.5 dB*
S/PN	83.7 dB*

\* Primarily 2nd harmonic

Gain	9*
Input	1.5 kHz, $\pm 0.5$ Vpk
VREF	4.5 V
S/(N+D)	74.1 dB
S/D	87.3 dB
S/PN	84.7 dB

\* 5 K resistor connected

Figure 13. Instrumentation Amplifier

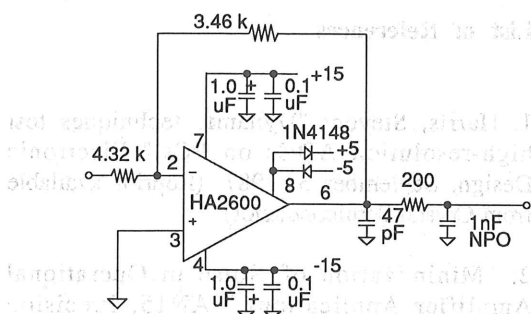


Figure 14. Compensation Pin Clamping

tional series resistance between the op amp and the converter to limit the amount of signal current available. The resistor is placed inside of the feedback loop of the amplifier where the loop gain of the circuit reduces the effect of the 1 kΩ resistor under normal operating conditions. When a fault condition exists, the signal output from the amplifier may attempt to exceed the power supply rails of the A/D converter. Under this condition the current into the A/D converter input will be limited to less than 10 mA by the 1 kΩ resistor.

The added 1 kΩ resistor increases the open loop output impedance of the circuit. This increase in output impedance adversely affects the effective open loop gain of the circuit when driving lower impedance loads. Therefore, it is desirable to take

advantage of op amps with higher open loop gains. Decompensated op amps offer greater gain-bandwidth products but with the restriction that they are generally specified to be stable only with higher gain configurations. For example, the OP-37 is specified for operation with a minimum gain of 5 but offers higher open loop gain than the OP-27 (about 15 dB higher at 10 kHz). The circuits in Figures 15 and 16 take advantage of the added open loop gain of the OP-37 yet still meet the requirements for stability demanded by the amplifier. At low frequencies (below 10 kHz) the loop gain of the circuit reduces the effect of the 1 kΩ resistor significantly. At the same time the effective load to the amplifier output (including the 1 kΩ output resistor) is dominated by the feedback resistor. At high frequencies (above 1

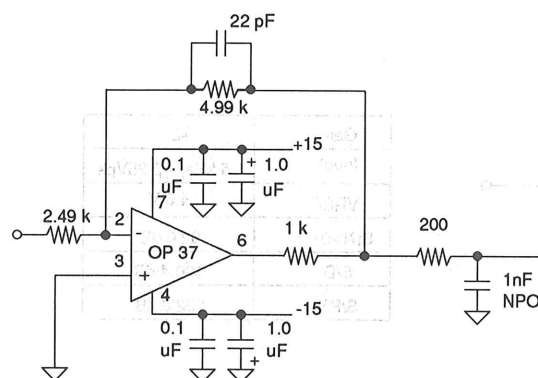


Figure 15. Inverting Amplifier with current limiting

Gain	-0.8
Input	1.5 kHz, ±5.6Vpk
VREF	4.5 V
S/(N+D)	90.5 dB
S/D	97.0 dB
S/PN	98.1 dB

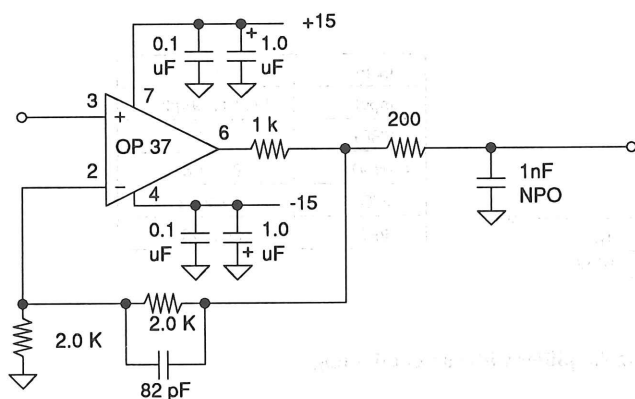
Gain	-2
Input	1.5kHz, ±9Vpk
VREF	4.5 V
S/(N+D)	91.2 dB
S/D	97.9 dB
S/PN	99.2 dB

MHz) the impedance of the 1 nF capacitor in the output filter begins to look like a short circuit therefore the load seen by the op amp circuit is dominated by the RC filter network. At the higher frequencies the open loop gain of the op amp is decreasing. The corresponding reduction in loop gain allows the effect of 1 k $\Omega$  resistor to begin to take effect, increasing the output impedance to the feedback node. The combined effect of the higher output impedance due to the 1 k $\Omega$  resistor and the loading effect of the 200  $\Omega$  resistor causes an effective loop gain reduction of about  $200/(1000 + 200)$  or a factor of 6. This gain reduction in combination with the phase compensation of the feedback capacitor allows the circuit to maintain stability while it also provides current limiting under fault conditions.

This application note has discussed the making of a good buffer circuit and has illustrated several examples with relevant test data. For further information on design and dynamic testing of amplifier circuits refer to the following references.

### List of References

1. Harris, Steven: "Dynamic techniques test high-resolution ADCs on PCs," Electronic Design, September 3, 1987. (Reprint available from Crystal Semiconductor)
2. "Minimization of Noise in Operational Amplifier Applications," AN15, Precision Monolithics, Inc.
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7. Roberge, James K.: Operational Amplifiers: Theory and Practice, John Wiley and Sons, New York, 1975.
8. Dostal, J.: Operational Amplifiers, Elsevier/North-Holland, New York, 1981



Gain	+2
Input	1.5 kHz, +2.25Vpk
VREF	4.5 V
S(N+D)	92.0 dB
S/D	100.4 dB
S/PN	102.8 dB

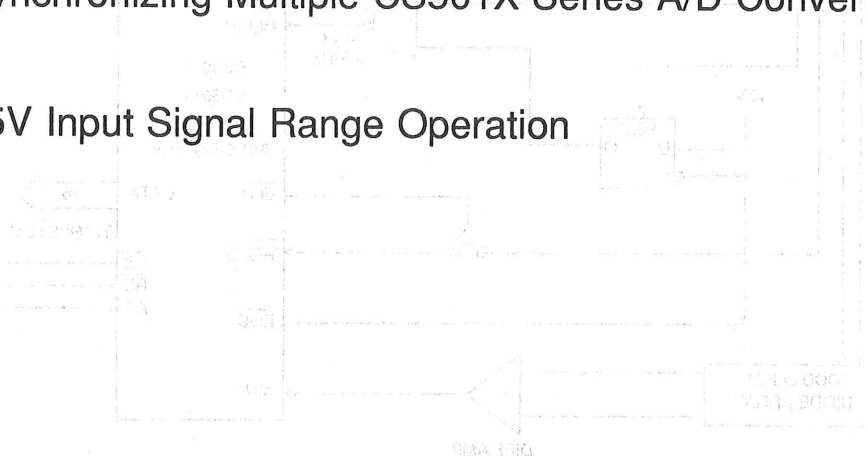
Figure 16. Noninverting Amplifier with Current Limiting

## Application Note

### A Collection of Application Hints for the CS501X Series of A/D Converters

By Jerome Johnston

- Jam ADC into Coarse Charge for High Slew Signals
- Single Control Input Acts as a "Start Convert" Command
- Synchronizing Multiple CS501X Series A/D Converters
- $\pm 5V$  Input Signal Range Operation



Here are several application hints which extend the flexibility of the CS501X series of A/D converters.

### Jam ADC Into Coarse Charge For High Slew Signals

The CS501X family of A/D converters have within their capacitor-based architecture a track-and-hold function. Upon completing a conversion the A/D converter immediately begins to track the input signal. The design is such that the input signal is buffered (internal to the A/D) from the capacitor array for six cycles of the master clock. Then the buffer is bypassed and the array is directly connected to the AIN pin of the converter. This allows the converter to settle to its final value within the accuracy specifications. The period of time that the buffer is connected is known as the coarse charge time. The time when the buffer is bypassed to sample the input signal directly is known as fine charge time. Slew rate capability during coarse charge time is much

greater than the slew rate in fine charge. Any step changes of the input signal should occur either prior to or during the coarse charge time. Under normal operation, once the converter has completed the coarse charge time and entered into the fine charge time it will stay in the fine charge state until the  $\overline{\text{HOLD}}$  input goes low. When  $\overline{\text{HOLD}}$  goes low the charge on the capacitor array is immediately trapped and conversion begins.

In applications which exhibit step changes in the input signal, it is not desirable that the converter remain waiting in the fine charge mode (with its slower slew rate capability). Extending the coarse charge time allows the ADC to track high slew signals.

Figure 1 depicts the logic by which the master clock to the converter is stopped during the coarse charge time to lock the converter into coarse charge. At the end of each conversion the End of Conversion (EOC) signal indicates the

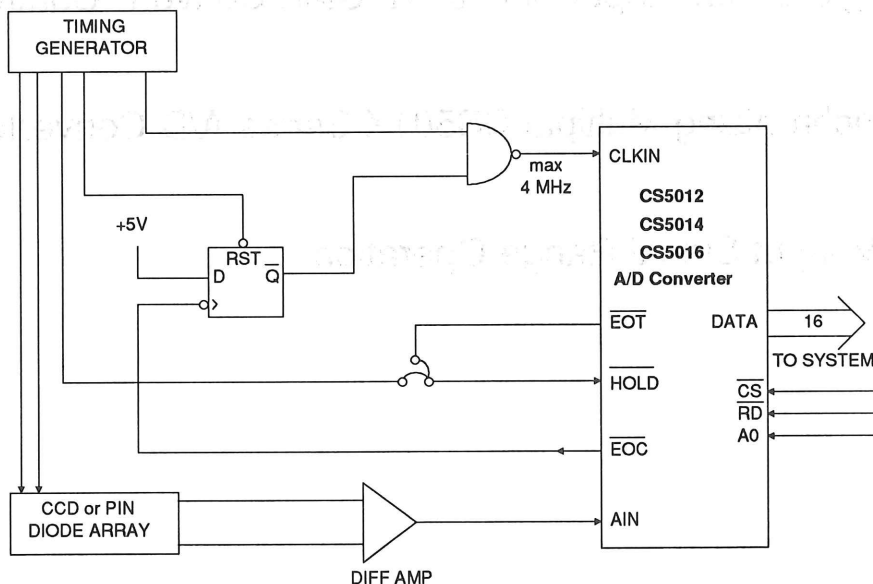


Figure 1. Sample Logic Jams Converter into High Slew Rate Mode

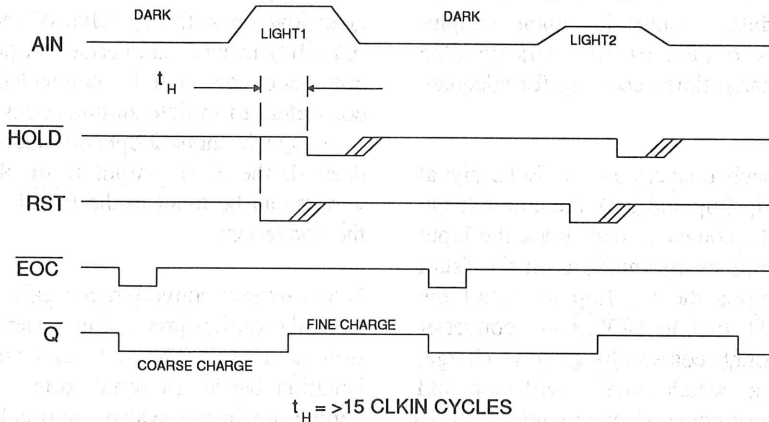


Figure 2. Extending Coarse Charge Time Allows Tracking of Dark to Light Transition

end of a conversion and the beginning of a coarse charge time. EOC falling toggles the flip-flop, causing its Q output to go low. This jams the NAND gate output high which locks the converter into the coarse charge mode until the timing generator circuitry resets the flip-flop.

Figure 2 illustrates the timing of the various signals of the circuit in Figure 1. CCD or PIN diode array outputs exhibit step changes in their signal levels as each array element is selected for output. After each conversion the converter is stopped in the coarse charge mode until the video output signal from a particular element of the sensor array is stable. The clock to the A/D converter is then restarted. The converter then proceeds through the coarse and fine charge times and awaits a HOLD signal. If the EOT output of the converter is tied to the HOLD conversion will begin as soon as the track time is complete.

While this coarse charge jamming circuit is designed to operate with the CS501X series of converters, note that the CS5101 A/D converter offers a CRS/FIN (coarse/fine) pin as an input to allow user control of the tracking mode.

### Creating a Single "Track, Hold, and Convert" Command

The coarse charge jamming circuitry of Figure 1 is altered to allow a single control line to initiate a sample and convert sequence. First, the EOT output from the converter must be directly tied to

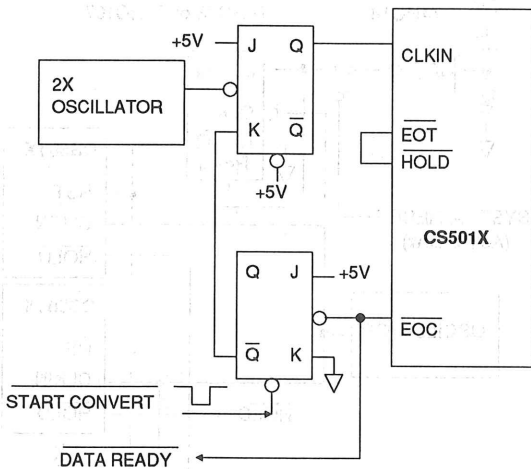


Figure 3. Coarse Charge Jamming with "StartConvert" Control

**HOLD** input. This connection will enable the converter to initiate a conversion upon completion of 9 clock cycles of fine charge (the minimum fine charge time necessary for adequate settling).

At the end of each conversion the **EOC** signal will toggle the flip-flop and lock the converter in coarse charge. The converter will track the input signal in the coarse charge mode until the "start convert" input resets the flip-flop to restart the clock. With **EOT** tied to **HOLD** the converter will proceed through coarse charge, fine charge, and conversion at which time it will stop and await another "start convert" command. Data in the output port will remain available until a new start convert command is issued, but due to internal logic, the port cannot be read in the byte-wide (**BW** = 0) mode.

Figure 3 illustrates an example of the "start convert" circuitry using a dual J-K flip-flop. Note that the input clock is twice that required by the converter and that the low time of "start convert" pulse should be less than the conversion time of the converter. The "start convert" signal should be held low during calibration.

### Synchronizing Multiple CS501X Series A/D Converters

Simultaneous sampling of several channels is often required. For example, in measurements of the outputs of three-axis magnetometers or three-axis inclinometers it is desirable that all three signals be simultaneously sampled and then converted. Because the CS501X converters offer very good repeatability from part to part they can yield very good channel to channel measurement correlation even though each channel is converting with its own A/D converter.

Figure 4 illustrates how multiple CS501X series converters can be synchronized, allowing simultaneous sampling. The circuit uses a flip-flop to synchronize a reset (**RST**) signal common to all

of the A/D converters such that the reset signal goes low on a falling edge of the master clock (**CLKIN**) to each converter. A common **HOLD** command can then be connected to all of the converters to initiate simultaneous sampling. Or, if the synchronous loopback mode of sampling is desired, the **EOT** output from one of the converters can be input to the **HOLD** inputs of all of the converters.

When several converters are galvanically isolated from the digital processing system, synchronization is useful. The data is passed across the isolation barrier in serial form. If several converters are in the system, normally both **SDATA** and **SCLK** signals from each converter are passed across the isolation barrier. However, if the converters are synchronized, the **SDATA** outputs of several converters can be clocked into serial to parallel registers on the digital side by sending a single **SCLK** signal across the barrier.

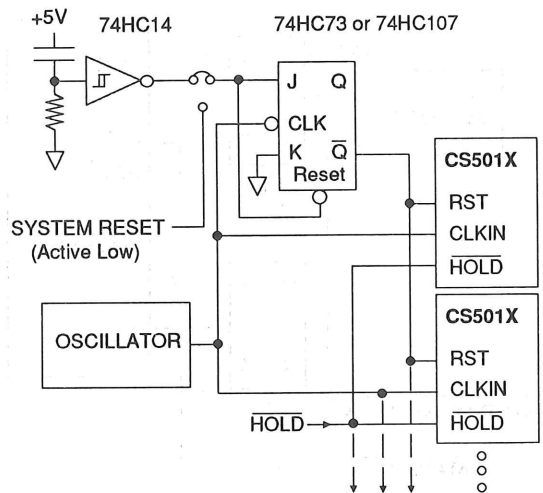


Figure 4. Controlled Reset for Synchronization of Multiple Converters

### ± 5V Input Signal Range Operation

Some system specifications may require signal levels of  $\pm 5$  V. Operating the CS501X series of A/D converters with  $\pm 5$  V signals requires a 5 V reference and therefore the supplies have to be raised. The supplies should be adjusted to output voltages in the range from 5.3 to 5.5 volts. The positive and negative supplies should be of equal magnitude and the system connections recommended in the A/D converter data sheet should be maintained.

An easy means of achieving the proper supply voltages is to use LM317L and LM337L regulators. These devices are acceptable as the power requirements of the A/D converter are very low. See Figure 5 for the appropriate resistor values to set the regulator voltages. An alternative is to use LM78L05AC and LM79L05AC regulators with adjustment resistors to increase their output voltages. This is illustrated in Figure 6.

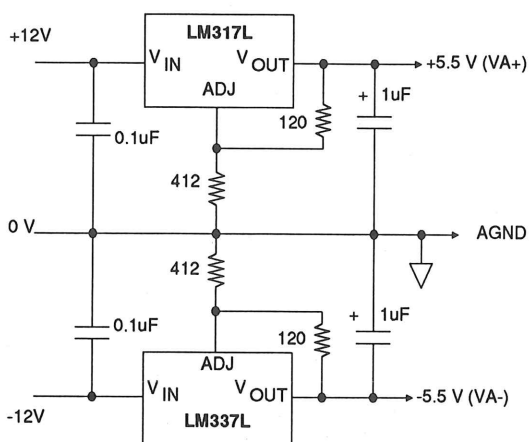


Figure 5. LM317L/LM337L Voltage Regulators

References which output 5 V require a minimum input voltage from 6.5 to 11 volts. This increased voltage is necessary to accommodate the 1 to 6 volt input to output voltage differential needed by the reference. Supply voltages of +12 V or +15 V are common. Care should be exercised to insure

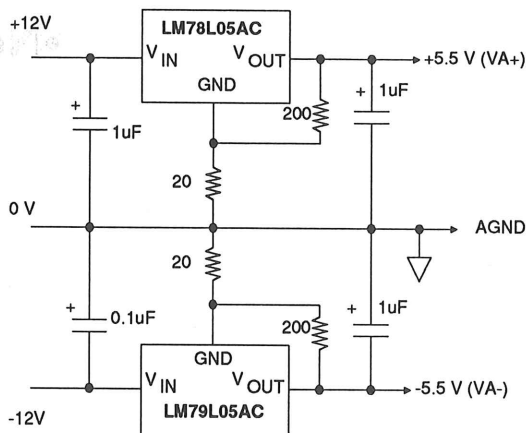
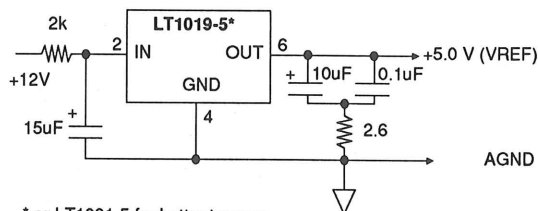


Figure 6. LM78L05/LM79L05 Voltage Regulators

that the voltage reference output does not source current into the A/D converter VREF pin before the power supplies on the A/D are established. One means of insuring this is to add an RC filter in front of the voltage reference as illustrated in Figure 7. This will delay the reference output until the regulated supplies (Figure 5 or 6) for the A/D are established.

With raised supply voltages on the A/D converter, the digital outputs will output logic 1's with a higher output voltage ( $V_{OH}$ ). To accommodate this increase the digital logic in the system can use 74HC4049 or 74HC4050 logic level translators to restore the logic outputs back to the 5 V level. Alternatively, the logic system (if 74HC logic is used) can also use a supply voltage elevated to the value of the A/D supply. This problem is also eliminated if the ADC is isolated using opto-couplers.



\* or LT1021-5 for better tempo.  
or LT1019-4.5 for 4.5V output

Figure 7. 5V Reference with RC Input Delay



# Notes

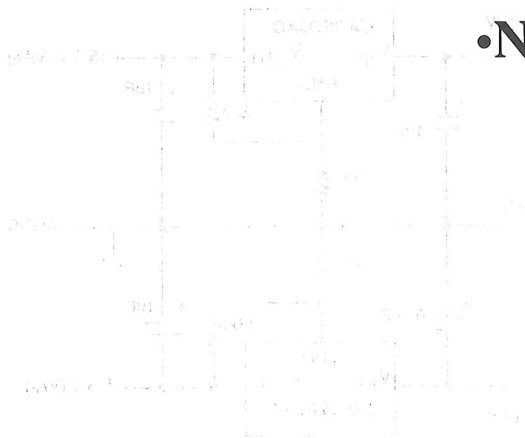
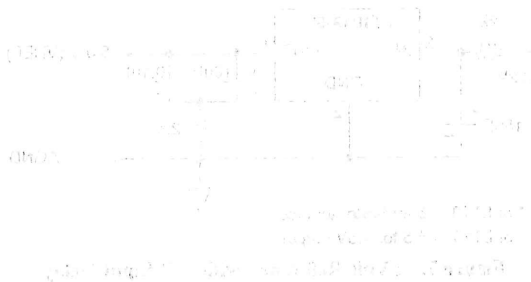


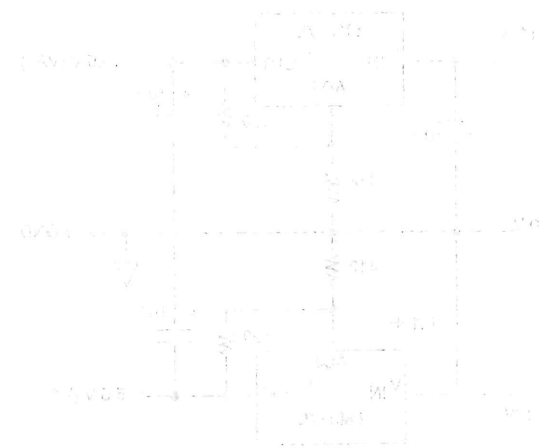
Figure 1 shows the typical application circuit for the CS501X. The crystal is connected between pins 1 and 2. Pin 3 is connected to ground. Pin 4 is connected to a 10k resistor, which is then connected to a 10V supply. Pin 5 is connected to ground. The crystal is labeled 'CRYSTAL' and has a frequency of '32.768 kHz'.

The CS501X is a low-power, high-precision, 32.768 kHz crystal oscillator. It is designed for use in a wide range of applications, including timekeeping, data logging, and communication systems. The device is available in a 5-pin package, which is shown in Figure 1. The typical application circuit for the CS501X is shown in Figure 1. The crystal is connected between pins 1 and 2. Pin 3 is connected to ground. Pin 4 is connected to a 10k resistor, which is then connected to a 10V supply. Pin 5 is connected to ground. The crystal is labeled 'CRYSTAL' and has a frequency of '32.768 kHz'.



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## Self-Calibrating Analog-to-Digital Converter Chips Overcome Laser-trim Technology Limitations

By Jerome E. Johnston, Crystal Semiconductor Corp., Austin, Texas

Innovation has always been the lifeblood of leading technology companies. Semiconductor companies release a constant barrage of new products into the marketplace each year. Many of these new semiconductor products provide new and better building blocks for hybrid circuit designers. Other semiconductors provide monolithic solutions which encroach on the hybrid circuit marketplace.

Many monolithic innovations render hybrid solutions either technically obsolete or no longer cost competitive. Therefore it is wise for hybrid circuit manufacturers to stay in tune with recently introduced semiconductor products. Each semiconductor product introduction needs to be examined as to its impact on the hybrid circuit marketplace. The new semiconductor product may present a new product opportunity for the hybrid manufacturer, or it may render a current hybrid solution obsolete.

Analog-to-digital converters (ADCs) are a prime example. Whereas hybrid vendors supplied the industry's first packaged 12-bit ADC solutions, today there are dozens of 12-bit monolithic solutions from which customers can choose. Many of these monolithic solutions provide no better specifications than the hybrid solutions they have unseated, yet they win because of lower cost. Newer monolithic solutions are appearing with resolutions of 14, or 16 bits and beyond. While the prevailing technology of most of these new monolithic ADCs relies on laser-trimmed thin film technology, some of the new ADCs utilize digital self-calibration circuitry. This calibration circuitry adjusts the sizes of the DAC elements incrementally to insure ratiometricity and does not require any laser trimming. These self-calibrating converters are available as 12, 14 and 16-bit devices.

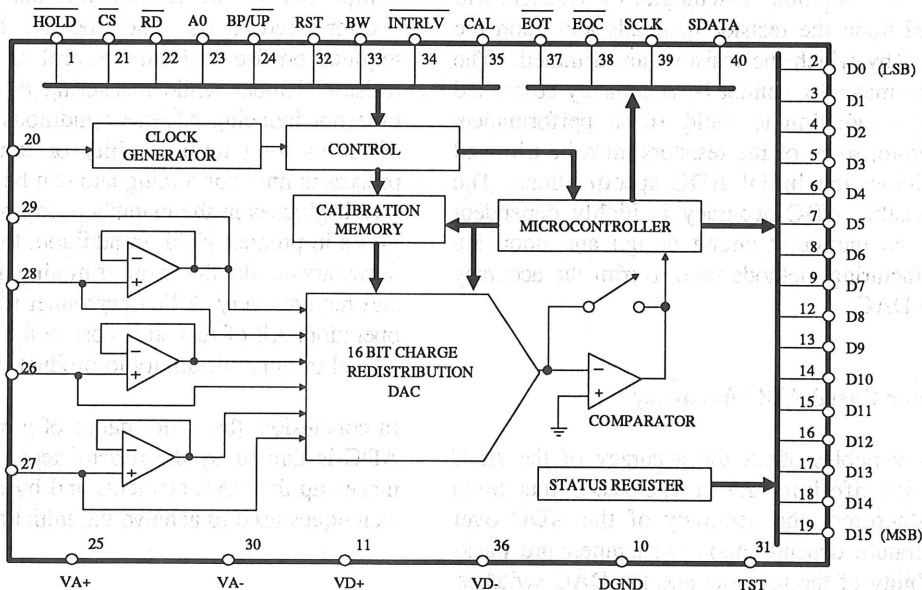


Figure 1. Block diagram of a monolithic 16-bit self-calibrating ADC.

## **Self-Calibrating Converters**

How will this monolithic self-calibrating technology impact the hybrid ADC marketplace? Let's examine the technology and assess its potential effects on the hybrid circuit marketplace by asking several questions: How are self-calibrating ADCs different from the current hybrid ADC technology? Do self-calibrating ADCs contain any significant technological advantages? Does this self-calibrating technology present a crisis, or an opportunity for new innovation? Only by addressing each of these questions can the hybrid ADC supplier develop an ADC product strategy for the future.

How are self-calibrating ADCs different from the current hybrid A/D converter technology? The majority of current hybrid ADCs utilize the SAR (successive-approximation register) architecture. To achieve their specifications, these hybrid ADCs rely upon resistor-based DACs as the core element of the A/D converter. The performance of the A/D converter itself is dependent upon the matching of the resistors and the switches used in the DAC. The initial matching of the resistors will depend upon the resistor materials and upon the method by which the resistors are trimmed. The resistor matching cannot be adequately controlled during deposition to yield 16-bit performance. Therefore, some of the resistors must be trimmed to achieve the initial ADC specifications. The achievable ADC accuracy is highly dependent upon the particular circuit design and upon the manufacturing methods used to trim the accuracy of the DAC.

## **Resistor Based ADC Accuracy**

Many variables affect the accuracy of the ADC over its lifetime. After the ADC has been manufactured, the accuracy of the ADC over temperature depends upon the temperature tracking ability of the resistors and the DAC switches. The thermal tracking capability will depend upon

such things as the particular resistor materials being used, the type of switches used, and how well the circuit is laid out to minimize the effects of thermal gradients. The resistor materials themselves have inadequate thermal stability and inadequate thermal tracking to achieve the required accuracy in a 16-bit ADC, especially over large temperature spans. Therefore, to achieve 16-bit performance over temperature using resistor based technology is "a tough nut to crack".

Long-term ADC accuracy will depend upon the aging characteristics of the particular components. Several phenomenon affect the aging process. The characteristics of the resistor materials change with time. This aging phenomenon is accelerated with elevated temperatures. While the aging characteristics of the resistor material itself is somewhat predictable, its aging characteristics may be adversely affected if the resistor is laser-trimmed. While laser trimming is the process by which the initial accuracy of the ADC is achieved, it may detrimentally affect the long term stability.

The laser-trimming process adds a major order of complexity to the design and manufacture of resistor-based ADCs. The process is difficult as it requires precise real-time control of trimming a resistor element while measuring it, at the same time not inducing adverse conditions which may affect its long term stability or reliability. The process is time-consuming and can be very expensive if glitches in the manufacturing process cause losses in product yield. In addition, the equipment necessary to do the laser trimming is expensive and requires very skilled personnel for set-up and operation. All of this adds cost to the product and a level of unpredictability to product yield.

In conclusion, the performance of a resistor-based ADC is limited by the resistor technology which makes up the DAC elements and by the trimming techniques used to achieve the initial accuracy.

## Capacitive-Based ADCs

In contrast to this, the self-calibrating SAR ADCs use capacitive-based DACs. The DAC elements in these monolithic devices require no trimming at the factory. These ADCs contain algorithms in microcode which calibrate the ratiometric weighting of the DAC elements upon command. Figure 1 illustrates an example of a 16-bit self-calibrating ADC. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. Figure 2 illustrates the capacitor array and DAC comparator. All capacitors share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF by means of CMOS analog switches.

When the ADC is not calibrating or converting, all capacitors are tied to AIN forming  $C_{tot}$  (Figure 3a). Switch S1 is closed and the charge on the array,  $Q_{in}$ , tracks the input signal voltage on the AIN pin. When the conversion command is issued, switch S1 opens (Figure 3b). This traps the charge  $Q_{in}$  on the comparator side of the capacitor array and creates a floating node at the comparator's input. During conversion the algorithm operates on this fixed charge. In effect, the entire capacitor array serves as a sample capacitor when connected to the AIN signal, and as an analog memory during conversion, much like a hold capacitor in a sample/hold amplifier. For this reason the ADC needs no external sample/hold circuitry.

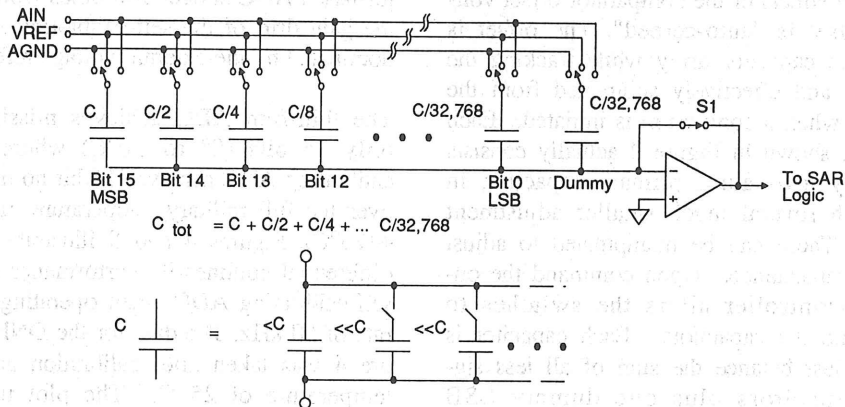


Figure 2. Capacitor Array and Comparator

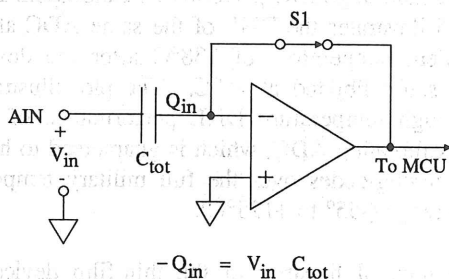


Figure 3a. Capacitor Array While Tracking Input Signal.

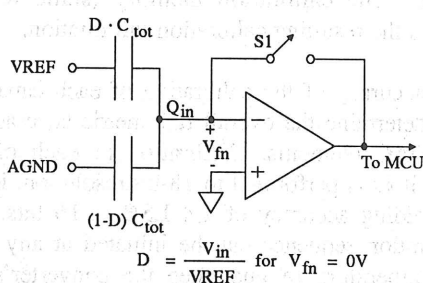


Figure 3b. Capacitor Array While Converting.

During the successive-approximation conversion algorithm the free plates of the capacitor array elements are manipulated to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance (labelled D in Figure 3b) which, when connected to VREF (the voltage reference) will drive the voltage at the comparator input to zero. That binary fraction of the capacitance represents the converter's digital output.

Achieving accurate conversions at 16-bits clearly depends upon the accuracy of the comparator and the ratiometric weighting of the capacitors. To minimize the effects of the comparator offset voltage, the offset is "auto-zeroed". The offset is stored on the capacitor array while tracking the input signal and effectively subtracted from the input signal when a conversion is initiated. Each bit capacitor shown in Figure 2 actually consists of a slightly low-valued primary capacitor, in parallel with several much smaller adjustment capacitors. These can be manipulated to adjust the overall capacitance. Upon command the on-chip microcontroller alters the switches to precisely ratio the capacitors. Each capacitor is adjusted to just balance the sum of all less significant capacitors plus one dummy LSB capacitor (for example,  $16C = 8C + 4C + 2C + C + C$ ). The calibration memory (static RAM) retains the resulting calibration information.

The accuracy of the calibration of each capacitor will determine the overall ratiometric accuracy of the DAC elements. Calibration of each of the capacitors is performed to 18-bit resolution, ideally yielding accuracy of 1/4 LSB at 16 bits. The calibration sequence can be initiated at any time or temperature to guarantee the converter's accuracy, even long after the device leaves the factory.

### **Comparison of Resistor Based vs. Capacitor Based A/D Converters**

Do Self-Calibrating ADCs offer any significant technological advantages? Just how well does this self-calibrating technology compare to current hybrid resistor-based ADCs of similar speed and resolution? Table 1 compares the specifications of a typical 16-bit thin-film type SAR converter (including sample/hold amplifier) with a 16-bit monolithic self-calibrating ADC. The initial bipolar zero error of the thin-film device is 16 times worse than the self-calibrating ADC. The gain error of the resistor-based device is over 20 times worse than the same error in the self-calibrating ADC. Likewise, bipolar zero drift of the thin-film ADC is 25 times worse than the self-calibrating ADC while the gain drift of the resistor-based ADC is over 100 times worse (Note that the gain drift of the self-calibrating ADC will be dominated by the external voltage reference drift).

The thin-film ADC achieves missing codes to only 14 bits ( $0^{\circ}$  to  $70^{\circ}\text{C}$ ) whereas the self-calibrating ADC achieves 16 bit no missing codes over the full military temperature range ( $-55^{\circ}$  to  $+125^{\circ}\text{C}$ ). Figures 4 and 5 illustrate the superior differential nonlinearity performance of the 16-bit self-calibrating ADC when operating at a sample rate of 50 kHz. The data for the DNL plot of Figure 4 was taken after calibration at an ambient temperature of  $25^{\circ}\text{C}$ . The plot illustrates the 18-bit (1/4 LSB at 16 bits) resolution to which the self-calibrating ADC performs its calibration. Figure 5 illustrates the DNL of the same ADC at an ambient temperature of  $138^{\circ}\text{C}$  after the device was self-calibrated at  $25^{\circ}\text{C}$ . The plot illustrates the high temperature DNL performance of the self-calibrating ADC, which is guaranteed to have no-missing-codes over the full military temperature range ( $-55^{\circ}$  to  $+125^{\circ}\text{C}$ ).

The integral linearity of the thin-film device is specified at 0.003%, but only at a temperature of  $25^{\circ}\text{C}$ . At  $70^{\circ}\text{C}$  this linearity may degrade to be as poor as 0.01%. The integral linearity of the self-

**Table 1**  
**Comparison: 50 kHz ADCs with S/H Amplifier**

Type of ADC	16-bit Thin-Film ADC <sup>A</sup>	16-bit Self-Cal ADC <sup>B</sup>
Specified Operating Temperature Range	0 to 70°C	-55 to +125°C
Bipolar Zero Error	±500 ppm max.	±30 ppm max.
Bipolar Zero Drift	±5 ppm/°C max.	<0.2 ppm/°C <sup>1</sup>
Gain Error	±1000 ppm max.	±45 ppm max.
Gain Drift	±20 ppm/°C max.	<0.2 ppm/°C <sup>1,2</sup>
Minimum Resolution for which No-Missing-Codes is Guaranteed	14 bits <sup>3</sup>	16 bits <sup>4</sup>
Integral Linearity Error	0.003% max. <sup>5</sup>	0.0015% max.
Integral Linearity Drift	Not Specified	0.02 ppm/°C <sup>6</sup>
Power Dissipation	900 mW typ.	120 mW typ.

**Notes:**

- A. AD1380-KD Analog Devices
- B. CS5016-TD16 Crystal Semiconductor
- 1. Less than 40 ppm total change for -55 to +125°C after calibration at 25°C.
- 2. Gain drift will be dominated by the off-chip voltage reference.
- 3. For 0° to +70°C.
- 4. For -55° to +125°C.
- 5. Specified only at 25°C.
- 6. Typically ±3.8 ppm total drift over the entire -55° to 125°C range.

calibrating ADC is specified at 0.0015% with only minor degradation over the military temperature range. Figure 6 illustrates the superior spectral performance of the self-calibrating device. The data for the FFT plot of Figure 6 was taken at 138°C after calibration at 25°C. The signal/distortion ratio (99.32 dB) indicates the superb integral linearity of the device. Signal/(noise + distortion) performance for the ADC in the same test exceeded 91 dB. Power dissipation for the thin-film device is over 7 times greater than the 120 mW of the monolithic device.

As can be seen from this comparison, self-calibrating ADCs have stepped ahead of currently available laser-trimmed hybrid ADCs when comparing A/D converters of similar speed and resolution. The self-calibrating ADCs have particular advantages in that they include the sample and hold function and work very well over the entire military temperature range (-55° to

+125°C). In addition, the calibration mechanism is "on-chip" and available to the user. In contrast, laser-trimmed devices leave their calibration station at the factory. Therefore after being manufactured, the accuracy on the thin-film ADC will change with the effects of aging, possibly not meeting initial specifications within six months after manufacture. In contrast, the monolithic self-calibrating ADC chip can be recalibrated at any time or at any temperature to meet its data sheet specifications over the full life cycle of the product in which it is used.

Having the self-calibration circuitry on-chip adds another particular advantage to users of the ADC in die form. It is very difficult for semiconductor manufacturers to fully test the operational parameters of an analog die. Generally, only limited testing of the die can be performed. Manufacturers of resistor-DAC die have a tough job. The dice suffer from limited yield in that it

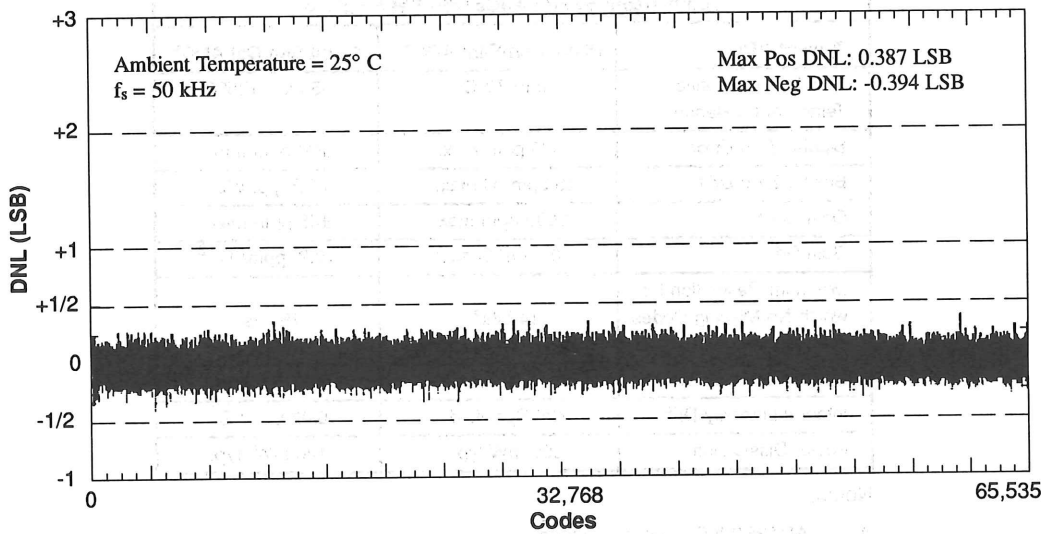


Figure 4. Differential nonlinearity plot of 16-bit self-calibrating ADC after calibration at 25° C.

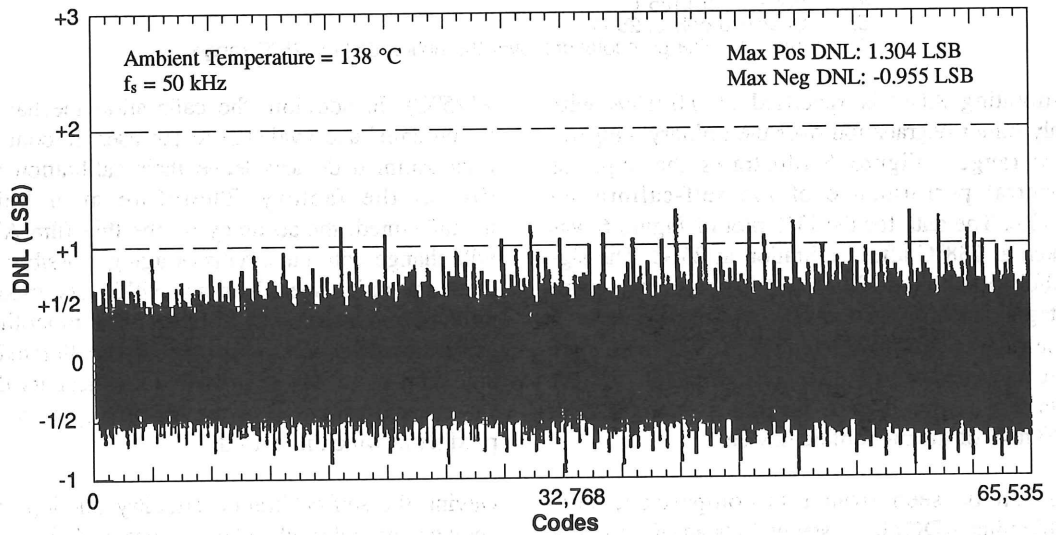


Figure 5. Differential nonlinearity plot of 16-bit self-calibrating ADC operating at an ambient temperature of 138° C.



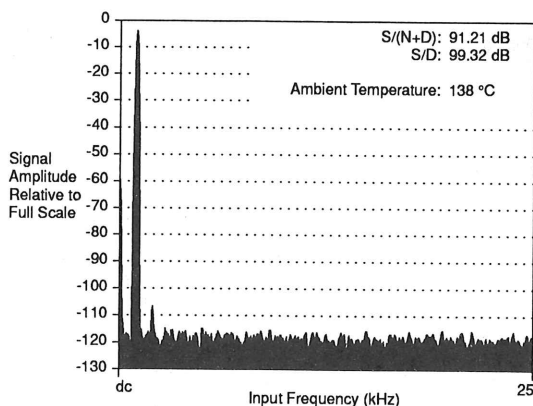


Figure 6. FFT plot with 1 kHz full scale input

is difficult to accurately trim them while still part of a silicon wafer. And even if they are trimmed perfectly at the wafer probe station, there is no way to be certain that they will meet specification after they are mounted and packaged.

Generally, a hybrid manufacturer who uses resistor-based DACs will suffer yield fall-out at final product test and will have to keep extra dice on hand for rework.

Self-calibrating die overcomes these problems. In the self-calibrating ADC the self-calibration function is primarily a digital circuit and can be easily verified for proper operation at the wafer probe stage. Once it can be verified that the self-calibration circuitry is functional, it is highly probable that the die will meet its performance specifications.

This offers at least two advantages over resistor-based DACs in die form. First, there is a higher probability that the self-calibrating die will truly meet its performance specifications after wafer probe. This gives the user of the die more yield for a given number of dice purchased than one normally expects from laser-trimmed die. Second, the on-chip self-calibration removes the yield uncertainty brought about by die stress when the die is mounted and packaged. Self-calibration over-

comes this yield fall-out because the chip self-calibrates after it is packaged.

Another advantage of the self-calibrating ADC chip is that the entire A/D function, except for the voltage reference, is on the same die. The die includes the sample/hold function, the DAC capacitors, switches, comparator, and successive-approximation register, the calibration microcontroller, SRAM, on-chip oscillator, and parallel output port. Current resistor-based designs require multiple chips to implement an equivalent system function.

### Conclusion

Self-calibrating ADC chips do offer hybrid manufacturers a number of significant technological advantages over resistor-based technology, in particular, better performance and higher yield.

Does this self-calibrating technology present a crisis, or an opportunity for new innovation? For some there is a crisis! Monolithic self-calibrating ADCs are displacing current hybrid ADCs in many customer applications. Still, there remains the opportunity for hybrid manufacturers to innovate in the ways they have always done: assemble the best available components into a packaged "total solution".

Future hybrid ADCs can be enhanced over current thin film technology by including a monolithic self-calibrating device as the core of the design. The self-calibrating die can be assembled together with crystal clock, voltage reference, and analog multiplexers to build system level solutions which exceed the performance capability of current products. The resulting hybrid can be more easily designed and manufactured than a laser-trimmed solution, while at the same time resulting in a better product at an equal cost. As the future unfolds, self-calibrating ADCs will offer many opportunities for innovation in future hybrid ADC solutions.



## •Notes•

# Dynamic techniques test high-resolution ADCs on PCs

**Steven Harris**

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Since the analog-to-digital converter is typically the key component in a data-acquisition or digital signal-processing system, confirming the performance of a-d converters is paramount during the design-evaluation phase. But testing each part to 16-bit accuracy at full conversion speed and over the military temperature range poses several problems. The test setup must be faster and more accurate than the a-d under test. Test engineers at an IC manufacturing plant must carefully observe shielding, use separate analog and digital grounds, and control impedance lines. This is possible on the bench, but for production testing, where the environment is noisy and lead lengths are long, testing such converters is a nightmare.

A test fixture is one way a-d users can simplify the process. The fixture, which connects with an IBM PC, exercises the device under test (DUT) with a variety of conditions. The most significant tests show the histogram distribution for Differential Non Linearity (DNL) and Integral Non Linearity (INL), and Fast Fourier Transform (FFT) frequency analysis. The personal computer collects and processes the output data-words of the DUT.

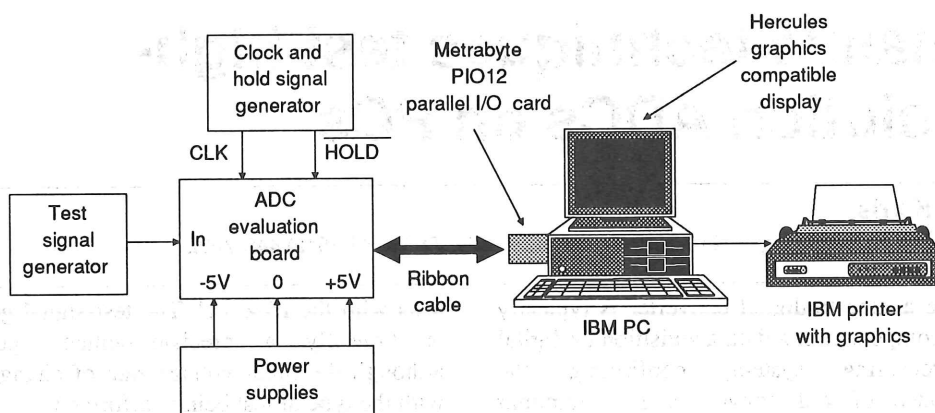
While manufacturers like Crystal Semiconductor offer an evaluation circuit board, which has a socket for the a-d converter, along with BNC connectors for inputs and ribbon cable headers for outputs, other manufacturers are not as generous and designers must roll their own. The test setup (Fig. 1) can be used for both histogram and FFT

tests with the IBM PC. The test-signal generator is typically a precision-voltage generator, although the input voltage rate of change varies with the type of test being performed.

With histogram techniques, for example, the a-d converter is presented with a full-scale, slow-ramp input. The ramp proceeds slow enough for the converter to take several samples at each voltage level. The object is to build up a statistical picture of the analog-to-digital accuracy, using averaging to remove the effects of noise. The more samples taken at each voltage level, the more accurate the statistical picture will be, although it penalizes memory and computer run time.

Where the input signal is slow enough to generate about 100 samples at each level, the resolution of DNL measurements will be within 0.01 LSB; good enough for most engineers. Test times are long, however: 100 counts multiplied by 65,536 codes at a conversion rate of 50 kHz gives 2.18 minutes of data capture and process time.

In test system operation, software running on the PC collects each output code and then increments a counter associated with collected code. All counters are zeroed at the start of the test. At the end, codes with a larger than average number of counts must be wider than ideal. Codes with less than the average number of counts must be narrower than they should be. Codes that have zero counts are considered missing codes.



**1. With IBM PC-based testing, a common computing tool is right for multiple tests. The test setup is inexpensive and the results are easily repeatable**

This information may be scaled and offset so that a perfect code gives a value of 0 LSB DNL error while a code that is 0.5 LSB too wide gives a result of +0.5 LSB DNL error. The numbers for the entire range of codes may be plotted out as DNL error vs. code (Fig. 2)

Simple Fortran routines to average, scale and offset the numbers to give DNL in LSBs as follows:

```

AVERAGE = TOTAL NUMBER OF
CONVERSIONS/2**N
DO 10 I = 1,2**N
DNL(I) = [IN ARRAY(I)/AVERAGE]-1
10 CONTINUE
  
```

where IN ARRAY(I) equals the number of count values in each code, and N is the number of bits in the a-d converter.

In theory at least, the same set of numbers gives DNL values can also generate integral non linearity (INL) information.

Currently other tests for checking dc accuracy are used: usually the dc servo method, which forces the input voltage to generate a particular code.

This method is good for spot checking certain codes but is very slow and says nothing about the dynamic performance of the ADC.

Alternatively, a sine wave may be input to the a-d converter, resulting in a histogram which is not flat. Instead, the graph has a density-function envelop dependant on a sine probability curve. This may be calculated in software and therefore corrected. The DNL graph will then accurately represent the DUT, not the input signal characteristics. It is easier to generate a 16-bit accurate sine wave than a 16-bit linear ramp. Fortunately, an accurate sine wave is exactly the test signal required for frequency domain FFT-based testing.

When presenting a very pure sine wave to an a-d and performing a Fourier analysis on the resulting sequence of numbers, the result should be just one frequency component: the input sine-wave frequency. Other components represent the lack of purity of the input signal, lack of linearity in the a-d converter, measurement artifacts, and noise. The a-d converter can be tested in real time. As a result, there is no need to extrapolate dynamic performance from static dc linearity specs.

For these tests, the test-signal generator (Fig. 1) is replaced with a Krohn-Hite 4400A sine-wave generator. A filtering and buffering circuit (Fig. 3) is inserted between the signal generator and the a-d converter to reduce the Krohn-Hite output noise. Similarly, the HOLD & CONVERT command to the a-d converter must be derived from a low jitter clock source, otherwise the resulting frequency spectrum will be corrupted. Jitter in the clock source looks like aperture jitter in the on-chip sample/hold. Since this aperture jitter is very low, <100 ps, it is very important to have a low jitter sample clock to gain the best performance from the a-d converter.

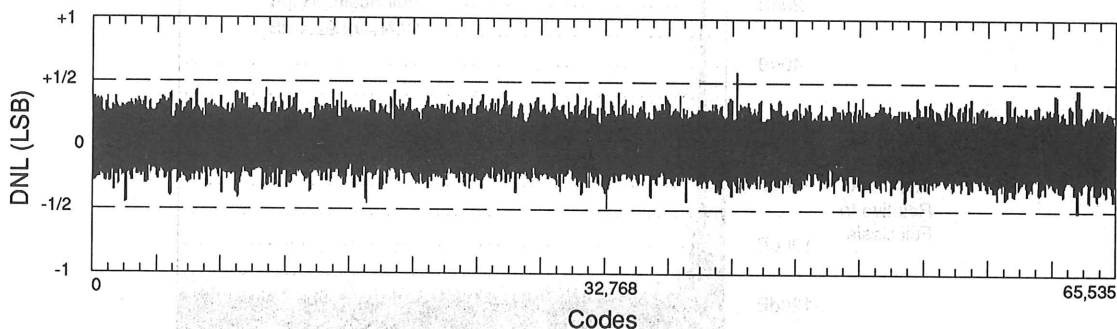
In operation, 1024 consecutive numbers from the a-d are captured. Before FFT processing, the data sequence is multiplied by a "window function." This forces the first and last values to be zero, which helps the FFT algorithm "link up" repetitions of the input record without generating effective transients. The alternative would be to synchronize the sampling clock to the input sine wave (a very difficult task at the 16-bit level).

There are many window functions in FFT processing. The main trade-off is between frequency resolution and the amplitude of the distortion effects introduced by the window. A window whose distortion side-lobes are low in amplitude will also spread out the frequency components. One suggestion is to use a Blackman Harris window for harmonic distortion analysis.<sup>1</sup>

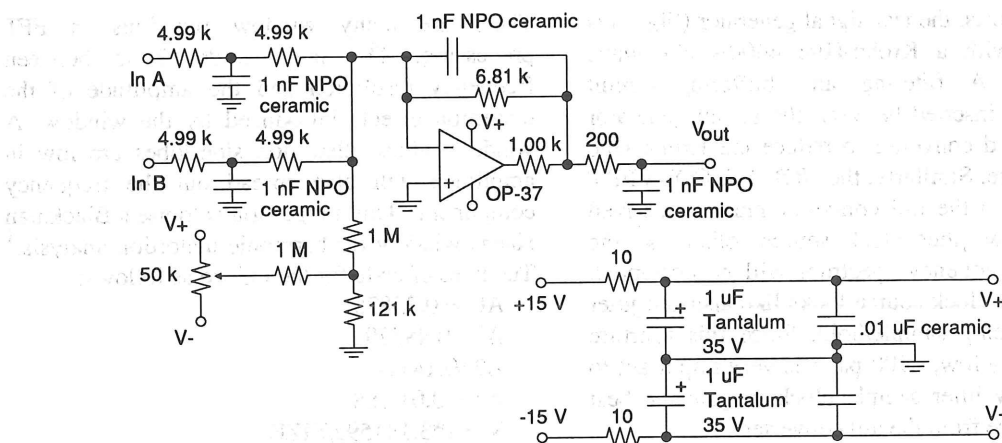
The lines of code for the PC are as follows:

```
AO = 0.35875
A1 = 0.48829
A2 = 0.14128
A3 = 0.01168
V = 2*3.141592/SIZE
DO 5 I = 1,SIZE
M = I-1
CUMUL(I) = JAY(I)*
&(AO-(A1*COS(V*M))+(A2*COS(V*2*M)-
&(A3*COS(V*3*M)))
5-CONTINUE
```

where SIZE is the number of points in the input array (1024), JAY(I) is the input data, and CUMUL(I) is the windowed data. The actual FFT algorithm used is given in an IEEE manual.<sup>2</sup>



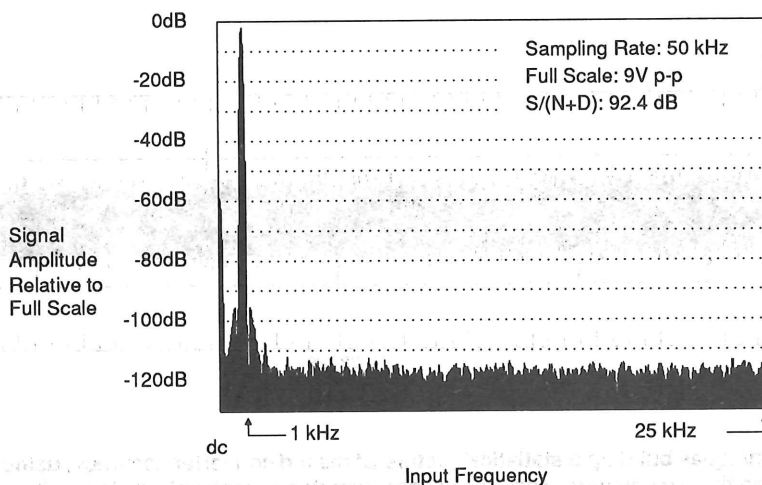
2. Histogram techniques build up a statistical picture of the a-d converter accuracy, using a full-scale, slow ramp input so the a-d converter can take several samples at each voltage level. The ideal output codes can then be plotted against the ideal codes to reveal DNL error. Pictured is the Crystal Semiconductor CS5016 16-bit CMOS a-d converter with a conversion rate of 16  $\mu$ s.



3. A noisy, but spectrally very pure, Krohn-Hite 4400A signal generator is made significantly quieter by this filter circuit. Also, the 200  $\Omega$  output resistor and 1 nF capacitor offer the ideal source impedance for Crystal Semiconductor's CS501X-CSZ511X family of a-d converters.

Several useful results may be gleaned from the FFT output. One is the spectrum plot. The FFT plot of the CSZ5116 is Crystal's dynamically specified and tested self-calibrating 16-bit a-d converter. (Fig. 4).

Signal-to-distortion ratio may be calculated by comparing the input sine-wave level with the sum of all the harmonics. Signal to noise may also be calculated; however the window artifacts, in particular the sidelobes on either side of the fundamental, have to be removed and replaced with a predicted average value.



4. The use of a Blackman Harris window function for 16-bit analog-to-digital evaluation points out distortion components and the noise floor for a 16-bit successive approximation a-d converter (Crystal's CSZ5116). The plot runs from dc to 25 kHz, with the converter running at a 50-kHz sampling rate.

Readily available is the signal to noise plus distortion value; a very useful single figure of merit.

IBM PC-based testing has a speed limitation. Most PC's can only input data at up to 50 kHz (maybe 100 kHz). A device like Crystal Semiconductor's new CS5212, a two-stage flash a-d converter with 12 bits, runs at 1 MHz throughput; much too fast for a PC to handle. One solution, which still allows for use of the PC-based software, is to buffer the data. There are two requirements: for FFT testing, a simple 1024-by-12 fast buffer memory is all that is required. For histogram DNL testing, where typically over 5 million samples are taken, a very large buffer memory may put to work.

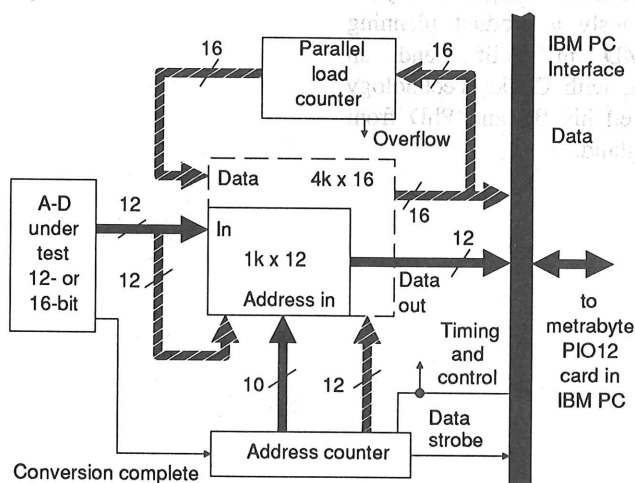
However, it is better to use a so-called "histogramming memory", where additional hardware logic is needed to count the codes as they occur. This avoids the need to store each code value (Fig. 5).

The solid lines show the data flow when the board is used as a 1k-by-12 buffer. Before data

capture, the address counter is zeroed. On command from the PC, consecutive a-d samples are written to consecutive memory locations, while the conversion-complete signal increments the address counter.

After the 1024 samples are captured, the address counter is zeroed again and this time incremented by the pc. Consecutive memory locations are read from the memory into the computer.

The broken lines show the data flow when the board is used as a histogramming memory. In accumulating counts for each possible code, the memory has to be 4096 locations (for a 12-bit a-d converter). Sensible choices for word width include 8, 12, or 16 bits. Ideal for ramp input testing, 8 bits make possible a maximum count of 255. A 12-bit word width is good because it is the same width as the FFT buffer mode; 16 bits is also good, particularly for sine wave input histogram testing, when the minimum and maximum codes count may well approach 65,535.



**5. Flash a-d converter testing is made possible with a buffer memory board. A hardware histogramming architecture makes it possible to count code occurrences, avoiding the need to store the actual codes.**

One excellent method of generating the necessary timing pulses to read the memory, load the counter, clock the counter, and then write back to the memory, is to use a pair of ones clocked through a parallel output shift register. In this way, the hardware accumulates a histogram of the code occurrences. The parallel load-counter overflow may be used to stop acquisition, or acquisition may be controlled from the PC. To read the histogram into the PC, the address counter is clocked by the PC, in a similar fashion to reading the FFT data. The histogram numbers may then be scaled and processed to give DNL in LSBs.

1.F.J. Harris, "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform Processor." *Journal of the IEEE*, Vol 66, No.1, Jan 1978.

2. *Programs for Digital Signal Processing*, edited by the Digital Signal Processing Committee, IEEE Acoustics, Speech, and Signal Processing Society (IEEE Press).

Steven Harris is application manager at Crystal Semiconductor. Previously a product planning management at AMD in Calif., and an independent consultant with Cooke Technology in England, he received his BS and PhD from Sussex University, England.

## **Application Note**

### **CDB5501 to IBM-PC Serial Interface (using BASIC)**

By Jerome Johnston and Steven Harris

The CDB5501 Evaluation Board supports easy evaluation of the CS5501 A/D converter. Included on the evaluation board is an RS-232 type line driver (MC145406) which allows the UART-compatible mode of the CS5501 to transmit data to an RS-232 port of a computer.

This application note documents the appropriate configuration of the CDB5501 board to interface to the RS-232 serial port of an IBM compatible computer. A Basic program listing to read the port and display the data in HEX format is included.

The CDB5501 has many jumper selection options. The jumpers should be placed in the following positions to configure the evaluation board in the proper operating mode for RS-232 transmission.

- P1 INT CLK
- P2 "1" (2.45 MHz clock)
- P3 "12" (1200 baud)
- P4 "1"
- P5 AC mode
- P9 "DC"
- P11 "BC"

These jumper selections set the evaluation board to operate from the on-board 4.9152 MHz oscillator. The oscillator is divided by two to provide CLKIN signal to the CS5501 at 2.45 MHz. The CS5501 is operating in the Asynchronous Communication mode with an output rate at 1200 baud. The decimation counter is used to provide some "dead-time" between each transmission of two bytes of data.

To connect the DB-25 connector on the CDB5501 evaluation board to the serial input (RS-232 compatible) of the IBM compatible computer a cable must be provided. To insure proper operation the cable should provide straight-through connections for pins 2-8 and pin 20.

A program listing written in GW Basic is provided. The program reads the input data from the serial port of the computer and then displays the received binary information in HEX format on the computer screen. The software assumes the input is into communications port COM1. The software prompts for the baud rate. A baud rate of 1200 should be entered unless the CDB5501 jumper selection is modified to provide some other baud rate.



The Basic program is not complex. Lines 90-93 give some opening comments with line 94 prompting for the baud rate. Your reply will enter a baud rate for the text string defined in line 96. Line 96 defines a text string which sets up the data format and control line status of the COM1 serial port. In line 100 the text string is then used to open a data buffer for the port into which six bytes are read as defined in lines 150-340. Each character is then converted to HEX characters for display on the screen in line 350. Line 365 then

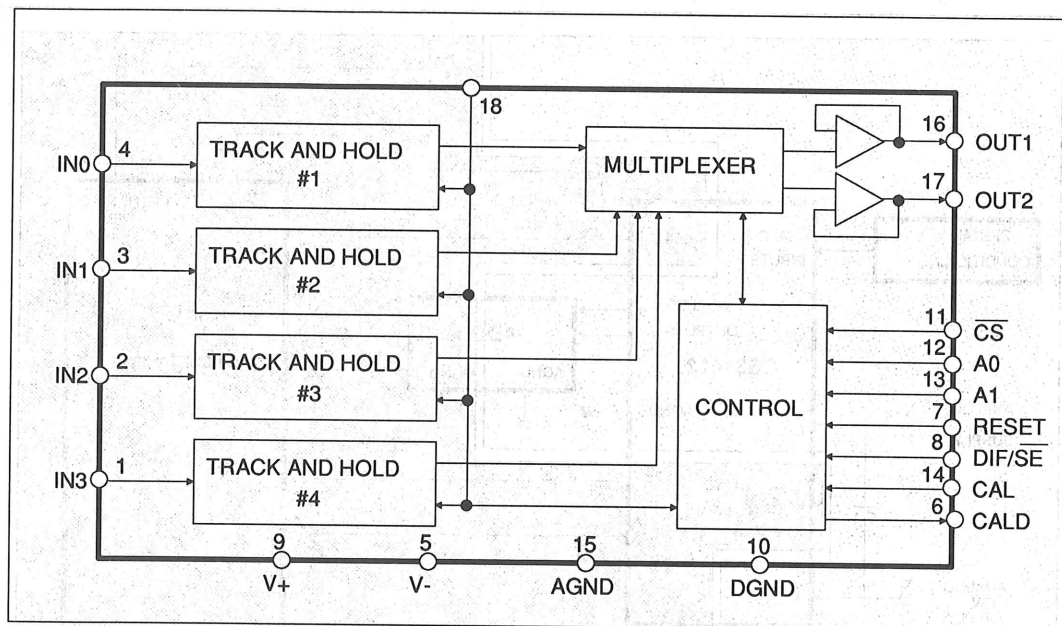
prints the HEX characters on the screen. Use of the port is then terminated by closing the data buffer in line 370. Note that the buffer must be opened and closed to cause the serial port control lines to follow the proper sequence necessary to read each set of six characters. The program will cause the computer to continuously read the port unless line 380 is commented out or deleted. If line 380 is deleted, the program will read six characters and pause with a prompt to continue.

```
90 PRINT "5501COM - DISPLAYS SERIAL DATA FROM CDB5501"
92 PRINT "Crystal Semiconductor VER1.0 5/8/88 Steve Harris"
93 PRINT "Uses COM1:"
94 INPUT "Baud rate ?","BR$"
96 COMFIL$="COM1:" + BR$ + ",N,8,2,RS,CS,DS,CD"
100 OPEN COMFIL$ AS #1
150 FIELD 1,6 AS D$
300 GET #1,6
340 FOR N = 1 TO 6 STEP 1
350 PRINT HEX$(ASC(MID$(D$,N,1))); " ";
360 NEXT N
365 PRINT
370 CLOSE #1
372 FOR K = 1 TO 10
374 NEXT K
380 GOTO 100
400 INPUT "Quit OR Continue";A$
410 IF A$ = "Q" THEN GOTO 10000
420 GOTO 100
10000 END
```

## Application Note

### Suggested Grounding and Supply Arrangements for the CS31412

by  
Steven Harris



## APPLICATION NOTE

### *CS31412 Quad Track and Hold Amplifier Recommended Grounding and Supply Arrangements*

The CS31412 connections fall into 6 classes: analog inputs, analog outputs, non time-critical digital inputs, digital outputs, power supplies, and the hold signal. The fundamental guideline to follow is to think carefully about the currents flowing due to the above 6 classes of signals, and keep them separate.

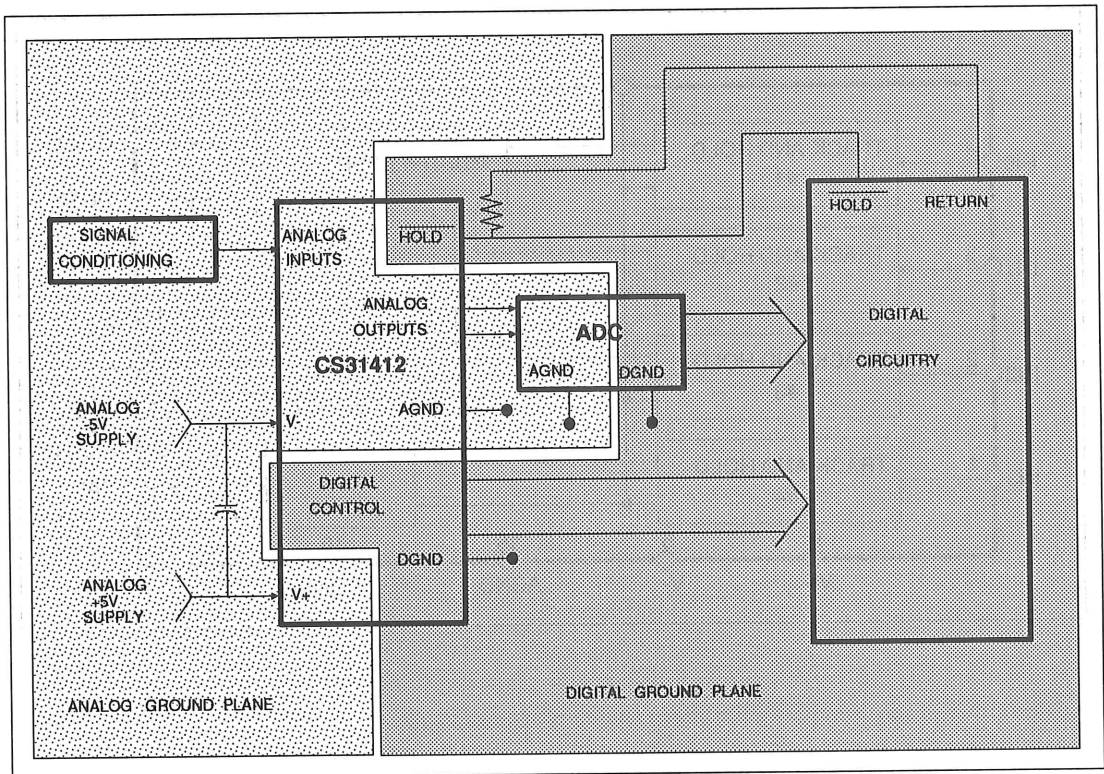
A good layout scheme will:

a) Keep digital signal noise from the analog output.

- b) Obtain the best possible accuracy.
- c) Minimize the aperture jitter.
- d) Minimize power supply noise affecting the output.

The following guidelines will help to achieve these goals:

- 1) Have separate analog and digital grounds. Only join these grounds together at one place, typically either at the power supply or at the ADC.
- 2) Decouple the part with a  $10\mu\text{F}/0.1\mu\text{F}$  capacitor combination connected between  $V+$  and  $V-$ , as near to the part pins as possible
- 3) Group all of the non time-critical digital signal traces together and keep them separated from the analog signals. Also use digital ground traces to



**CS31412 SUGGESTED GROUND PLANE LAYOUT**

isolate this group of traces from the other signals.

- 4) The high input impedance of the part on the analog input pins results in a very small input current. Nevertheless, if termination resistors are used, the return currents for each resistor should be kept separate to avoid introducing crosstalk
- 5) Connect the loads to the analog outputs such that the return currents do not flow in any input related ground leads.
- 6) Typically the hold signal will be terminated to ground near to the CS31412. This gives a clean edge and also minimizes the absolute amplitude of the hold signal. Both the hold signal and its return current trace should be brought back to the pins of the part generating the signal.

The figure shows a possible ground plane layout, concentrating on the area around the CS31412.

**Notes:**

- 1) The CS31412 is grossly out of scale. It is enlarged to highlight the grounding around the sample hold.
- 2) The Analog and Digital ground planes should be joined together at the ADC or at the power supplies.

## • Notes •

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**GENERAL INFORMATION****1*****DIGITAL AUDIO:*****DIGITAL AUDIO PRODUCTS****2****Digital Volume Control****Multimedia Codecs****Digital-to-Analog Converters****Analog-to-Digital Converters****AES/EBU & S/PDIF Interfaces*****DATA ACQUISITION:*****ANALOG-TO-DIGITAL CONVERTERS****3****General Purpose & Military****Seismic****DC Measurement****Transducer Interface*****SUPPORT FUNCTIONS:*****SUPPORT FUNCTION PRODUCTS****4****Power Monitor****Track & Hold Amplifiers****Voltage References*****COMMUNICATIONS:*****COMMUNICATIONS PRODUCTS****5****T1/CEPT Line Interfaces & Framers****Jitter Attenuators****T3 Receiver****Local Area Network I.C.s****DTMF Receivers*****MISCELLANEOUS:*****APPLICATION NOTES & PAPERS****6****APPENDICES****7****Radiation Information****Reliability Calculation Methods****Package Mechanical Drawings****SALES OFFICES****8**

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**DEFINITION OF PRELIMINARY PART TYPES**

Before a part is in full production, Crystal will supply preliminary parts. There are two varieties:

**I. Engineering Sample (ES)**

Engineering sample "ES" is a product which has not been completely characterized or where qualification has not reached the first lot 500 hours read point. ES product will be assembled per manufacturing specs at qualified assembly sites. All units will be tested to a published data sheet and applicable errata sheet (if needed). Any ES units which are tested only at room temperature will receive a supplemental brand "25°". As soon as automated temperature testing is available for this device, all subsequent ES units will be 100% temperature tested.

The following premium - temperature product grades will always be 100% tested at temperature:

TELECOMMUNICATIONS - "M" grade  
DATA ACQUISITION - "A", "B", "C", "S",  
"T", and "U" grades

**II. Engineering Prototype (EP)**

Engineering Prototype is an engineering prototype of a device which works sufficiently for beta site purposes.

**DEFINITION OF DATA SHEET TYPES**

Each product developed by Crystal will be supported by technical literature where the data sheets progress through the following levels of refinement:

**I. Product Preview**

This is a 1-to-4 page document which describes the main features and specifications for a product that is under development. Some specifications such as exact pin-outs may not be finalized at time of publication. The purpose of this document is to provide customers with advance product planning information.

**II. Preliminary Product Information**

This is the first document completely describing a new product. It contains an overview, specifications, timing diagrams, theory of operation, pin-out diagram, applications information, ordering guide and mechanical information. The numbers in this data sheet are based on prototype silicon performance and on worst-case simulation models. The specifications represent the designer's best estimate for the "real" numbers. Min and max values are included where possible. The purpose of this document is to provide system designers with technical information sufficiently detailed to guarantee that they can safely begin active development.

**III. Final Data Sheet**

This is an updated version of the preliminary data sheet reflecting actual production performance of the final product. Updates include tighter specifications, more min and max values, and any application information that has arisen during the early life of the part. The purpose of this document is to communicate the confirmed performance of products which have passed qualification, been fully characterized, and are in production.



## RADIATION RESISTANCE PERFORMANCE

Crystal products are manufactured using 1, 2 and 3 micron CMOS processes. While not able to withstand large doses of radiation, our products are suitable for operation in low dose applications. Indeed, the self calibrating architecture of many of the A/D Converters is able to compensate for the effects of radiation.

Crystal will assist customers to test parts for radiation resistance by supplying free, data-logged parts. In exchange, we would like the

parts returned to us, so that we can measure their post-radiation performance. In addition, we would like a copy of any report that is generated, along with permission to publish the report for other customer's information.

Several customer's have already undertaken radiation testing of our A/D Converters. Please contact the factory for the latest information and copies of the radiation performance reports.

## RELIABILITY METHODS

### I. CONCEPT OF RELIABILITY

In general terms, the reliability of a semiconductor device is defined as the measure of the functional stability of the device with respect to time. Expressed in a more quantitative sense, it is the probability that the device will operate with a specified performance over a specified period of time under a given set of conditions.

Reliability characteristics are usually stated in reverse terms as the loss of ability to function, or failure rate. The reliability performance of a device can best be summarized by the reliability life or "bathtub" curve (Figure 1). The reliability performance is characterized by three phases: infant mortality, useful life, and wearout. Infant mortality failures can be reduced by proper manufacturing controls and screening techniques. The useful life period is typically a long period of time where only occasional random failures occur. During this time the failure rate is usually very low. The final period is aptly named wearout. Using proper design guidelines and device applications, this period is shifted well beyond the lifetime required by the user.

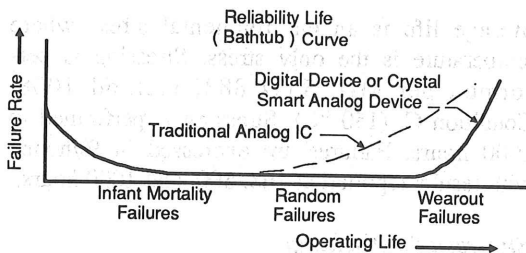


Figure 1.

An item of great importance in evaluating reported reliability characteristics is the definition of a failure. Crystal's definition of a failure is any device that fails to meet ANY data sheet parameter. Crystal's digital self-calibration techniques provide stable performance over temperature

and life. Traditional Analog IC's and hybrids exhibit wearout mechanisms very early in the life of the product. One competitor's analog-to-digital converter's linearity error stability is specified at  $\pm 0.00075\%$  per 1000 hours at  $25^\circ\text{C}$ . Stability degradation at  $70^\circ\text{C}$  is unspecified and is likely to be accelerated greatly as temperature increases. The dashed line of Figure 1 is typical of the wearout seen in a competitor's Analog IC or hybrid. As you can see, wearout begins much earlier than a digital device or a mixed analog and digital chip utilizing Crystal's SMART analog design architecture and CMOS wafer technology.

### II. CRYSTAL SEMICONDUCTOR RELIABILITY STRESSING

These stresses are done on every new product, assembly house or fabrication subcontractor. The Crystal acceptance criteria and goals are as described in Table 1 of the Quality and Reliability information in section 1 of this data book.

#### Accelerated Operating Life Stress

Accelerated operating life stressing is performed to accelerate thermally-activated failure mechanisms through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are  $125^\circ\text{C}$  with a bias level at the maximum data sheet specifications. Some devices may be stressed at an even higher voltage level to further stress the oxides of the device. All devices used in life stress are sampled directly from the production flow with no special processing or pre-screening. Stressing is performed per MIL STD 883, method 1015, condition D (dynamic signals). These dynamic conditions simulate as much as possible actual operating conditions in an application.

Both infant mortality operating life stress (168 hrs at 125 °C) and long term operating life (typically 1000 hrs at 125 °C) are reported. Infant mortality life simulates approximately 6-8 months in the field at 70 °C and is reported as %/168 hrs. Long term life simulates the total failure seen in the field and is expressed in FITS (failures in time). 1 FIT = 1 failure per billion device-hours. Derating of long term operating life is done using Arrhenius thermal equations along with Weibull statistics. A 60 % upper confidence limit (UCL) and .7 electron volts (eV) activation energy are used in this calculation.

#### **85 °C/85% R.H.**

85 °C/ 85% R.H. is an environmental stress performed at a temperature of 85 °C and at a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated devices. A nominal-voltage static bias is applied, with minimum power consumption, to the device, to accelerate the electrolytic corrosion of the metallization. Failures are expressed in % /time with 168, 500, and 1000 hour cumulative results reported.

#### **Autoclave**

Autoclave is also an environmental stress which measures the moisture resistance of plastic encapsulated devices. Conditions for this test are 121 °C, 100% relative humidity, and 1 atmosphere of pressure (15 psig), with no bias applied to the circuit. Corrosion of the die is the expected failure mechanism. Stressing is usually performed for 144 hours. Failures are expressed in %/time with 48, 96, and 144 hour results reported.

#### **Temperature Cycling**

Temperature cycling typically accelerates the effects of the thermal expansion mismatch among the different components within a specific package and circuit. The stress is performed per MIL STD 883, method 1010, Condition C (-65 °C

to +150 °C). Stressing is done in an air environment. A cycle consists of ten minutes at -65 °C, five minutes transfer time, and ten minutes at +150 °C. Stressing is typically performed for 1000 cycles. Failures are expressed in %/cycles, with 100, 500, and 1000 cycle results reported.

#### **Thermal Shock**

The objective of thermal shock is basically the same as that of temperature cycling - to exercise the difference in thermal expansion coefficients within the integrated circuit package and die. Thermal shock provides additional stress as the device is exposed to a rapid change in temperature, due to a maximum transfer time of ten seconds, as well as the increased thermal conductivity of a liquid environment. This test is performed per MIL STD 883, method 1011, Condition B (-55 °C to +125 °C). In one cycle of thermal shock, devices are placed in a fluoro-carbon bath cooled to -55 °C for five minutes, then transferred to an adjacent bath filled with fluoro-carbon at 125 °C for five minutes. Stressing is performed for 500 cycles. Failures are expressed in %/cycles, with results reported at 100, 200, and 500 cycles.

#### **High Temperature Storage Life**

Storage life is an environmental stress where temperature is the only stress. Stressing is performed per MIL STD 883, method 1008, Condition C. (150 °C). Stressing is performed to 1000 hours. Failures are expressed in %/hours, with results reported at 168, 500, and 1000 hours.

#### **Electrostatic Discharge**

Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device. This test is performed per MIL STD 883 method 3015, which simulates the resistance (1500Ω) and capacitance (100 pF) of the human body. Also the machine model test is performed with a 0Ω resistance and a capacitance of

200 pF to simulate, as its name implies, a typical insertion tool, handler, etc. that comes in contact with the leads of a semiconductor device.

### Latchup

Latchup testing is performed to ascertain whether a device can sustain SCR latchup due to a DC current input. The pin being tested has a DC current forced to it with the device power supplies at nominal voltage and inputs at ground state. Susceptibility of each input is tested with both a positive and negative DC current forced into it. This test is performed per the standard test procedure recognized by JEDEC.

### C dv/dt Latchup Testing

This test is performed to evaluate the susceptibility of a CMOS device's power pin to instantaneous ESD discharge into a power supply pin or a rapid ramp of a power pin during power up. Positive and negative pulses are supplied to the power supply pins with a change in voltage of greater than 500 V/ $\mu$ s and a 0 to 5 V risetime of less than 15 ns. Ground,  $V_{SS}$ , and the pin under test are connected to ground. The supply current is monitored for excessive current.

## III. FAILURE RATE CALCULATIONS

Failures during typical reliability stressing generally are in the infant mortality and random failure sections of the "bathtub" curve. Thermally accelerated failure rates can be derated to actual operating conditions by commonly accepted mathematical models.

Operating life stress is usually reported in the derated form. That is, operating life is performed at 125 °C and results are reported for an equivalent time at a typical operating stress temperature for an application, generally 25 °C, 55 °C, or 70 °C. Failure rates for other tempera-

tures are calculated using a computed acceleration factor.

There are many probability models used in reliability analysis for calculating failure rates. The simplest form of calculating a failure rate (F.R.) would be to divide the number of failures observed after test (N) by the number of device-hours of stress.

$$F.R. = \frac{N}{D \cdot H} \quad (1)$$

where D is the number of devices stressed and H is the number of stress hours. If this number is multiplied by  $10^9$  we obtain the failure rate expressed as Failure In Time (FIT). FITS are expressed as failures per billion device operating hours.

$$FITS = (F.R.) (10^9) \quad (2)$$

However, using equation (1) allows only for a failure rate calculation at the stress temperature. In order to apply the equation to the desired use temperature we use the well-known Arrhenius relationship to determine the thermal acceleration factor,  $F_a$ . One hour of device operation at temperature  $T_1$  is equivalent to  $F_a$  hours of operation at temperature  $T_2$ . The activation energy, EA, is an important parameter in the Arrhenius equation and is discussed below. The Arrhenius equation is:

$$F_a(T_1 \rightarrow T_2) = e^{\frac{EA}{k} \left( \frac{1}{T_1} - \frac{1}{T_2} \right)} \quad (3)$$

where k = Boltzman's Constant ( $8.63 \times 10^{-5}$  eV/°K) and  $T_1$  is the accelerated stress junction temperature and  $T_2$  is the desired use operating junction temperature in degrees Kelvin.

Junction temperatures,  $T_1$  and  $T_2$ , should be used in determining acceleration factors. This temper-

ture can be obtained from the equation below.

$$T_j = T_a + \theta_{ja} P_d \quad (4)$$

where  $T_a$  is the operating ambient temperature and  $\theta_{ja}$  is the package thermal dissipation ( $^{\circ}\text{C}/\text{W}$ ) and  $P_d$  is the device power dissipation.

Crystal utilizes a low power CMOS process which typically raises the junction temperature about 7 to 15  $^{\circ}\text{C}$ , whereas analog bipolar IC's and hybrids can have power dissipations in the 1 W range. These differences in device junction operating temperatures can greatly affect the acceleration factors. For example, let's calculate the acceleration factors of a device with a power dissipation of 1 watt packaged in a 40 pin ceramic package. This is equivalent to a junction temperature change from 160  $^{\circ}\text{C}$  to 60  $^{\circ}\text{C}$  and from Table 2 the acceleration factor is 277. A typical Crystal device junction temperature is 10  $^{\circ}\text{C}$  higher than the ambient which results in a junction tempera-

TEMPERATURE CHANGE	ACCELERATION FACTOR
125 --> 70 $^{\circ}\text{C}$	26.3
125 --> 55 $^{\circ}\text{C}$	77.5
125 --> 25 $^{\circ}\text{C}$	933.0
135 --> 35 $^{\circ}\text{C}$	636
160 --> 60 $^{\circ}\text{C}$	277

TABLE 2  
ACCELERATION FACTORS FOR DIFFERENT  
TEMPERATURES (E. A. = .7 eV)

E. A.	ACCELERATION FACTOR
1.0	106.0
.9	66.7
.8	41.7
.7	26.3
.6	16.4
.5	10.3
.4	6.5
.3	4.1

TABLE 3  
ACCELERATED FACTORS FOR DIFFERENT  
ACTIVATION ENERGIES (125  $^{\circ}\text{C}$  --> 70 $^{\circ}\text{C}$ )

ture change from 135  $^{\circ}\text{C}$  to 35  $^{\circ}\text{C}$ . This results in an acceleration factor of 636, as shown in Table 2. By comparing the results in Table 2 one can see how derating to a lower use temperature or failing to consider junction temperature when calculating acceleration factors can result in greatly differing failure rates.

Table 3 compares acceleration factors for different activation energies. Using a 1.0 eV activation energy versus a .7 eV activation energy results in a factor of four increase in the acceleration factor. Crystal uses an activation energy of .7 eV, a conservative value, compared to the .8 eV to 1.0 eV used by other analog IC vendors.

We now take the failure rate equation (1) at accelerated temperatures expressed in FITS and factor in the acceleration factors from the Arrhenius relationships considering junction temperatures and arrive at the equation below.

$$\text{FITS} = \frac{10^9 N}{\text{DHF}_a} \quad (5)$$

Using composite Crystal data through the 1st quarter of 1988, a failure rate at 25 $^{\circ}\text{C}$  can be calculated by substituting in equation (5) above:

$$N = 23$$

$$D \cdot H = 5,371,036$$

$$F_a = 702 \text{ (Assuming .7 eV and stress temperature of 125 $^{\circ}\text{C}$ , using junction temperature derating)}$$

$D \cdot H$  is the summation of the devices stressed at each readpoint multiplied by that number of stress hours.

Substituting we get:

$$\text{FITS } 25^{\circ}\text{C} = \frac{(10^9)(23)}{(5,371,036)(702)}$$

The Weibull distribution is often used for product life predictions because it can describe increasing and decreasing failure rates. Also the Weibull dis-

tribution has both a shape parameter,  $\beta$ , and a scaling parameter,  $\alpha$ . This is very useful in accurately describing the shape and scaling of the "bathtub" curve. These more accurate descriptions of the failure rate of the Weibull distribution make this method superior to the uniform failure distribution described in Equation (1). The Weibull probability distribution function (PDF)  $f(t)$  is the probability of failure between time  $t$  and  $t + dt$ .

$$f(t) = \frac{\beta}{\alpha} t^{(\beta-1)} e^{-\left(\frac{t}{\alpha}\right)^\beta} \quad (6)$$

The Weibull PDF can also be expressed as a function of the Reliability function,  $R(t)$ , and the instantaneous failure rate function,  $h(t)$ , therefore:

$$f(t) = h(t)R(t) \quad (7)$$

The Reliability function is found by integrating the Weibull PDF from  $t$  to  $\infty$ . This function is the probability that a device will survive to time  $t$ .

$$R(t) = \int_t^\infty f(t') dt' = e^{-\left(\frac{t}{\alpha}\right)^\beta} \quad (8)$$

The instantaneous failure rate function is the probability that a device will fail between time  $t$  and  $t+dt$ :

$$h(t) = -\frac{1}{R} \frac{dR}{dt} = \frac{\beta}{\alpha} t^{(\beta-1)} \quad (9)$$

The Reliability function is used to calculate the shape parameter,  $\beta$ , and the time scale parameter,  $\alpha$ . The shape parameter is the key function in shaping the infant mortality portion of the "bathtub" curve. A  $\beta$  of 1 indicates a uniform failure rate,  $\beta > 1$  indicates wearout and  $\beta < 1$  indicates a declining failure rate. To use Weibull statistics, failures that occur during operating life stresses are used to produce values of  $R(t)$ . Failure times and  $R(t)$  values can be combined to estimate  $\alpha$

and  $\beta$ . We first take the natural logarithm of both sides of equation (8).

$$\ln \left( \frac{1}{R(t)} \right) = \frac{t^\beta}{\alpha^\beta}$$

We again take the natural logarithm and obtain:

$$\ln \left[ \ln \frac{1}{R(t)} \right] = \beta \ln(t) - \ln(\alpha) \quad (10)$$

This last equation is now in the form of a linear function. Using linear regression techniques or Weibull plotting paper we obtain the Weibull shape and scale parameter. Most semiconductor manufacturers perform a burn-in screening on devices to insure that the end customer receives a population of devices that have minimal infant mortality and are from the useful life period of the reliability "bathtub" curve. It is very important to include this data for the entire lifetime of the device to obtain an accurate curve fit for obtaining  $\alpha$  and  $\beta$ .

Once the parameters  $\alpha$  and  $\beta$  for the Weibull distribution are known we utilize  $R(t)$  to calculate FITS. Crystal uses a 20 year lifetime in its FIT calculations and typically uses a 48 hour burn-in at 125 °C hence:

$$\begin{aligned} t_{20} &= 20 \text{ yrs} = 175,200 \text{ hours} \\ t_1 &= 48 \text{ hours} \end{aligned}$$

The number of devices that will fail in the twenty year lifetime following burn-in is given by:

$$N = D [R(t_1) - R(t_1 + t_{20})] \quad (11)$$

where  $D$  is the total number of devices stressed. The number of device-hours accumulated in 20 years can be estimated by counting the devices surviving after 20 years.

$$DH \geq D \cdot R(t_1 + t_{20}) \cdot t_{20} \quad (12)$$



Using equation (2) for expressed failures in FITS we obtain the equation below for a Weibull distribution

$$\begin{aligned} \text{FITS} &\leq 10^9 \frac{D [R(t_1) - R(t_1 + t_{20})]}{D \cdot R(t_1 + t_{20}) \cdot (t_{20})} \\ &= \frac{10^9 [R(t_1) - R(t_1 + t_{20})]}{R(t_1 + t_{20}) \cdot (t_{20})} \end{aligned} \quad (13)$$

The above equation applies only at the stress temperature. In order to apply the equation to the desired use temperature we factor in the acceleration factors,  $F_a$ , from the Arrhenius relationship as it relates to time in the reliability function. Therefore in equation (12) above we replace  $R(t_1 + t_{20})$  by  $R(t_1 + t_{20}/F_a)$ . Note that the device lifetime  $t_{20}$  is still 20 years but the reliability function must have the acceleration factor considered for derating to use temperature. Using composite Crystal data through the first quarter of 1988, and using from equation (10),  $\beta = .19$  and  $\alpha = 521$  and  $F_a = 702$  yields a failure rate at 25 °C of 9.7 FITS.

This failure rate is a more accurate measure of Crystal reliability than that provided by the constant failure rate model of equation (5).

Reliability evaluations involve only samples of an entire population of devices. Therefore a confidence level, (CL), should be placed on the average failure rate. At any time a sample is stressed from a population there exists a finite chance of failures. If many separate samples were stressed from the same population and failure rates plotted, a normal distribution of failure rates would occur. Therefore, valid statistical methods for a normal distribution should be used to determine the desired CL. Confidence levels for reliability analysis are expressed in upper confidence levels (UCL), typically at 60% or 90% depending on the criticality of the device's application. The total sample size stressed is critical

in defining the UCL. Therefore rather large sample sizes must be stressed to more accurately demonstrate the true failure rate. A larger spread will exist between the 50% and 90% UCL distribution for smaller sample sizes due to the greater probability that the sample stressed was not representative of the entire population.

Environmental stresses, such as autoclave, temperature cycling, thermal shock, storage life and 85 °C/85%R.H., usually have their actual results reported, due to the lack of widely recognized derating models. These are usually expressed as %failure / stress time. An example of this would be a temperature cycling failure rate expressed as %/ 1000 cycles. These failure rates should have a confidence level associated with the data given. For environmental stresses, Crystal publishes data with a 90% confidence level. To calculate this failure rate with confidence levels, the following binomial probability statistics calculations are made:

$$P_c = P_a + Z \frac{[P_a (100 - P_a)]^{1/2}}{n} \quad (14)$$

where  $P_c$  is the failure rate with confidence level,  $P_a$  is the observed failure rate in percentage defective,  $n$  is the number of samples stressed, and  $Z$  is the value of the standard normal probability distribution associated with the desired confidence level. ( $Z = 1.28$  for 90% UCL.) This calculation agrees with the widely accepted lot tolerance percent defective, LTPD, plans that are based on 90 % upper confidence.

Of course it is not satisfactory to have accurate methods on reporting failure rates without having programs and methods in place to continuously improve the reliability of the product. Crystal uses methodologies in every level of the company to provide the highest possible quality and reliability standards of its products.

Using the reliability calculation methods of Maxim, an analog IC quality leader, Crystal achieves a failure in time (FIT) rate of 6.1 parts per billion operating hours. This compares favorably with Maxim's own performance of 6.8 FITs. Crystal's reliability is also established for devices requiring far greater analog accuracy than its competitors' products.

In summary Crystal Semiconductor uses conservative models that are accepted throughout the semiconductor industry to determine the reliability

of its devices and has active programs in place to continuously improve the quality and reliability of its devices.

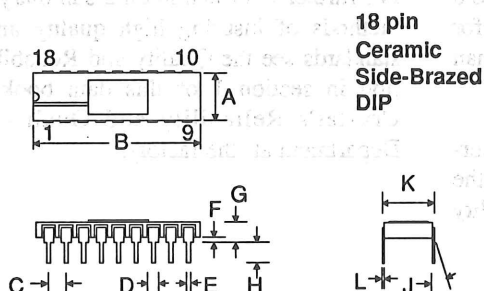
For further information on a summary of Crystal's methods of insuring high quality and reliability standards see the Quality and Reliability information in section 1 of this data book, or contact Crystal's Reliability and Quality Assurance Department at the factory.

Part No.	Lot No.	Test Date	Test Result	Test Method
1000	1000	10/10/00	Pass	100%
1001	1001	10/10/00	Pass	100%
1002	1002	10/10/00	Pass	100%
1003	1003	10/10/00	Pass	100%
1004	1004	10/10/00	Pass	100%
1005	1005	10/10/00	Pass	100%
1006	1006	10/10/00	Pass	100%
1007	1007	10/10/00	Pass	100%
1008	1008	10/10/00	Pass	100%
1009	1009	10/10/00	Pass	100%
1010	1010	10/10/00	Pass	100%
1011	1011	10/10/00	Pass	100%
1012	1012	10/10/00	Pass	100%
1013	1013	10/10/00	Pass	100%
1014	1014	10/10/00	Pass	100%
1015	1015	10/10/00	Pass	100%
1016	1016	10/10/00	Pass	100%
1017	1017	10/10/00	Pass	100%
1018	1018	10/10/00	Pass	100%
1019	1019	10/10/00	Pass	100%
1020	1020	10/10/00	Pass	100%

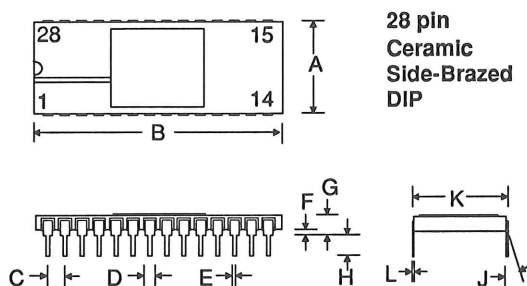
Part No.	Lot No.	Test Date	Test Result	Test Method
1021	1021	10/10/00	Pass	100%
1022	1022	10/10/00	Pass	100%
1023	1023	10/10/00	Pass	100%
1024	1024	10/10/00	Pass	100%
1025	1025	10/10/00	Pass	100%
1026	1026	10/10/00	Pass	100%
1027	1027	10/10/00	Pass	100%
1028	1028	10/10/00	Pass	100%
1029	1029	10/10/00	Pass	100%
1030	1030	10/10/00	Pass	100%
1031	1031	10/10/00	Pass	100%
1032	1032	10/10/00	Pass	100%
1033	1033	10/10/00	Pass	100%
1034	1034	10/10/00	Pass	100%
1035	1035	10/10/00	Pass	100%
1036	1036	10/10/00	Pass	100%
1037	1037	10/10/00	Pass	100%
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1039	1039	10/10/00	Pass	100%
1040	1040	10/10/00	Pass	100%



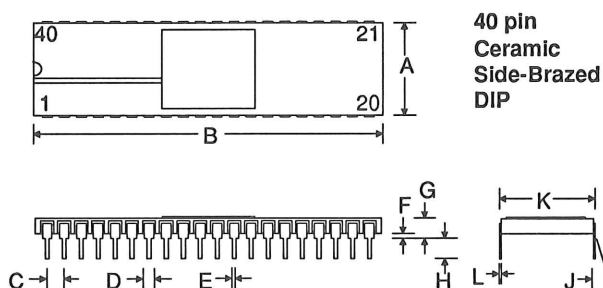
### MECHANICAL DATA



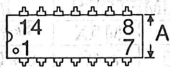
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.29	7.70	0.287	0.303
B	22.63	23.09	0.891	0.909
C	2.54	BSC	0.100	BSC
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.67	4.32	0.105	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	7.62	8.13	0.300	0.320
L	0.20	0.30	0.008	0.012



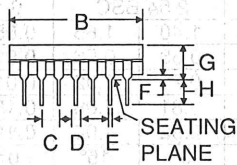
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54	BSC	0.100	BSC
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.63	15.49	0.576	0.610
B	50.29	51.31	1.980	2.020
C	2.54	BSC	0.100	BSC
D	0.76	1.52	0.030	0.060
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.65	0.590	0.616
L	0.20	0.30	0.008	0.012



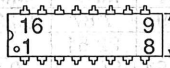
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CerDIP



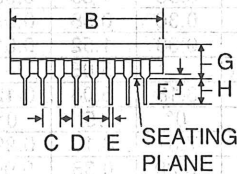
NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.49	0.240	0.295
B	19.05	19.94	0.750	0.785
C	2.54 BSC		0.100 BSC	
D	1.40	1.78	0.055	0.070
E	0.38	0.53	0.015	0.021
F	0.51	1.02	0.020	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.32	0.115	0.170
J	-	15°	-	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012



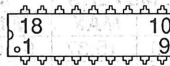
16 pin  
CerDIP



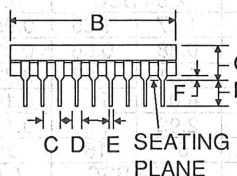
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2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.49	0.240	0.295
B	19.05	19.94	0.750	0.785
C	2.54 BSC		0.100 BSC	
D	1.40	1.78	0.055	0.070
E	0.38	0.53	0.015	0.021
F	0.51	1.02	0.020	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.32	0.115	0.170
J	-	15°	-	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012



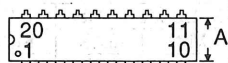
18 pin  
CerDIP



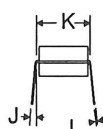
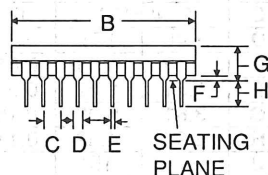
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2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.49	0.240	0.295
B	22.35	23.11	0.880	0.910
C	2.54 BSC		0.100 BSC	
D	1.40	1.78	0.055	0.070
E	0.38	0.53	0.015	0.021
F	0.51	1.02	0.020	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.32	0.115	0.170
J	0°	15°	0°	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012



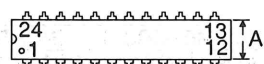
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CerDIP



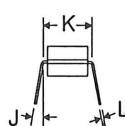
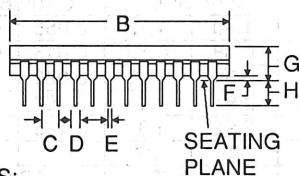
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2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.60	7.49	0.260	0.295
B	23.88	25.15	0.940	0.990
C	2.54	BSC	0.100	BSC
D	1.40	1.65	0.055	0.065
E	0.38	0.56	0.015	0.022
F	0.25	1.02	0.010	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.06	0.115	0.160
J	0°	15°	0°	15°
K	7.62	BSC	0.300	BSC
L	0.20	0.30	0.008	0.012



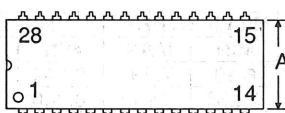
24 pin  
Skinny  
CerDIP



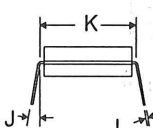
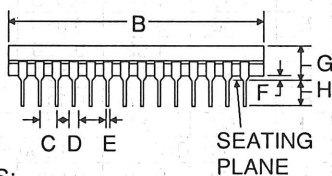
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2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.59	7.87	0.220	0.310
B	-	32.51	-	1.280
C	2.54	BSC	0.100	BSC
D	0.96	1.65	0.038	0.065
E	0.36	0.58	0.014	0.023
F	0.38	1.52	0.015	0.060
G	-	5.08	-	0.200
H	3.18	5.08	0.125	0.200
J	0°	15°	0°	15°
K	7.37	8.13	0.290	0.320
L	0.20	0.38	0.008	0.015



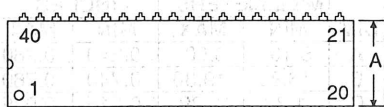
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CerDIP



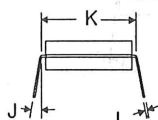
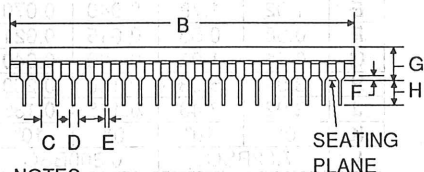
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2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.37	0.500	0.605
B	36.45	37.85	1.435	1.490
C	2.54	BSC	0.100	BSC
D	1.27	1.65	0.050	0.065
E	0.38	0.56	0.015	0.022
F	0.51	1.27	0.020	0.050
G	4.06	5.84	0.160	0.230
H	2.92	4.06	0.115	0.160
J	5°	15°	5°	15°
K	15.24	BSC	0.600	BSC
L	0.20	0.30	0.008	0.012



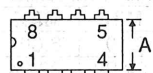
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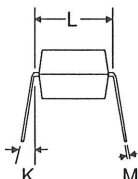
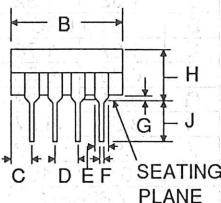
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2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.37	0.500	0.605
B	50.29	52.57	1.980	2.070
C	2.54 BSC		0.100 BSC	
D	1.27	1.65	0.050	0.065
E	0.38	0.56	0.015	0.022
F	0.51	1.27	0.020	0.050
G	4.06	5.84	0.160	0.230
H	2.92	4.06	0.115	0.160
J	5°	15°	5°	15°
K	15.24 BSC		0.600 BSC	
L	0.20	0.30	0.008	0.012



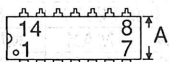
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Plastic DIP



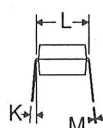
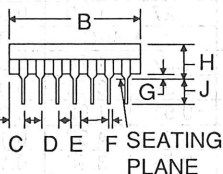
**NOTES:**

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015



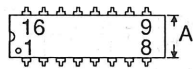
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Plastic DIP



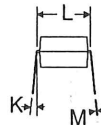
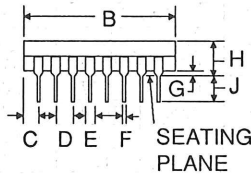
**NOTES:**

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.54	19.56	0.730	0.770
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015



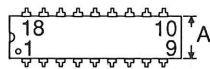
16 pin  
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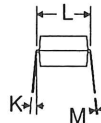
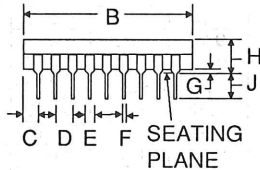
**NOTES:**

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015



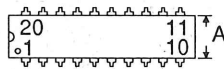
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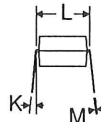
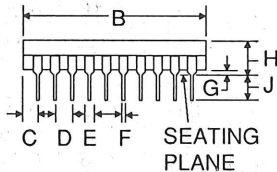
**NOTES:**

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	22.22	23.24	0.875	0.915
C	1.02	1.52	0.040	0.060
D	2.54 BSC		0.100 BSC	
E	1.27	1.78	0.050	0.070
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.56	4.57	0.140	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015



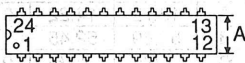
20 pin  
Plastic DIP



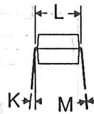
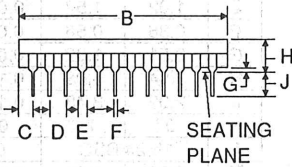
**NOTES:**

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	25.65	26.42	1.010	1.040
C	1.27	1.78	0.050	0.070
D	2.54 BSC		0.100 BSC	
E	1.27	1.78	0.050	0.070
F	0.38	0.56	0.015	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.79	3.56	0.110	0.140
K	0°	15°	0°	15°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015



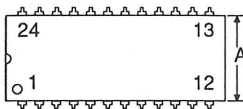
24 pin  
Plastic  
Skinny DIP



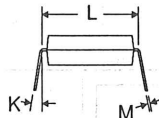
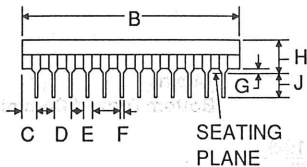
**NOTES:**

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015



24 pin  
Plastic DIP



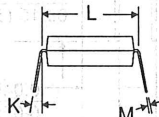
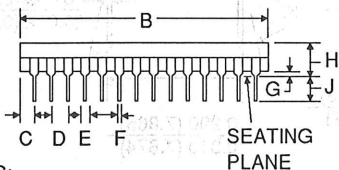
**NOTES:**

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015



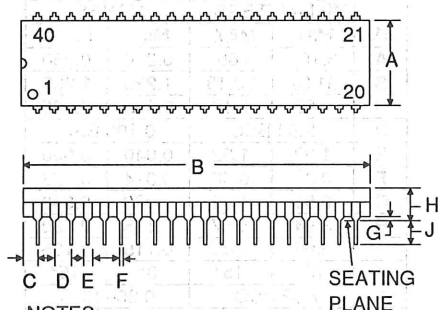
28 pin  
Plastic DIP



**NOTES:**

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
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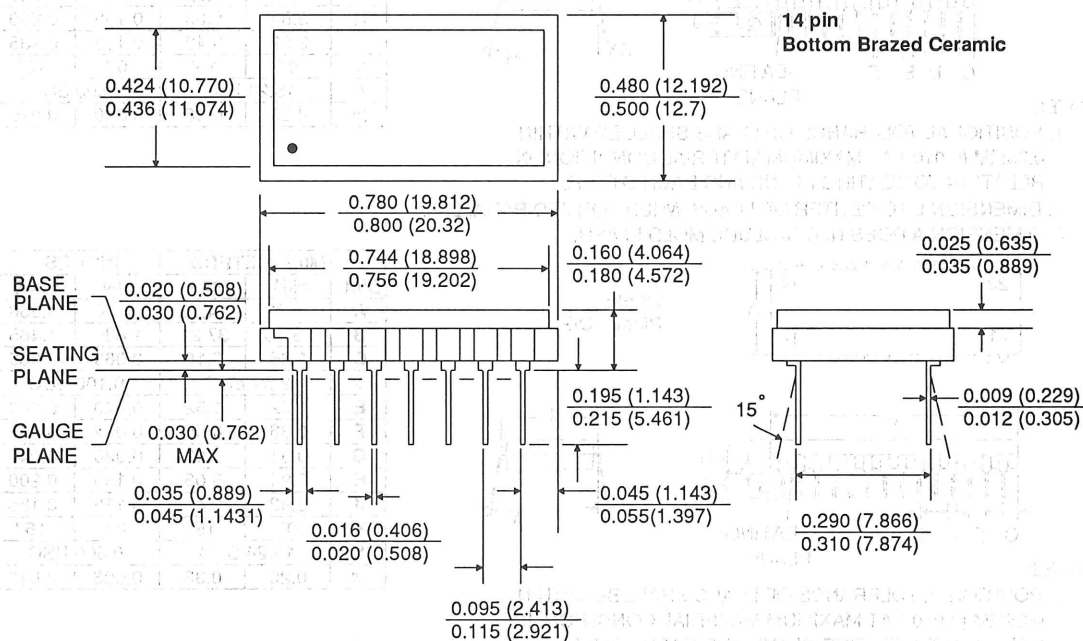
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015



### NOTES:

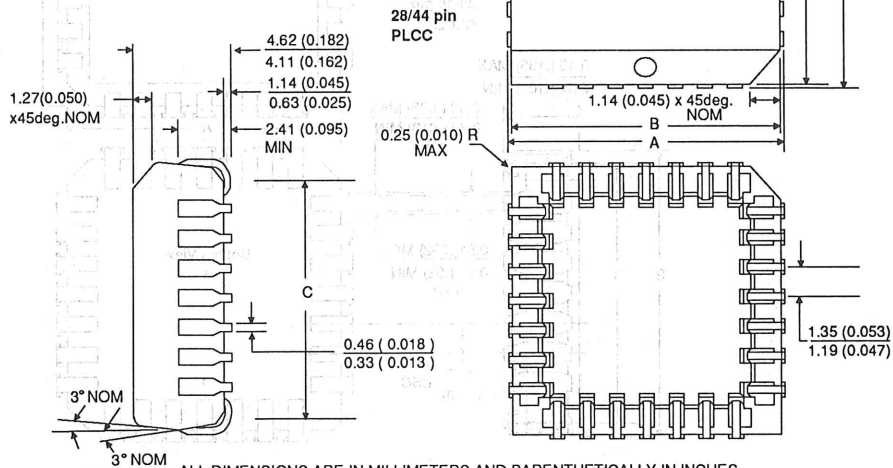
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	51.69	52.45	2.035	2.065
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

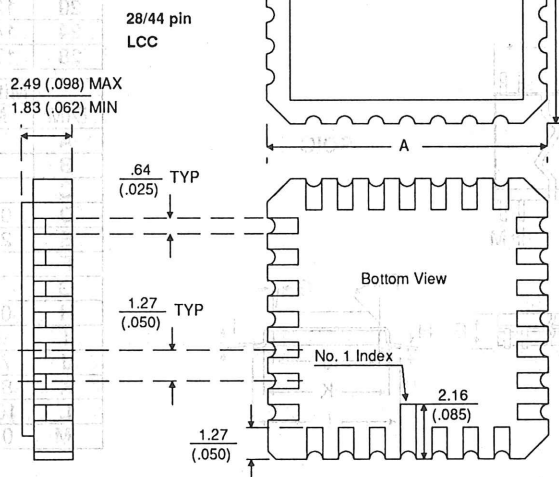




NO. OF TERMINAL	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
28	12.32 (.485)	12.57 (.495)	11.43 (.450)	11.58 (.456)	9.91 (.390)	10.92 (.430)
44	17.40 (.685)	17.65 (.695)	16.51 (.650)	16.66 (.656)	14.98 (.590)	16.00 (.630)

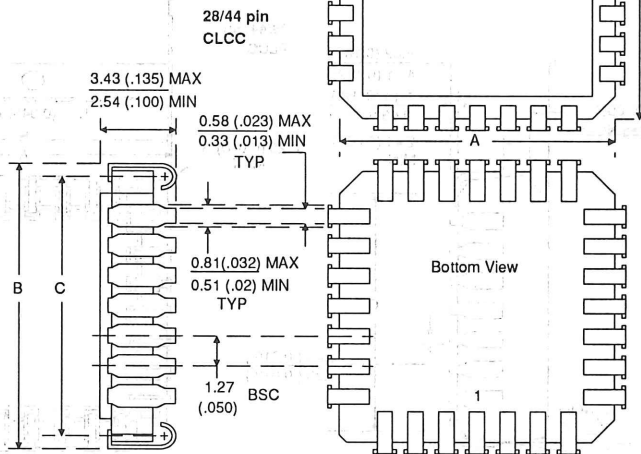


NO. OF TERMINALS	A	
	MIN	MAX
28	11.25 (.443)	11.73 (.462)
44	16.33 (.643)	16.81 (.662)

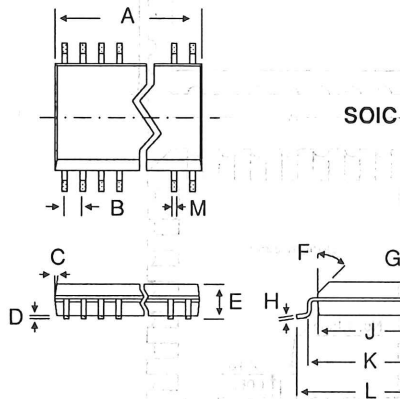




NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
28	NA		NA		NA	
44	16.26 (.640)	16.77 (.660)	17.28 (0.680)	17.79 (0.700)	15.50 (0.610)	16.52 (0.650)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



pins	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	see table above			
B	1.27	BSC	0.050	BSC
C	7°	NOM	7°	NOM
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45°	NOM	45°	NOM
G	7°	NOM	7°	NOM
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

**GENERAL INFORMATION*****DIGITAL AUDIO:*****DIGITAL AUDIO PRODUCTS**

Digital Volume Control  
Multimedia Codecs  
Digital-to-Analog Converters  
Analog-to-Digital Converters  
AES/EBU & S/PDIF Interfaces

***DATA ACQUISITION:*****ANALOG-TO-DIGITAL CONVERTERS**

General Purpose & Military  
Seismic  
DC Measurement  
Transducer Interface

***SUPPORT FUNCTIONS:*****SUPPORT FUNCTION PRODUCTS**

Power Monitor  
Track & Hold Amplifiers  
Voltage References

***COMMUNICATIONS:*****COMMUNICATIONS PRODUCTS**

T1/CEPT Line Interfaces & Framers  
Jitter Attenuators  
T3 Receiver  
Local Area Network I.C.s  
DTMF Receivers

***MISCELLANEOUS:*****APPLICATION NOTES & PAPERS****APPENDICES**

Radiation Information  
Reliability Calculation Methods  
Package Mechanical Drawings

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**SALES OFFICES****8**

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Europe Representatives . . . . .	8-9
Far East Representatives . . . . .	8-10

**UNITED STATES****SALES OFFICES****WESTERN AREA**

Sales Office and  
Applications Support:  
Crystal Semiconductor Corp.  
50 Airport Parkway  
San Jose, CA 95110  
Ph: 408-437-7743  
FAX: 408-437-4943

Crystal Semiconductor Corp.  
27281 Las Ramblas, Suite 200  
Mission Viejo, CA 92691  
Ph: 714-348-8770  
FAX: 714-348-9556

**CENTRAL AREA**

Crystal Semiconductor Corp.  
4210 So. Industrial Dr.  
Austin, TX 78744  
Ph: 512-445-7222  
FAX: 512-445-7581

**EASTERN AREA**

Crystal Semiconductor Corp.  
8601 Six Forks Rd., Suite 703  
Raleigh, NC 27615  
Ph: 919-846-4832  
FAX: 919-846-4839

Crystal Semiconductor Corp.  
790 Turnpike St. #202  
North Andover MA 01845  
Ph: 508-794-1194  
FAX 508-685-7107

**SALES REPRESENTATIVES****ALABAMA**

Currie, Peak and Frazier, Inc.  
2317 Starmount Circle  
P.O. Box 1424  
Huntsville, AL 35807  
Ph: 205-536-1506  
FAX: 205-551-0558

**ALASKA**

Electronic Engineering Sales  
17020 S.W. Upper Boones Ferry Rd.,  
Suite 301  
Portland, OR 97224  
Ph: 503-639-3978  
FAX: 503-684-3326

**ARIZONA**

Western High Tech Marketing, Inc.  
9414 E. San Salvador, Suite 206  
Scottsdale, AZ 85258  
Ph: 602-860-2702  
FAX: 602-860-2712

**ARKANSAS**

TL Marketing, Inc.  
14850 Quorum Dr., #100  
Dallas, TX 75240  
Ph: 214-490-9300  
FAX: 214-960-6075

**CALIFORNIA**

Earle Associates, Inc.  
7585 Ronson Road, Suite 200  
San Diego, CA 92111  
Ph: 619-278-5441  
FAX: 619-278-5443  
Easylink: 62835672

Bager Electronics  
17220 Newhope St., Suite 209  
Fountain Valley, CA 92708  
Ph: 714-957-3367  
FAX: 714-546-2654

Bager Electronics  
6324 Variel Avenue, Suite 314  
Woodland Hills, CA 91367  
Ph: 818-712-0011  
FAX: 818-712-0160

NORCOMP, Inc.  
3350 Scott Blvd., #24  
Santa Clara, CA 95054  
Ph: 408-727-7707  
FAX: 408-986-1947

NORCOMP, Inc.  
2140 Professional Dr. #200  
Roseville, CA 95661  
Ph: 916-782-8070  
FAX: 916-782-8073

**COLORADO**

PromoTech  
2901 S. Colorado Blvd., Suite A  
Denver, CO 80222  
Ph: 303-692-8484  
FAX: 303-692-8416

**CONNECTICUT**

Alpha-Omega Sales Corp.  
P.O. Box 812  
Fairfield, CT 06430  
Ph: 508-664-1118  
FAX: 508-664-3212

**DELAWARE**

Vantage Sales Company  
1930 E. Marlton Pike  
Cherry Hill, NJ 08003  
Ph: 609-424-6777  
FAX: 609-424-8909

**DISTRICT OF COLUMBIA**

New Era Sales, Inc.  
678 Ritchie Highway  
Severna Park, MD 21146  
Ph: 410-544-4100  
FAX: 410-544-6092

**FLORIDA**

Currie, Peak and Frazier, Inc.  
7335 Lake Ellenor Drive  
P.O. Box 593229  
Orlando, FL 32859  
Ph: 407-855-0843  
FAX: 407-851-1464

**GEORGIA**

Currie, Peak and Frazier, Inc.  
2866 Buford Hwy.  
Duluth, GA 30136  
Ph: 404-497-9404  
FAX: 404-497-9412

**HAWAII**

Call Crystal Head Office  
Ph: 512-445-7222

**IDAHO**

Anderson Associates  
270 South Main Street, Suite 108  
Bountiful, UT 84010  
Ph: 801-292-8991  
FAX: 801-298-1503

Electronic Engineering Sales  
17020 S.W. Upper Boones Ferry Rd,  
Suite 301  
Portland, OR 97224  
Ph: 503-639-3978  
FAX: 503-684-3326

**ILLINOIS**

Micro Sales Inc.  
901 W. Hawthorne  
Itasca, IL 60143  
Ph: 708-285-1000  
FAX: 708-285-1008

Stan Clothier Co.  
3910 Old Hwy. 94 S.  
Suite 116  
St. Charles, MO 63304  
Ph: 314-928-8078  
FAX: 314-447-5214

**INDIANA**

TMC Electronics  
599 Industrial Dr.  
Carmel, IN 46032-4292  
Ph: 317-844-8462  
FAX: 317-573-5472

TMC Electronics  
4630-10 W. Jefferson Blvd.  
Ft. Wayne, IN 46804-6800  
Ph: 219-432-5553  
FAX: 219-432-5555

TMC Electronics  
1214 Appletree Lane  
Kokomo, IN 46902-5701  
Ph: 317-459-5152  
FAX: 317-457-3822

**IOWA**

Stan Clothier Co.  
1930 St. Andrews N.E.  
Cedar Rapids, IA 52402  
Ph: 319-393-1576  
FAX: 319-393-7317

**KANSAS**

Stan Clothier Co.  
815 S. Clairborne, Suite 275C  
Olathe, KS 66062  
Ph: 913-829-0073  
FAX: 913-829-0429

**KENTUCKY**

TMC Electronics  
4012 DuPont Circle, Suite 414  
Louisville, KY 40207-4818  
Ph: 502-893-1377  
FAX: 502-896-6679

**LOUISIANA**

TL Marketing, Inc.  
14343 Torrey Chase Blvd, Suite 1  
Houston, TX 77014  
Ph: 713-589-8100  
FAX: 713-580-7517

**MAINE**

Alpha-Omega Sales Corp.  
325 Main St, Suite 301  
North Reading, MA 01864  
Ph: 508-664-1118  
FAX: 508-664-3212

**MARYLAND**

New Era Sales, Inc.  
678 Ritchie Highway  
Severna Park, MD 21146  
Ph: 410-544-4100  
FAX: 410-544-6092

**MASSACHUSETTS**

Alpha-Omega Sales Corp.  
325 Main St, Suite 301  
North Reading, MA 01864  
Ph: 508-664-1118  
FAX: 508-664-3212

**MICHIGAN**

J.M.J. & Associates, Inc.  
678 Front St., Suite 150  
Grand Rapids MI 49504  
Ph: 616-774-9480  
FAX: 616-454-2680

**MINNESOTA**

The Twist Company  
12800 Industrial Park Blvd., Suite 150  
Plymouth, MN 55441  
Ph: 612-550-0922  
FAX: 612-550-0925

**MISSISSIPPI**

Currie, Peak and Frazier, Inc.  
2317 Starmount Circle  
P.O. Box 1424  
Huntsville, AL 35807  
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FAX: 205-551-0558

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